SCAN18373T Transparent Latch with Tri-State Outputs

Check for Samples: SCAN18373T

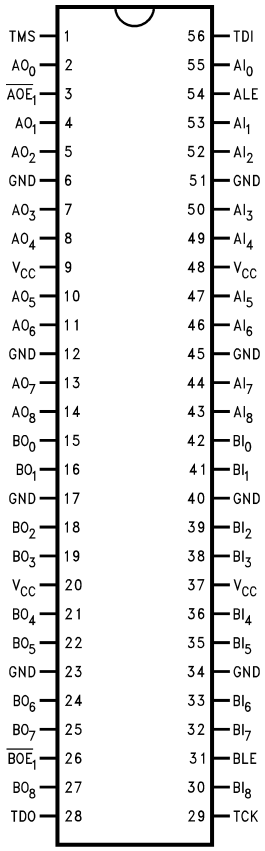
FEATURES

- **IEEE 1149.1 (JTAG) Compliant**
- **Buffered Active-Low Latch Enable**
- **Tri-State Outputs for Bus-Oriented Applications**
- **9-bit Data Busses for Parity Applications**
- **Reduced-Swing Outputs Source 24 mA/Sink 48 mA**
- **Ensured to Drive 50Ω Transmission Line to TTL Input Levels of 0.8V and 2.0V**
- **TTL Compatible Inputs**
- **25 mil Pitch Cerpack Packaging**
- **Includes CLAMP and HIGHZ Instructions**
- **Standard Microcircuit Drawing (SMD) 5962-9311801**

DESCRIPTION

The SCAN18373T is a high speed, low-power transparent latch featuring separate data inputs organized into dual 9-bit bytes with byte-oriented latch enable and output enable control signals. This device is compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture with the incorporation of the defined boundary-scan test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), and Test Clock (TCK).

Connection Diagram



Pin Names	Description
$AI_{(0–8)}$, $BI_{(0–8)}$	Data Inputs
ALE, BLE	Latch Enable Inputs
$\overline{AOE_1}$, $\overline{BOE_1}$	TRI-STATE Output Enable Inputs
$AO_{(0–8)}$, $BO_{(0–8)}$	TRI-STATE Latch Outputs

TRUTH TABLES

Inputs(1)			AO (0–8)
ALE	$\overline{AOE_1}$	AI (0–8)	
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	AO_0

(1) H= HIGH Voltage Level
L= LOW Voltage Level
X= Immaterial
Z= High Impedance
AO_0 = Previous AO before H-to-L transition of ALE
BO_0 = Previous BO before H-to-L transition of BLE

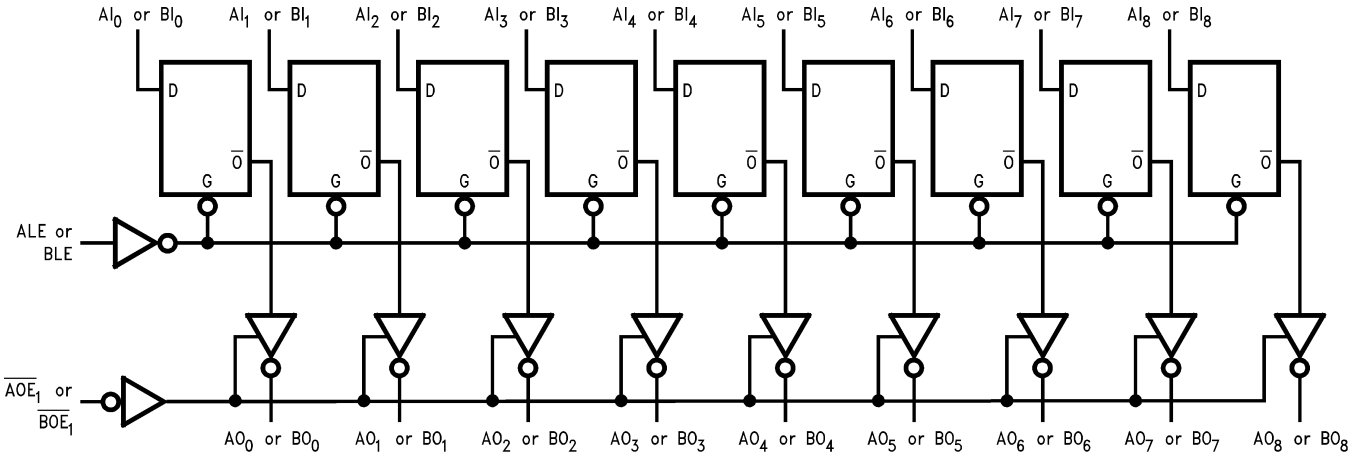
Inputs(1)			BO (0–8)
BLE	$\overline{BOE_1}$	BI (0–8)	
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	BO_0

(1) H= HIGH Voltage Level
L= LOW Voltage Level
X= Immaterial
Z= High Impedance
AO_0 = Previous AO before H-to-L transition of ALE
BO_0 = Previous BO before H-to-L transition of BLE

FUNCTIONAL DESCRIPTION

The SCAN18373T consists of two sets of nine D-type latches with Tri-State standard outputs. When the Latch Enable (ALE or BLE) input is HIGH, data on the inputs ($AI_{(0–8)}$ or $BI_{(0–8)}$) enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its input changes. When Latch Enable is LOW, the latches store the information that was present on the inputs a set-up time preceding the HIGH-to-LOW transition of the Latch Enable. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{AOE_1}$ or $\overline{BOE_1}$) input. When Output Enable is LOW, the standard outputs are in the 2-state mode. When Output Enable is HIGH, the standard outputs are in the high impedance mode, but this does not interfere with entering new data into the latches.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Block Diagrams

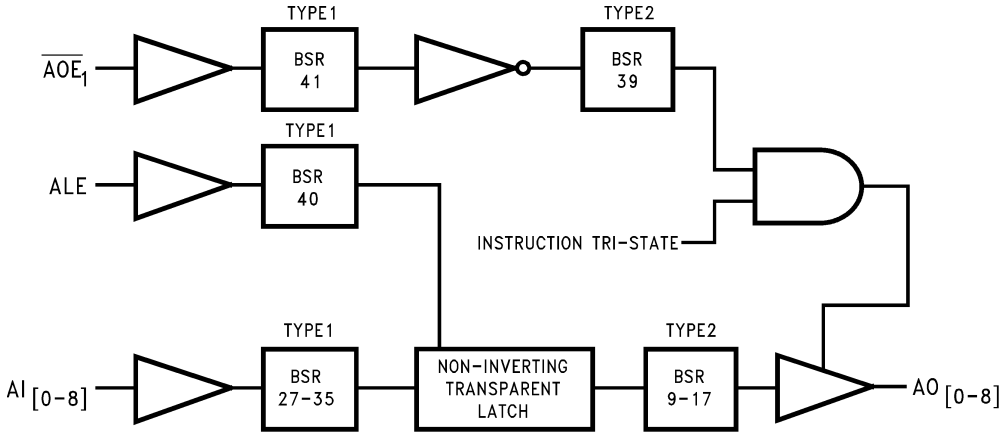


Figure 1. Byte-A

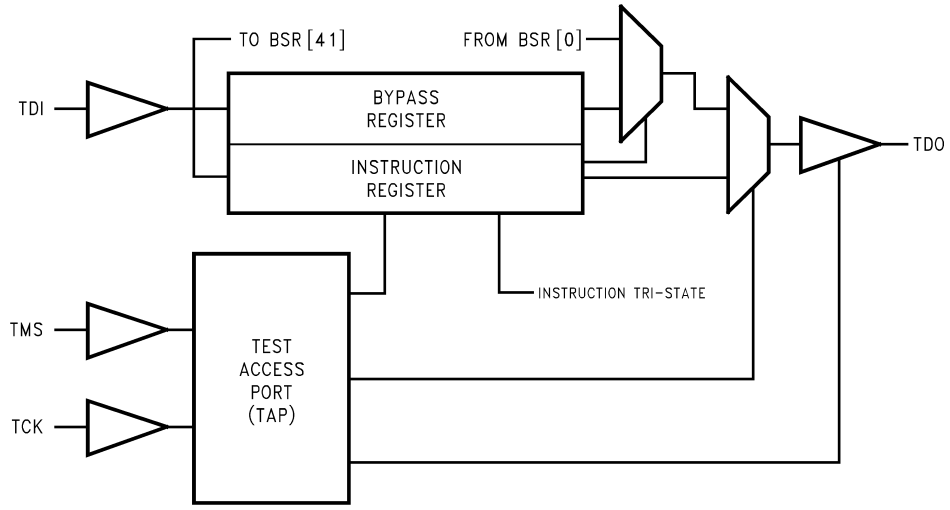
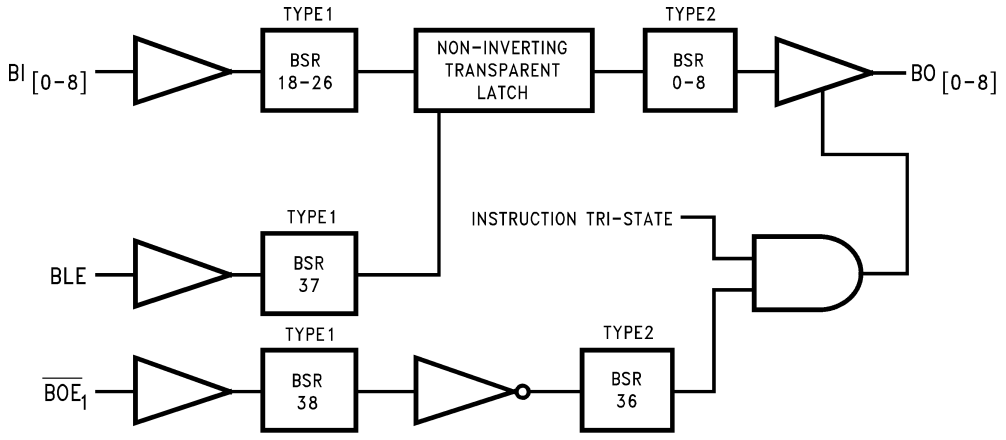


Figure 2. Tap Controller



BSR stands for Boundary Scan Register.

Figure 3. Byte-B

Description of Boundary-Scan Circuitry

The scan cells used in the BOUNDARY-SCAN register are one of the following two types depending upon their location. Scan cell TYPE1 is intended to solely observe system data, while TYPE2 has the additional ability to control system data. (See IEEE Standard 1149.1 for a further description of scan cell TYPE1 and for a further description of scan cell TYPE2.)

Scan cell TYPE1 is located on each system input pin while scan cell TYPE2 is located at each system output pin as well as at each of the two internal active-high output enable signals. AOE controls the activity of the A-outputs while BOE controls the activity of the B-outputs. Each will activate their respective outputs by loading a logic high.

The BYPASS register is a single bit shift register stage identical to scan cell TYPE1. It captures a fixed logic low.

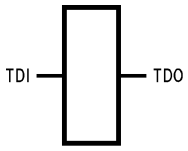


Figure 4. Bypass Register Scan Chain Definition Logic 0

The INSTRUCTION register is an eight-bit register which captures the value 00111101.

The two least significant bits of this captured value (01) are required by IEEE Std 1149.1. The upper six bits are unique to the SCAN18373T device. SCAN CMOS Test Access Logic devices do not include the IEEE 1149.1 optional identification register. Therefore, this unique captured value can be used as a “pseudo ID” code to confirm that the correct device is placed in the appropriate location in the boundary scan chain.

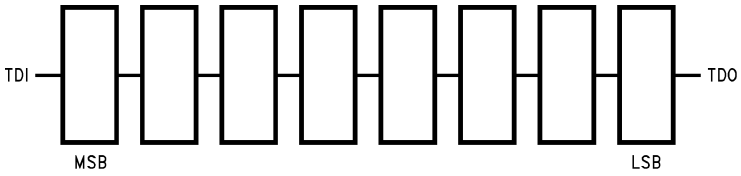


Figure 5. Instruction Register Scan Chain Definition

MSB → LSB

Instruction Code	Instruction
00000000	EXTEST
10000001	SAMPLE/PRELOAD
10000010	CLAMP
00000011	HIGHZ
All Others	BYPASS

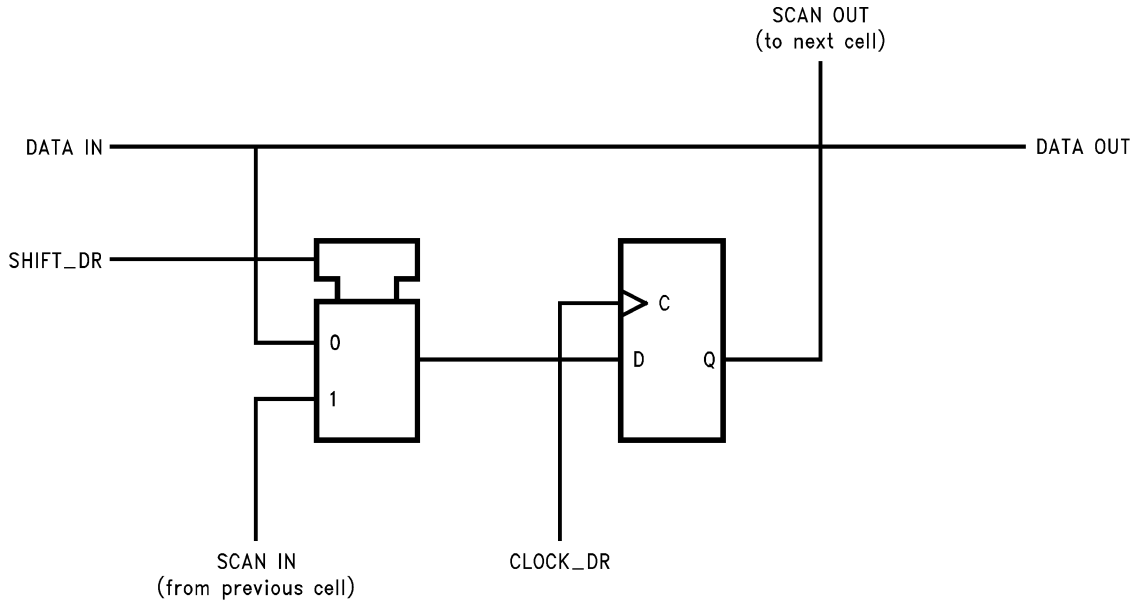


Figure 6. Scan Cell TYPE1

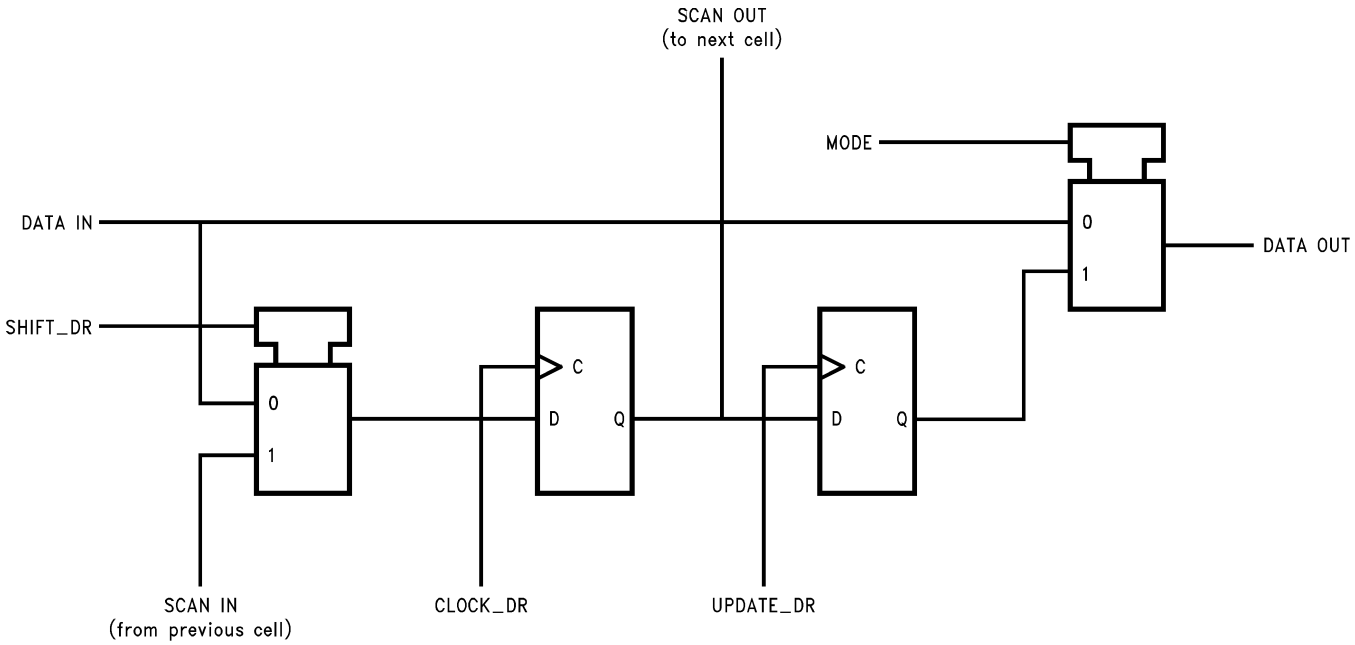


Figure 7. Scan Cell TYPE2

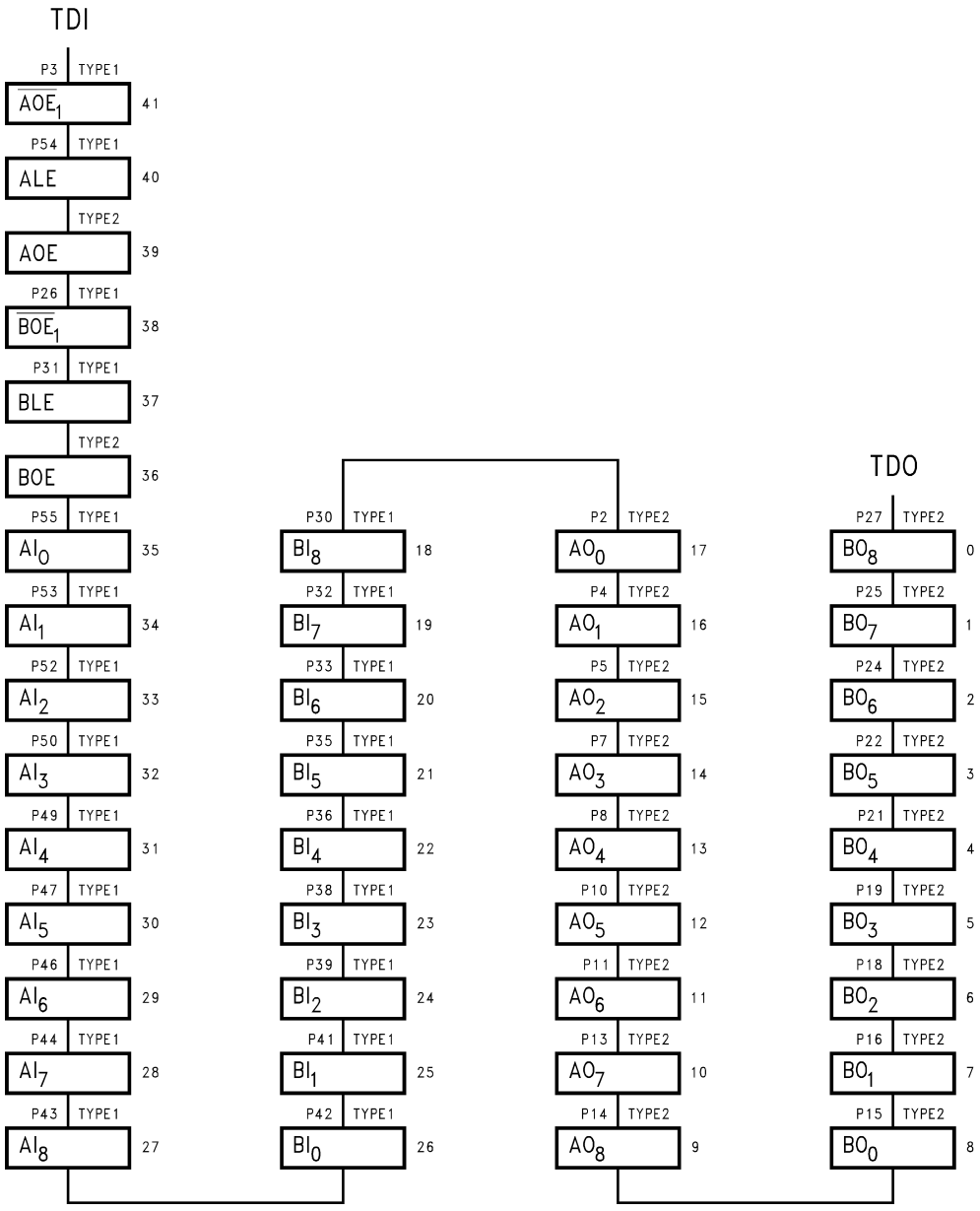


Figure 8. Boundary-Scan Register Scan Chain Definition (42 Bits in Length)

Boundary-Scan Register Definition Index

Bit No.	Pin Name	Pin No.	Pin Type	Scan Cell Type	
41	$\overline{AOE_1}$	3	Input	TYPE1	Control Signals
40	ACP	54	Input	TYPE1	
39	AOE		Internal	TYPE2	
38	$\overline{BOE_1}$	26	Input	TYPE1	
37	BCP	31	Input	TYPE1	
36	BOE		Internal	TYPE2	
35	AI_0	55	Input	TYPE1	A–in
34	AI_1	53	Input	TYPE1	
33	AI_2	52	Input	TYPE1	
32	AI_3	50	Input	TYPE1	
31	AI_4	49	Input	TYPE1	
30	AI_5	47	Input	TYPE1	
29	AI_6	46	Input	TYPE1	
28	AI_7	44	Input	TYPE1	
27	AI_8	43	Input	TYPE1	
26	BI_0	42	Input	TYPE1	B–in
25	BI_1	41	Input	TYPE1	
24	BI_2	39	Input	TYPE1	
23	BI_3	38	Input	TYPE1	
22	BI_4	36	Input	TYPE1	
21	BI_5	35	Input	TYPE1	
20	BI_6	33	Input	TYPE1	
19	BI_7	32	Input	TYPE1	
18	BI_8	30	Input	TYPE1	
17	AO_0	2	Output	TYPE2	A–out
16	AO_1	4	Output	TYPE2	
15	AO_2	5	Output	TYPE2	
14	AO_3	7	Output	TYPE2	
13	AO_4	8	Output	TYPE2	
12	AO_5	10	Output	TYPE2	
11	AO_6	11	Output	TYPE2	
10	AO_7	13	Output	TYPE2	
9	AO_8	14	Output	TYPE2	
8	BO_0	15	Output	TYPE2	B–out
7	BO_1	16	Output	TYPE2	
6	BO_2	18	Output	TYPE2	
5	BO_3	19	Output	TYPE2	
4	BO_4	21	Output	TYPE2	
3	BO_5	22	Output	TYPE2	
2	BO_6	24	Output	TYPE2	
1	BO_7	25	Output	TYPE2	
0	BO_8	27	Output	TYPE2	

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)(2)

Supply Voltage (V_{CC})		−0.5V to +7.0V
DC Input Diode Current (I_{IK})	V_I = −0.5V	−20 mA
	V_I = V_{CC} + 0.5V	+20 mA
DC Output Diode Current (I_{OK})	V_O = −0.5V	−20 mA
	V_O = V_{CC} +0.5V	+20 mA
DC Output Voltage (V_O)		−0.5V to V_{CC} + 0.5V
DC Output Source/Sink Current (I_O)		±70 mA
DC V_{CC} or Ground Current	Per Output Pin	±70 mA
Junction Temperature	Cerpack	+175°C
Storage Temperature		−65°C to +150°C
ESD (Min)		2000V

(1) Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Texas Instruments does not recommend operation of SCAN circuits outside databook specifications.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage (V_{CC})	SCAN Products	4.5V to 5.5V
Input Voltage (V_I)		0V to V_{CC}
Output Voltage (V_O)		0V to V_{CC}
Operating Temperature (T_A)	Military	−55°C to +125°C
Minimum Input Edge Rate dV/dt	V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC ELECTRICAL CHARACTERISTICS

All outputs loaded; thresholds associated with output under test.

Symbol	Parameter	V_{CC} (V)	Military T_A = −55°C to +125°C Specified Limits	Units	Conditions
V_{IH}	Minimum High Input Voltage	4.5 5.5	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Input Voltage	4.5 5.5	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Output Voltage	4.5 5.5	3.15 4.15	V	I_{OUT} = −50 µA
		4.5 5.5	2.4 2.4	V	V_{IN} = V_{IL} or V_{IH} I_{OH} = −24 mA
V_{OL}	Maximum Low Output Voltage	4.5 5.5	0.1 0.1	V	I_{OUT} = 50 µA
		4.5 5.5	0.55 0.55	V	V_{IN} = V_{IL} or V_{IH} I_{OL} = 48 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	µA	V_I = V_{CC}, GND
I_{IN} TDI, TMS	Maximum Input Leakage	5.5	3.7 −385	µA µA	V_I = V_{CC} V_I = GND
	Minimum Input Leakage	5.5	−160	µA	V_I = GND

DC ELECTRICAL CHARACTERISTICS (continued)

All outputs loaded; thresholds associated with output under test.

Symbol	Parameter	V_{CC} (V)	Military T_A = −55°C to +125°C Specified Limits	Units	Conditions
I_{OLD} I_{OHD}	Minimum Dynamic Output Current(1)	5.5	63 −27	mA mA	V_{OLD} = 0.8V Max V_{OHD} = 2.0V Min
I_{OZ}	Maximum Output Leakage Current	5.5	±10.0	µA	V_I (OE) = V_{IL}, V_{IH}
I_{OS}	Output Short Circuit Current	5.5	−100	mA Min	V_O = 0V
I_{CC}	Maximum Quiescent Supply Current	5.5	168	µA	V_O = Open TDI, TMS = V_{CC}
		5.5	930	µA	V_O = Open TDI, TMS = GND
I_{CCt}	Maximum I_{CC} per Input	5.5	2.0	mA	V_I = V_{CC} − 2.1V
		5.5	2.15	mA	V_I = V_{CC} − 2.1V TDI/TMS Pin, Test One with the Other Floating

(1) Maximum test duration 2.0 ms, one output loaded at a time.

NOISE SPECIFICATIONS

Symbol	Parameter	V_{CC} (V)	Military T_A = −55°C to +125°C Specified Limits	Units	Fig. No.
V_{OLP}	Maximum High Output Noise(1)(2)	5.0	0.8	V	
V_{OLV}	Minimum Low Output Noise(1)(2)	5.0	-0.8	V	

(1) Maximum number of outputs that can switch simultaneously is n. (n−1) outputs are switched LOW and one output held LOW.
(2) Maximum number of outputs that can switch simultaneously is n. (n−1) outputs are switched HIGH and one output held HIGH.

AC ELECTRICAL CHARACTERISTICS

Normal Operation

Symbol	Parameter	V_{CC} (V)(1)	Military T_A=−55°C to +125°C, C_L = 50 pF		Units	Fig. No.
			Min	Max		
t_{PLH}, t_{PHL}	Propagation Delay, D to Q	5.0	2.5 2.5	11.0 11.5	ns	
t_{PLH}, t_{PHL}	Propagation Delay, LE to Q	5.0	2.5 2.5	12.0 13.0	ns	
t_{PLZ}, t_{PHZ}	Disable Time	5.0	1.5 1.5	11.0 10.3	ns	
t_{PZL}, t_{PZH}	Enable Time	5.0	2.0 2.0	13.5 11.5	ns	

(1) Voltage Range 5.0 is 5.0V ±0.5V.

AC OPERATING REQUIREMENTS

Normal Operation

Symbol	Parameter	V_{CC} (V)(1)	Military	Units	Fig. No.
			T_A = −55°C to +125°C C_L = 50 pF		
			Specified Minimum		
t_S	Setup Time, H or L Data to LE	5.0	3.0	ns	
t_H	Hold Time, H or L LE to Data	5.0	1.5	ns	
t_W	LE Pulse Width	5.0	5.0	ns	

(1) Voltage Range 5.0 is 5.0V ±0.5V.

AC ELECTRICAL CHARACTERISTICS

Scan Test Operation

Symbol	Parameter	V_{CC} (V)(1)	Military		Units	Fig. No.
			T_A=−55°C to +125°C C_L = 50 pF			
			Min	Max		
t_{PLH}, t_{PHL}	Propagation Delay TCK to TDO	5.0	3.5 3.5	15.8 15.8	ns	
t_{PLZ}, t_{PHZ}	Disable Time TCK to TDO	5.0	2.5 2.5	12.8 12.8	ns	
t_{PZL}, t_{PZH}	Enable Time TCK to TDO	5.0	3.0 3.0	16.7 16.7	ns	
t_{PLH}, t_{PHL}	Propagation Delay TCK to Data Out during Update-DR State	5.0	5.0 5.0	21.7 21.7	ns	
t_{PLH}, t_{PHL}	Propagation Delay TCK to Data Out during Update-IR State	5.0	5.0 5.0	22.0 22.0	ns	
t_{PLH}, t_{PHL}	Propagation Delay TCK to Data Out during Test Logic Reset State	5.0	5.5 5.5	23.0 23.0	ns	
t_{PLZ}, t_{PHZ}	Propagation Delay TCK to Data Out during Update-DR State	5.0	4.0 4.0	19.6 19.6	ns	
t_{PLZ}, t_{PHZ}	Propagation Delay TCK to Data Out during Update-IR State	5.0	5.0 5.0	22.4 22.4	ns	
t_{PLZ}, t_{PHZ}	Propagation Delay TCK to Data Out during Test Logic Reset State	5.0	5.0 5.0	23.3 23.3	ns	
t_{PZL}, t_{PZH}	Propagation Delay TCK to Data Out during Update-DR State	5.0	5.0 5.0	22.6 22.6	ns	
t_{PZL}, t_{PZH}	Propagation Delay TCK to Data Out during Update-IR State	5.0	6.5 6.5	26.2 26.2	ns	
t_{PZL}, t_{PZH}	Propagation Delay TCK to Data Out during Test Logic Reset State	5.0	7.0 7.0	27.4 27.4	ns	

(1) Voltage Range 5.0 is 5.0V ±0.5V. All propagation delays involving TCK are measured from the falling edge of TCK.

AC OPERATING REQUIREMENTS

Scan Test Operation

Symbol	Parameter	V_{CC} (V)(1)	Military T_A = −55°C to +125°C, C_L = 50 pF Specified Minimum	Units	Fig. No.
t_S	Setup Time, Data to TCK(2)	5.0	3.0	ns	
t_H	Hold Time, TCK to Data(2)	5.0	5.5	ns	
t_S	Setup Time, H or L $\overline{AOE}_1$, $\overline{BOE}_1$ to TCK(3)	5.0	3.0	ns	
t_H	Hold Time, H or L TCK to $\overline{AOE}_1$, $\overline{BOE}_1$(3)	5.0	4.5	ns	
t_S	Setup Time, H or L Internal AOE, BOE, to TCK(4)	5.0	3.0	ns	
t_H	Hold Time, H or L TCK to Internal AOE, BOE(4)	5.0	3.0	ns	
t_S	Setup Time ALE, BLE(5) to TCK	5.0	3.0	ns	
t_H	Hold Time TCK to ALE, BLE(5)	5.0	4.0	ns	
t_S	Setup Time, H or L TMS to TCK	5.0	8.0	ns	
t_H	Hold Time, H or L TCK to TMS	5.0	2.0	ns	
t_S	Setup Time, H or L TDI to TCK	5.0	4.0	ns	
t_H	Hold Time, H or L TCK to TDI	5.0	4.5	ns	
t_W	Pulse Width TCK H Pulse Width TCK L	5.0	12.0 5.0	ns	
f_{max}	Maximum TCK Clock Frequency	5.0	25	MHz	
T_{pu}	Wait Time, Power Up to TCK	5.0	100	ns	
T_{dn}	Power Down Delay	0.0	100	ms	

(1) Voltage Range 5.0 is 5.0V ±0.5V. All Input Timing Delays involving TCK are measured from the rising edge of TCK.
(2) This delay represents the timing relationship between the data input and TCK at the associated scan cells numbered 0-8, 9-17, 18-26 and 27-35.
(3) Timing pertains to BSR 38 and 41 only.
(4) This delay represents the timing relationship between AOE/BOE and TCK for scan cells 36 and 39 only.
(5) Timing pertains to BSR 37 and 40 only.

CAPACITANCE

Symbol	Parameter	Max	Units	Conditions
C_{IN}	Input Pin Capacitance	5.0	pF	V_{CC} = 5.0V
C_{OUT}	Output Pin Capacitance	15.0	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	35.0	pF	V_{CC} = 5.0V

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	12

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