DS90CR286A/DS90CR286AQ/DS90CR216A +3.3V Rising Edge Data Strobe LVDS Receiver 28-Bit Channel Link - 66 MHz, +3.3V Rising Edge Strobe LVDS Receiver 21-Bit Channel Link - 66 MHz

Check for Samples: DS90CR216A, DS90CR286A

FEATURES

- **20 to 66 MHz Shift Clock Support**
- **50% Duty Cycle on Receiver Output Clock**
- **Best–in–Class Set & Hold Times on RxOUTPUTs**
- **Rx Power Consumption <270 mW (typ) @66MHz Worst Case**
- **Rx Power-down Mode <200µW (max)**
- **ESD Rating >7 kV (HBM), >700V (EIAJ)**
- **PLL Requires No External Components**
- **Compatible with TIA/EIA-644 LVDS Standard**
- **Low Profile 56-Lead or 48-Lead TSSOP Package**
- **Operating Temperature: −40°C to +85°C**
- **Automotive Q grade available - AEC-Q100 Grade 3 Qualified**

DESCRIPTION

The DS90CR286A receiver converts the four LVDS data streams (Up to 1.848 Gbps throughput or 231 Megabytes/sec bandwidth) back into parallel 28 bits of CMOS/TTL data. Also available is the DS90CR216A that converts the three LVDS data streams (Up to 1.386 Gbps throughput or 173 Megabytes/sec bandwidth) back into parallel 21 bits of CMOS/TTL data. Both Receivers' outputs are Rising edge strobe.

Both devices are offered in TSSOP packages.

The DS90CR286A / DS90CR216A devices are enhanced over prior generation receivers and provided a wider data valid time on the receiver output.

This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

BLOCK DIAGRAM

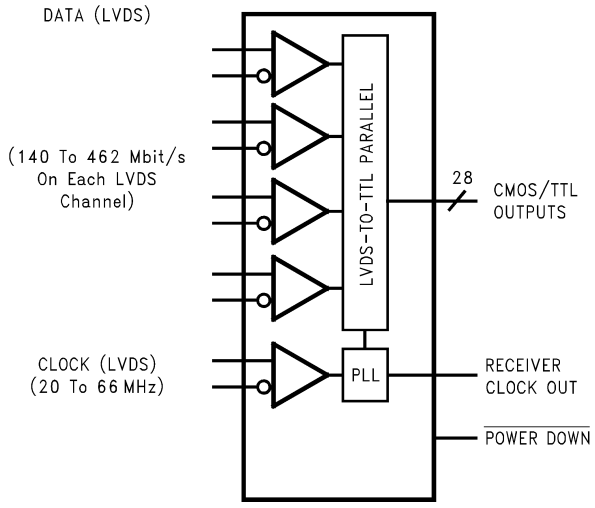


Figure 1. DS90CR286A
See Package Number DGG-56 (TSSOP)

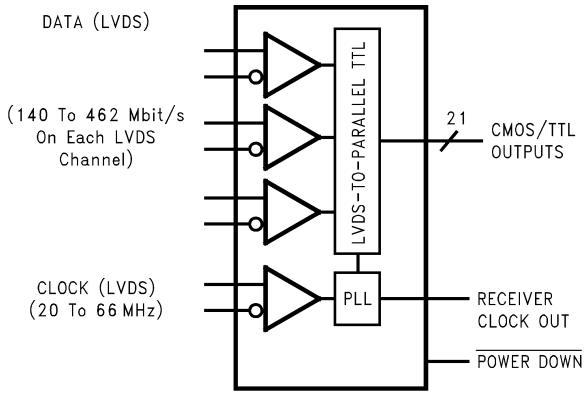


Figure 2. DS90CR216A
See Package Number DGG-48 (TSSOP)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

Absolute Maximum Ratings(1)(2)

Supply Voltage (V_{CC})			−0.3V to +4V
CMOS/TTL Output Voltage			−0.3V to (V_{CC} + 0.3V)
LVDS Receiver Input Voltage			−0.3V to (V_{CC} + 0.3V)
Junction Temperature			+150°C
Storage Temperature			−65°C to +150°C
Lead Temperature (Soldering, 4 sec)			+260°C
Maximum Package Power Dissipation Capacity @ 25°C	DGG0056A (TSSOP) Package	DS90CR286AMTD	1.61 W
	DGG0048A (TSSOP) Package	DS90CR216AMTD	1.89 W
Package Derating		DS90CR286AMTD	12.4 mW/°C above +25°C
		DS90CR216AMTD	15 mW/°C above +25°C
ESD Rating		(HBM, 1.5 kΩ, 100 pF)	> 7 kV
		(EIAJ, 0Ω, 200 pF)	> 700V

(1) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(2) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. "Electrical Characteristics" specify conditions for device operation.

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−40	+25	+85	°C
Receiver Input Range	0		2.4	V
Supply Noise Voltage (V_{CC})			100	mV_{PP}

Electrical Characteristics(1)(2)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS/TTL DC SPECIFICATIONS (For PowerDown Pin)						
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA		−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = 0.4V, 2.5V or V_{CC}		+1.8	+10	µA
		V_{IN} = GND	−10	0		µA
CMOS/TTL DC SPECIFICATIONS						
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA	2.7	3.3		V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA		0.06	0.3	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V		−60	−120	mA
LVDS RECEIVER DC SPECIFICATIONS						
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V			+100	mV
V_{TL}	Differential Input Low Threshold		−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V, V_{CC} = 3.6V			±10	µA
		V_{IN} = 0V, V_{CC} = 3.6V			±10	µA

(1) Typical values are given for V_{CC} = 3.3V and T_A = +25C.
(2) Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

Electrical Characteristics[1][2] (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
RECEIVER SUPPLY CURRENT							
ICCRW	Receiver Supply Current Worst Case	C_L = 8 pF, Worst Case Pattern, DS90CR286A (Figure 3 Figure 4), T_A=−10°C to +70°C	f = 33 MHz		49	65	mA
			f = 37.5 MHz		53	70	mA
			f = 66 MHz		81	105	mA
ICCRW	Receiver Supply Current Worst Case	C_L = 8 pF, Worst Case Pattern, DS90CR286A (Figure 3 Figure 4), T_A=−40°C to +85°C	f = 40 MHz		53	70	mA
			f = 66 MHz		81	105	mA
ICCRW	Receiver Supply Current Worst Case	C_L = 8 pF, Worst Case Pattern, DS90CR216A (Figure 3 Figure 4), T_A=−10°C to +70°C	f = 33 MHz		49	55	mA
			f = 37.5 MHz		53	60	mA
			f = 66 MHz		78	90	mA
ICCRW	Receiver Supply Current Worst Case	C_L = 8 pF, Worst Case Pattern, DS90CR216A (Figure 3 Figure 4), T_A=−40°C to +85°C	f = 40 MHz		53	60	mA
			f = 66 MHz		78	90	mA
ICCRZ	Receiver Supply Current Power Down	$\overline{\text{Power Down}}$ = Low Receiver Outputs Stay Low during Power Down Mode			10	55	µA

Receiver Switching Characteristics[1]

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
CLHT	CMOS/TTL Low-to-High Transition Time (Figure 4)			2	5	ns
CHLT	CMOS/TTL High-to-Low Transition Time (Figure 4)			1.8	5	ns
RSPos0	Receiver Input Strobe Position for Bit 0 (Figure 11, Figure 12)	f = 40 MHz	1.0	1.4	2.15	ns
RSPos1	Receiver Input Strobe Position for Bit 1		4.5	5.0	5.8	ns
RSPos2	Receiver Input Strobe Position for Bit 2		8.1	8.5	9.15	ns
RSPos3	Receiver Input Strobe Position for Bit 3		11.6	11.9	12.6	ns
RSPos4	Receiver Input Strobe Position for Bit 4		15.1	15.6	16.3	ns
RSPos5	Receiver Input Strobe Position for Bit 5		18.8	19.2	19.9	ns
RSPos6	Receiver Input Strobe Position for Bit 6		22.5	22.9	23.6	ns
RSPos0	Receiver Input Strobe Position for Bit 0 (Figure 11, Figure 12)	f = 66 MHz	0.7	1.1	1.4	ns
RSPos1	Receiver Input Strobe Position for Bit 1		2.9	3.3	3.6	ns
RSPos2	Receiver Input Strobe Position for Bit 2		5.1	5.5	5.8	ns
RSPos3	Receiver Input Strobe Position for Bit 3		7.3	7.7	8.0	ns
RSPos4	Receiver Input Strobe Position for Bit 4		9.5	9.9	10.2	ns
RSPos5	Receiver Input Strobe Position for Bit 5		11.7	12.1	12.4	ns
RSPos6	Receiver Input Strobe Position for Bit 6		13.9	14.3	14.6	ns
RSKM	RxIN Skew Margin[2] (Figure 13)	f = 40 MHz	490			ps
		f = 66 MHz	400			ps
RCOP	RxCLK OUT Period (Figure 5)		15	T	50	ns
RCOH	RxCLK OUT High Time (Figure 5)	f = 40 MHz	10.0	12.2		ns
RCOL	RxCLK OUT Low Time (Figure 5)		10.0	11.0		ns
RSRC	RxOUT Setup to RxCLK OUT (Figure 5)		6.5	11.6		ns
RHRC	RxOUT Hold to RxCLK OUT (Figure 5)		6.0	11.6		ns

(1) Typical values are given for V_{CC} = 3.3V and T_A = +25C.
(2) Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account the transmitter pulse positions (min and max) and the receiver input setup and hold time (internal data sampling window - RSPos). This margin allows for LVDS interconnect skew, inter-symbol interference (both dependent on type/length of cable), and clock jitter (less than 250 ps).

Receiver Switching Characteristics[1] (continued)

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
RCOH	RxCLK OUT High Time (Figure 5)	f = 66 MHz	5.0	7.6		ns
RCOL	RxCLK OUT Low Time (Figure 5)		5.0	6.3		ns
RSRC	RxOUT Setup to RxCLK OUT (Figure 5)		4.5	7.3		ns
RHRC	RxOUT Hold to RxCLK OUT (Figure 5)		4.0	6.3		ns
RCCD	RxCLK IN to RxCLK OUT Delay @ 25°C, V_{CC} = 3.3V[3] (Figure 6)		3.5	5.0	7.5	ns
RPLLS	Receiver Phase Lock Loop Set (Figure 7)				10	ms
RPDD	Receiver Power Down Delay (Figure 10)				1	µs

(3) Total latency for the channel link chipset is a function of clock period and gate delays through the transmitter (TCCD) and receiver (RCCD). The total latency for the 215/285 transmitter and 216A/286A receiver is: (T + TCCD) + (2*T + RCCD), where T = Clock period.

AC Timing Diagrams

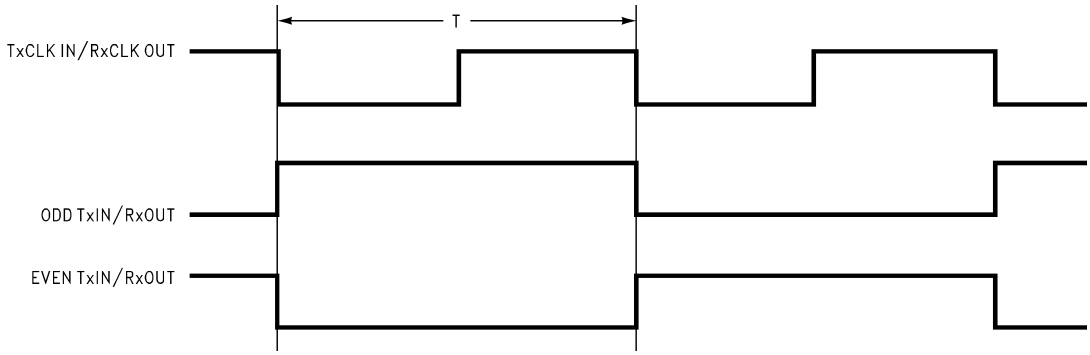


Figure 3. "Worst Case" Test Pattern

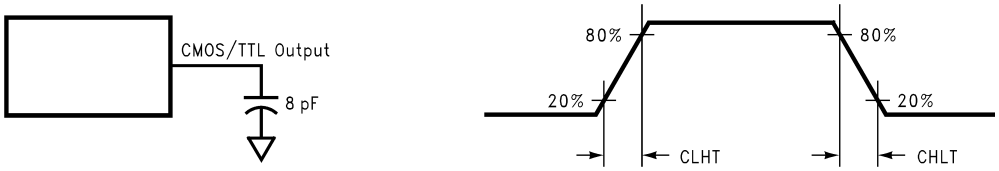


Figure 4. DS90CR286A/DS90CR216A (Receiver) CMOS/TTL Output Load and Transition Times

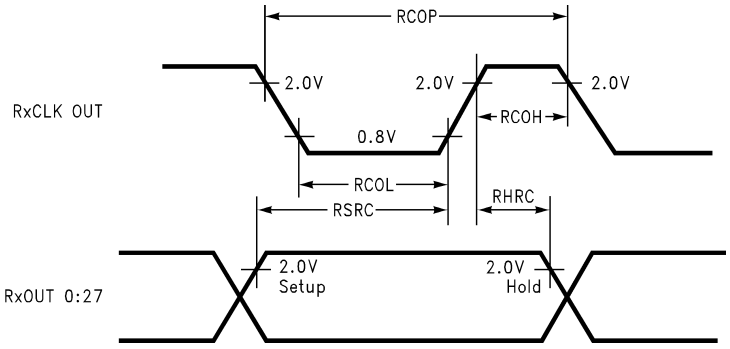


Figure 5. DS90CR286A/DS90CR216A (Receiver) Setup/Hold and High/Low Times

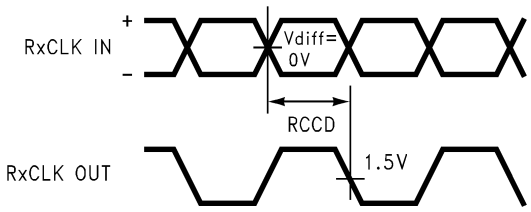


Figure 6. DS90CR286A/DS90CR216A (Receiver) Clock In to Clock Out Delay

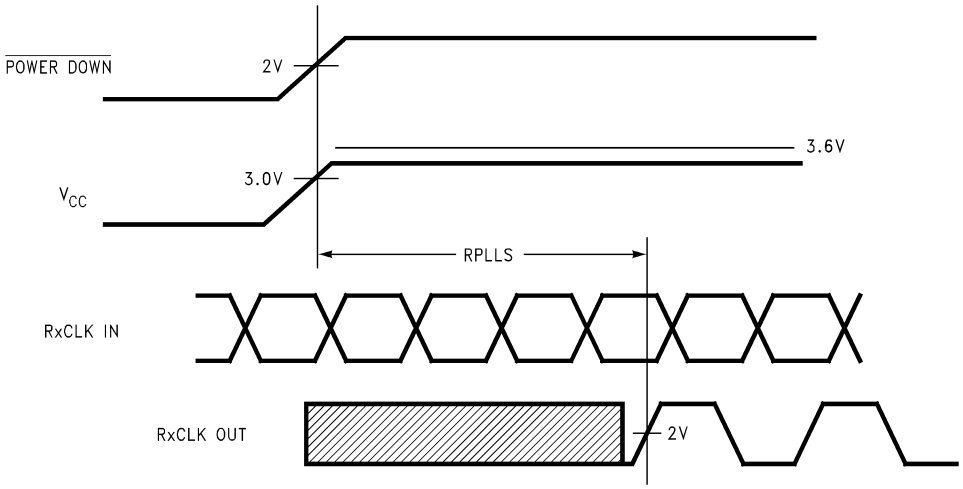


Figure 7. DS90CR286A/DS90CR216A (Receiver) Phase Lock Loop Set Time

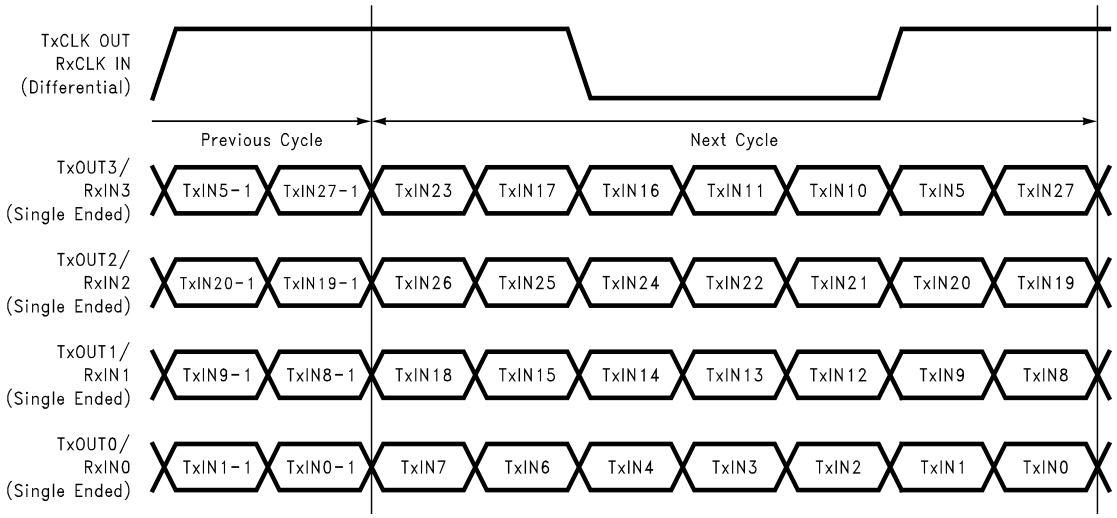


Figure 8. 28 Parallel TTL Data Inputs Mapped to LVDS Outputs - DS90CR286A

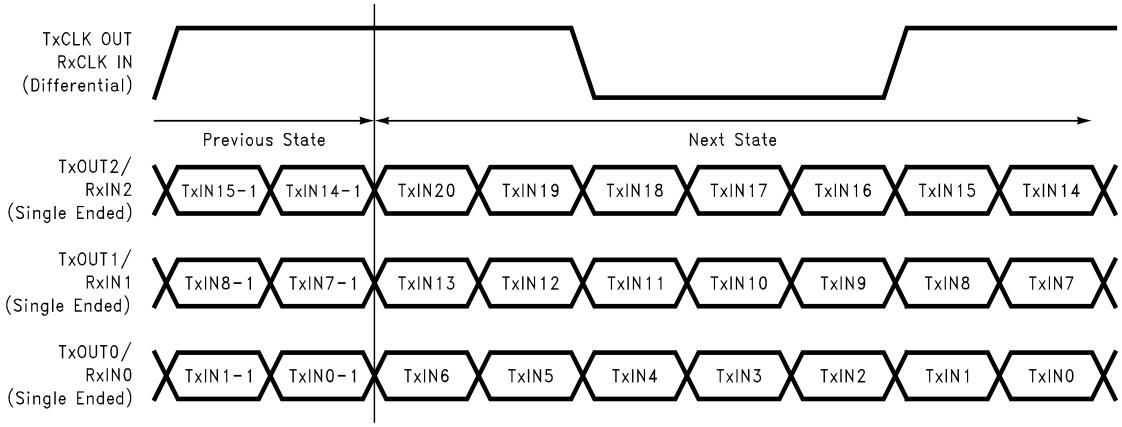


Figure 9. 21 Parallel TTL Data Inputs Mapped to LVDS Outputs - DS90CR216A

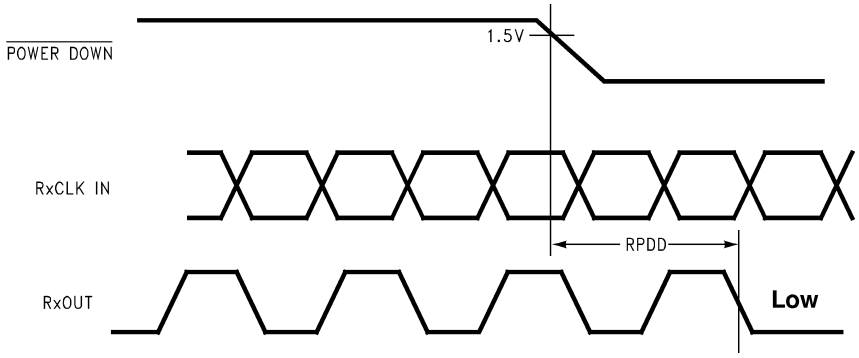


Figure 10. DS90CR286A/DS90CR216A (Receiver) Power Down Delay

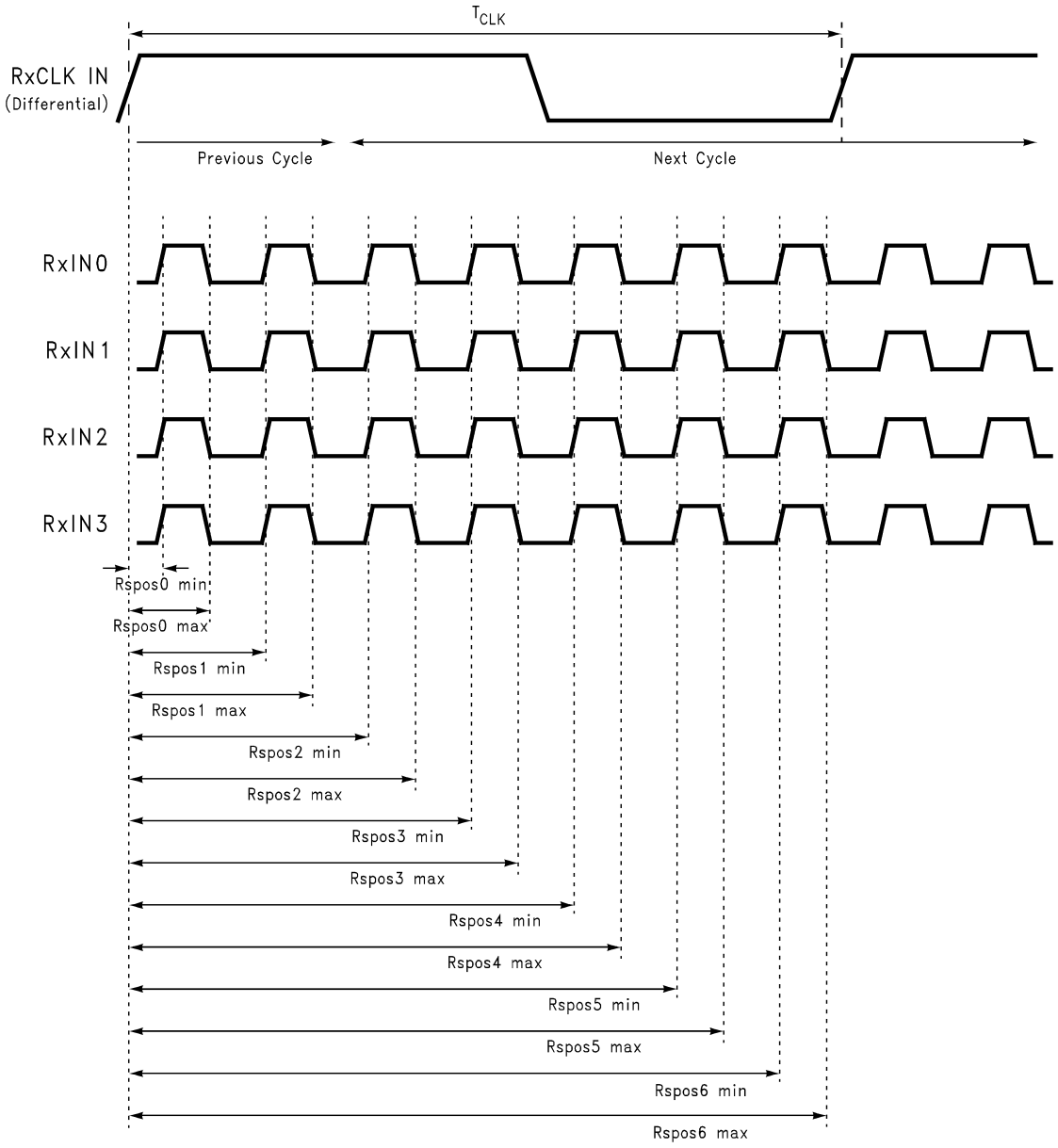


Figure 11. DS90CR286A (Receiver) LVDS Input Strobe Position

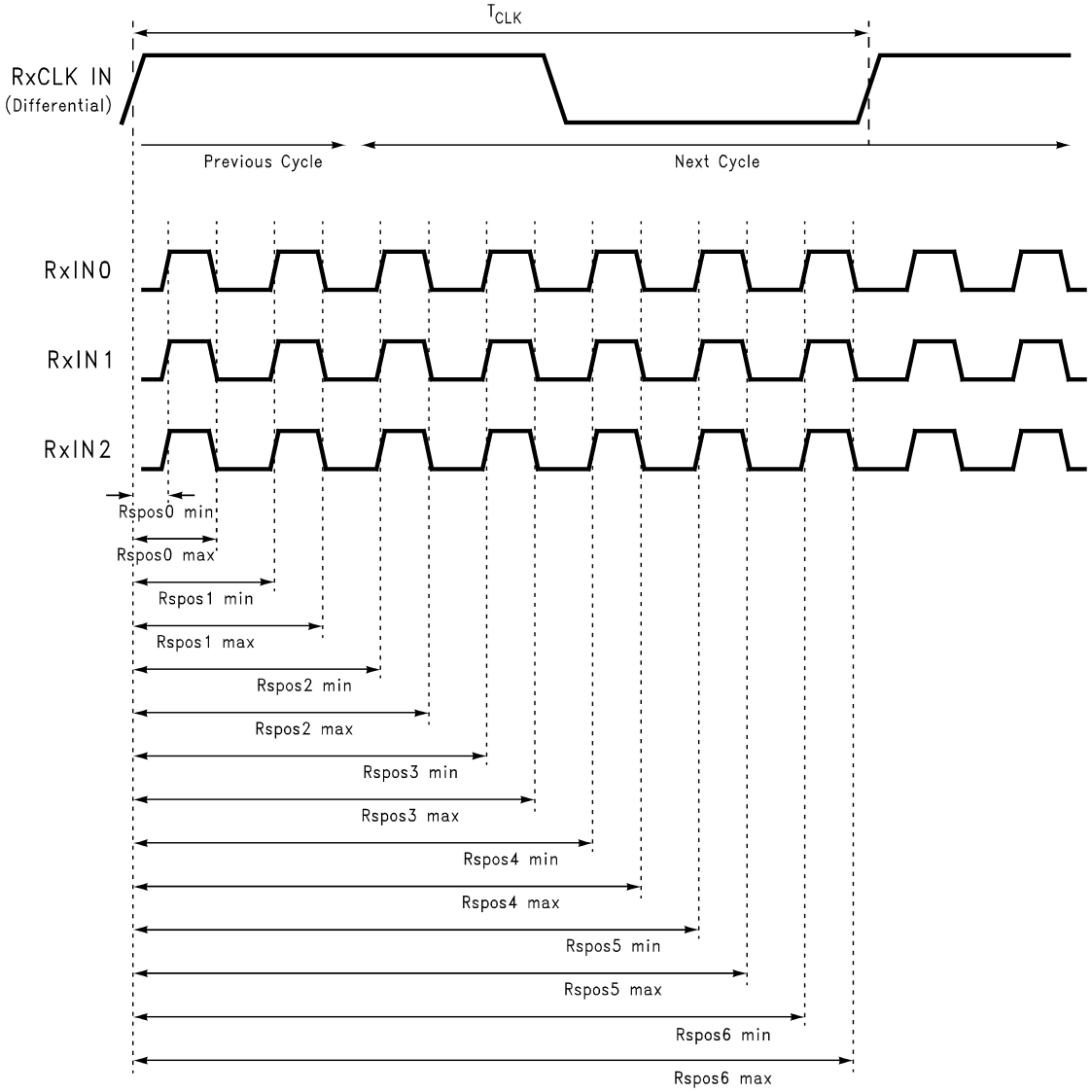
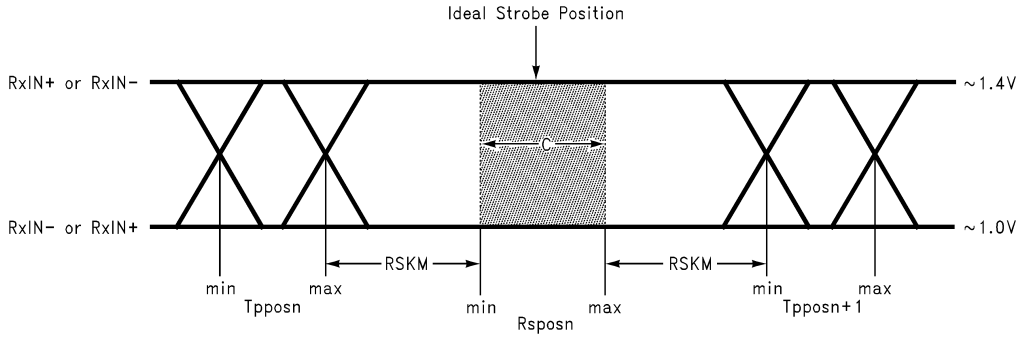


Figure 12. DS90CR216A (Receiver) LVDS Input Strobe Position



C—Setup and Hold Time (Internal data sampling window) defined by Rspos (receiver input strobe position) min and max

Tppos—Transmitter output pulse position (min and max)

RSKM = Cable Skew (type, length) + Source Clock Jitter (cycle to cycle)(1) + ISI (Inter-symbol interference)(2)

Cable Skew—typically 10 ps–40 ps per foot, media dependent

(1) Cycle-to-cycle jitter is less than TBD ps at 66 MHz.

(2) ISI is dependent on interconnect length; may be zero.

Figure 13. Receiver LVDS Input Skew Margin

DS90CR286A PIN DESCRIPTIONS — DGG0056A Package — 28-Bit Channel Link Receiver

Pin Name	I/O	No.	Description
RxIN+	I	4	Positive LVDS differential data inputs.
RxIN−	I	4	Negative LVDS differential data inputs.
RxOUT	O	28	TTL level data outputs.
RxCLK IN+	I	1	Positive LVDS differential clock input.
RxCLK IN−	I	1	Negative LVDS differential clock input.
RxCLK OUT	O	1	TTL level clock output. The rising edge acts as data strobe.
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. When asserted (low input) the receiver outputs are low.
V_{CC}	I	4	Power supply pins for TTL outputs.
GND	I	5	Ground pins for TTL outputs.
PLL V_{CC}	I	1	Power supply for PLL.
PLL GND	I	2	Ground pin for PLL.
LVDS V_{CC}	I	1	Power supply pin for LVDS inputs.
LVDS GND	I	3	Ground pins for LVDS inputs.

DS90CR216A PIN DESCRIPTIONS — DGG0048A Package — 21-Bit Channel Link Receiver

Pin Name	I/O	No.	Description
RxIN+	I	3	Positive LVDS differential data inputs.(1)
RxIN−	I	3	Negative LVDS differential data inputs.(1)
RxOUT	O	21	TTL level data outputs.
RxCLK IN+	I	1	Positive LVDS differential clock input.
RxCLK IN−	I	1	Negative LVDS differential clock input.
RxCLK OUT	O	1	TTL level clock output. The rising edge acts as data strobe.
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. When asserted (low input) the receiver outputs are low.
V_{CC}	I	4	Power supply pins for TTL outputs.
GND	I	5	Ground pins for TTL outputs.
PLL V_{CC}	I	1	Power supply for PLL.

(1) These receivers have input failsafe bias circuitry to guarantee a stable receiver output for floating or terminated receiver inputs. Under these conditions receiver inputs will be in a HIGH state. If a clock signal is present, outputs will all be HIGH; if the clock input is also floating/terminated outputs will remain in the last valid state. A floating/terminated clock input will result in a LOW clock output.

DS90CR216A PIN DESCRIPTIONS — DGG0048A Package — 21-Bit Channel Link Receiver (continued)

Pin Name	I/O	No.	Description
PLL GND	I	2	Ground pin for PLL.
LVDS V_{CC}	I	1	Power supply pin for LVDS inputs.
LVDS GND	I	3	Ground pins for LVDS inputs.

Pin Diagram for TSSOP Packages

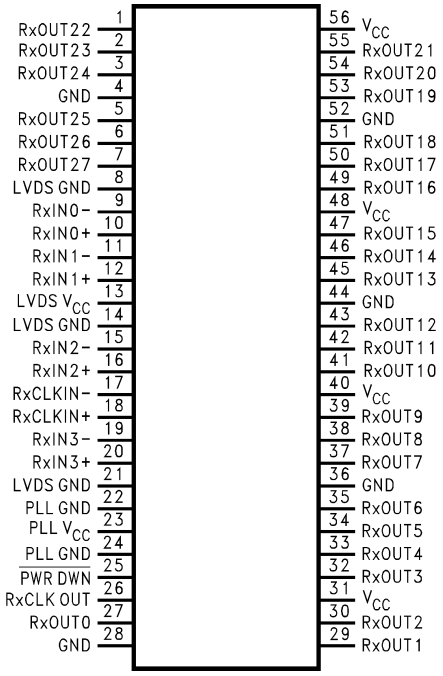


Figure 14. DS90CR286AMTD

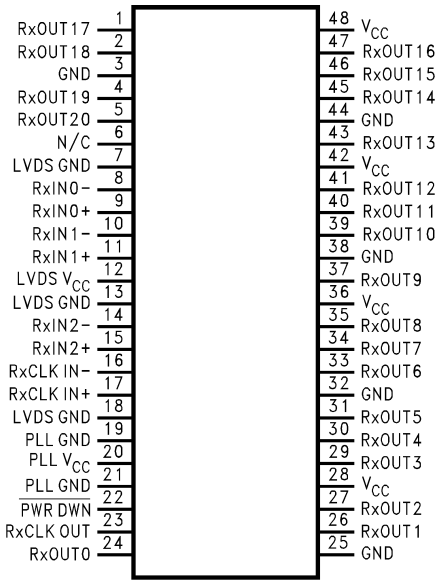


Figure 15. DS90CR216AMTD

REVISION HISTORY

Changes from Revision E (February 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DS90CR216AMTD	ACTIVE	TSSOP	DGG	48	38	TBD	Call TI	Call TI	-40 to 85	DS90CR216AMTD >B	Samples
DS90CR216AMTD/NOPB	ACTIVE	TSSOP	DGG	48	38	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	DS90CR216AMTD >B	Samples
DS90CR216AMTDX/NOPB	ACTIVE	TSSOP	DGG	48	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	DS90CR216AMTD >B	Samples
DS90CR286AMTD	ACTIVE	TSSOP	DGG	56	34	TBD	Call TI	Call TI	-40 to 85	DS90CR286AMTD >B	Samples
DS90CR286AMTD/NOPB	ACTIVE	TSSOP	DGG	56	34	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	DS90CR286AMTD >B	Samples
DS90CR286AMTDX/NOPB	ACTIVE	TSSOP	DGG	56	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	DS90CR286AMTD >B	Samples
DS90CR286AQMT/NOPB	ACTIVE	TSSOP	DGG	56	34	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	DS90CR286AQ MT	Samples
DS90CR286AQMTX/NOPB	ACTIVE	TSSOP	DGG	56	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	DS90CR286AQ MT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

OTHER QUALIFIED VERSIONS OF DS90CR286A, DS90CR286A-Q1 :

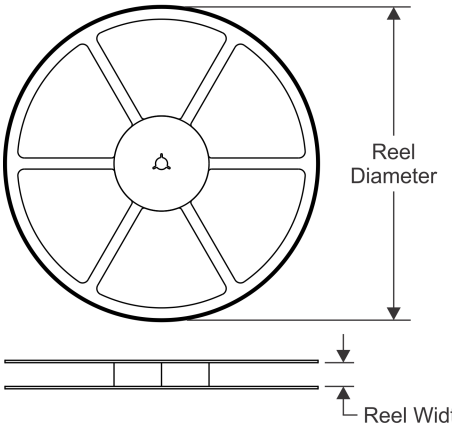
- Catalog: DS90CR286A
- Automotive: DS90CR286A-Q1

NOTE: Qualified Version Definitions:

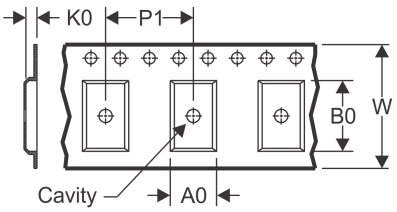
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

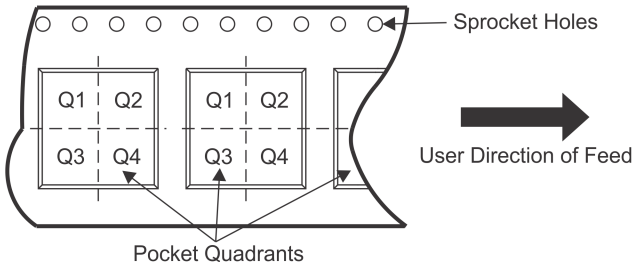


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

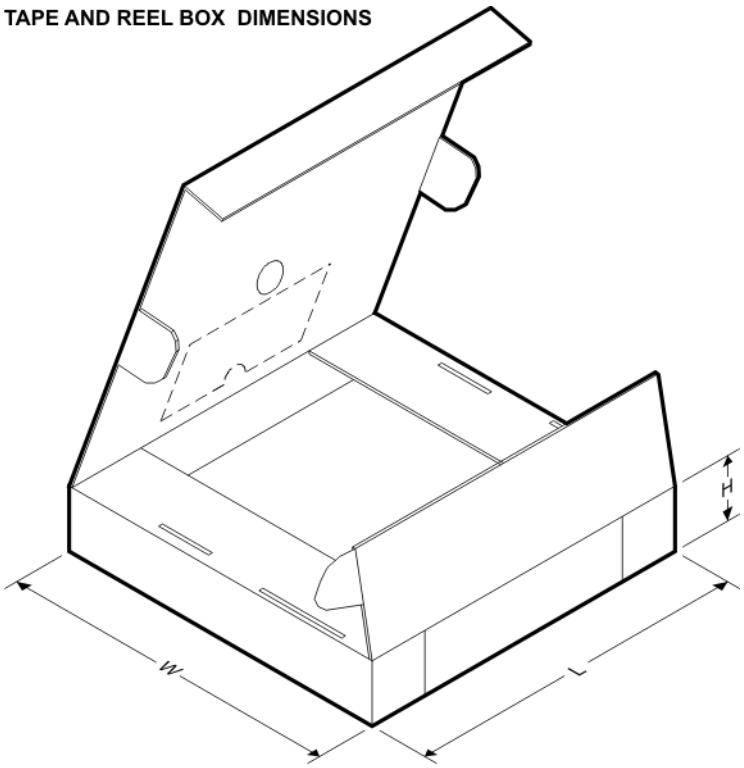
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90CR216AMTDX/NOPB	TSSOP	DGG	48	1000	330.0	24.4	8.6	13.2	1.6	12.0	24.0	Q1
DS90CR286AMTDX/NOPB	TSSOP	DGG	56	1000	330.0	24.4	8.6	14.5	1.8	12.0	24.0	Q1
DS90CR286AQMTX/NOPB	TSSOP	DGG	56	1000	330.0	24.4	8.6	14.5	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

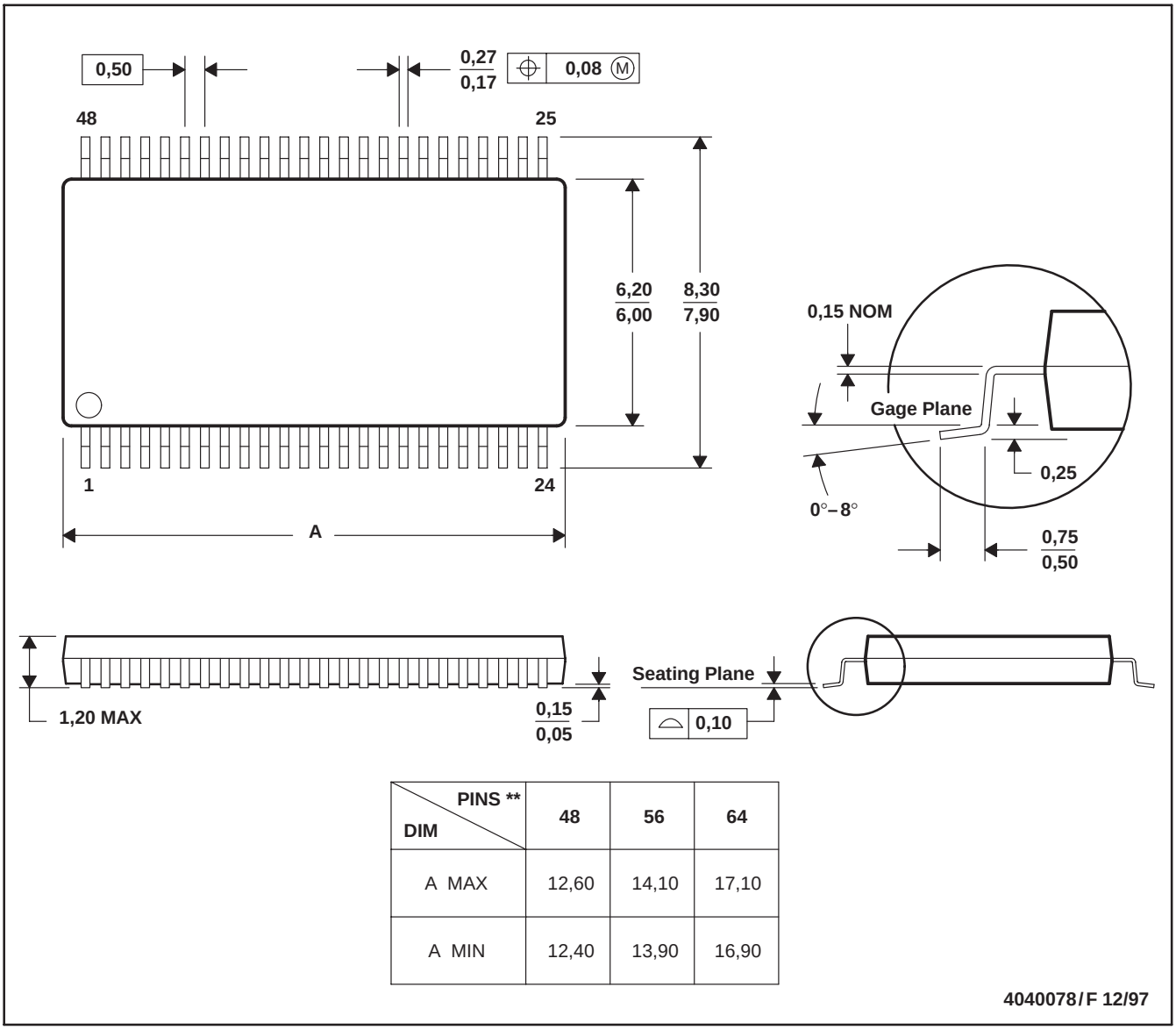


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90CR216AMTDX/NOPB	TSSOP	DGG	48	1000	367.0	367.0	45.0
DS90CR286AMTDX/NOPB	TSSOP	DGG	56	1000	367.0	367.0	45.0
DS90CR286AQMTX/NOPB	TSSOP	DGG	56	1000	367.0	367.0	45.0

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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