DP83861

DP83861 EN Gig PHYTER 10/100/1000 Ethernet Physical Layer

Literature Number: SNLS069D

National Semiconductor

PRELIMINARY

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DP83861VQM-3 EN Gig PHYTER® 10/100/1000 Ethernet Physical Layer

General Description

The DP83861 is a full featured Physical Layer transceiver with integrated PMD sublayers to support 10BASE-T, 100BASE-TX and 1000BASE-T Ethernet protocols.

The DP83861 uses state of the art 0.18 µm, 1.8 V/3.3 V CMOS technology, fabricated at National Semiconductor's South Portland Maine facility.

The DP83861 is designed for easy implementation of 10/100/1000 Mb/s Ethernet LANs. It interfaces directly to Twisted Pair media via an external transformer. This device interfaces directly to the MAC layer through the IEEE 802.3u Standard Media Independent Interface (MII) or the IEEE 802.3z Gigabit Media Independent Interface (GMII).

Applications

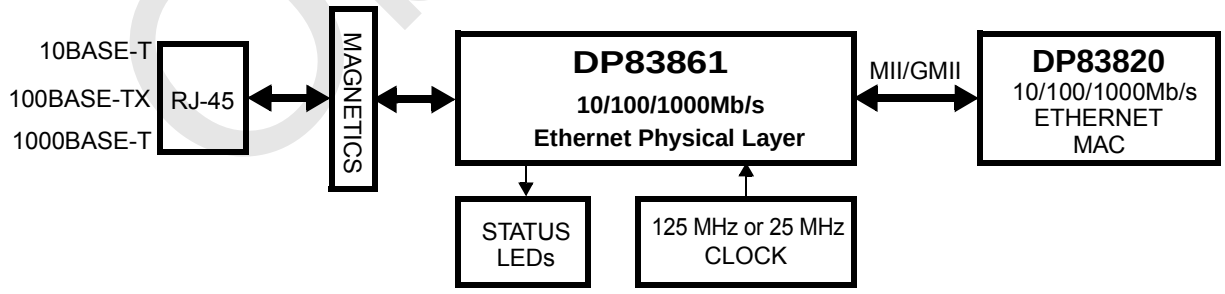
The DP83861 fits applications in:

- 10/100/1000 Mb/s capable node cards
- Switches with 10/100/1000 Mb/s capable ports
- High speed uplink ports (backbone)

Features

- 100BASE-TX and 1000BASE-T compliant
- Fully compliant to IEEE 802.3u 100BASE-TX and IEEE 802.3z/ab 1000BASE-T specifications. Fully integrated and fully compliant ANSI X3.T12 PMD physical sublayer that includes adaptive equalization and Baseline Wander compensation
- 10BASE-T compatible
- IEEE 802.3u Auto-Negotiation and Parallel Detection
  - Fully Auto-Negotiates between 1000 Mb/s, 100 Mb/s, and 10 Mb/s Full Duplex and Half Duplex devices
- Interoperates with frst generation 1000BASE-T Physical layer transceivers
- 3.3V MAC interfaces:
  - IEEE 802.3u MII
  - IEEE 802.3z GMII
- LED support: Link, Speed, Activity, Collision, TX and RX
- Supports 125 MHz or 25 MHz reference clock
- Requires only one 1.8 V and one 3.3 V supply
- Supports MDIX at 10, 100, and 1000 Mb/s
- Supports JTAG (IEEE1149.1)
- Dissipates 1 watt in 10/100 Mb/s mode
- Programmable Interrupts
- 208-pin PQFP package

System Diagram



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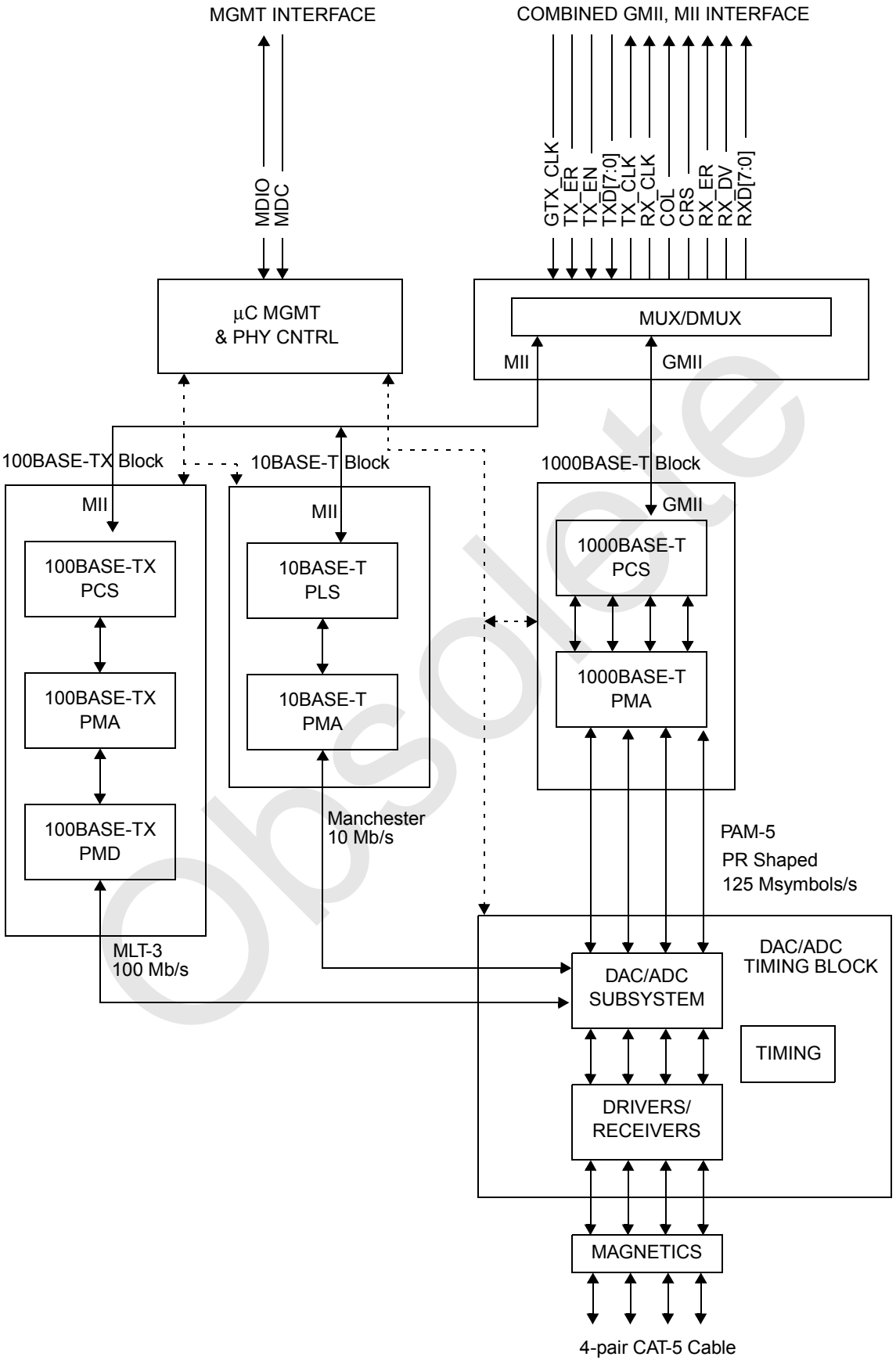
Block Diagram



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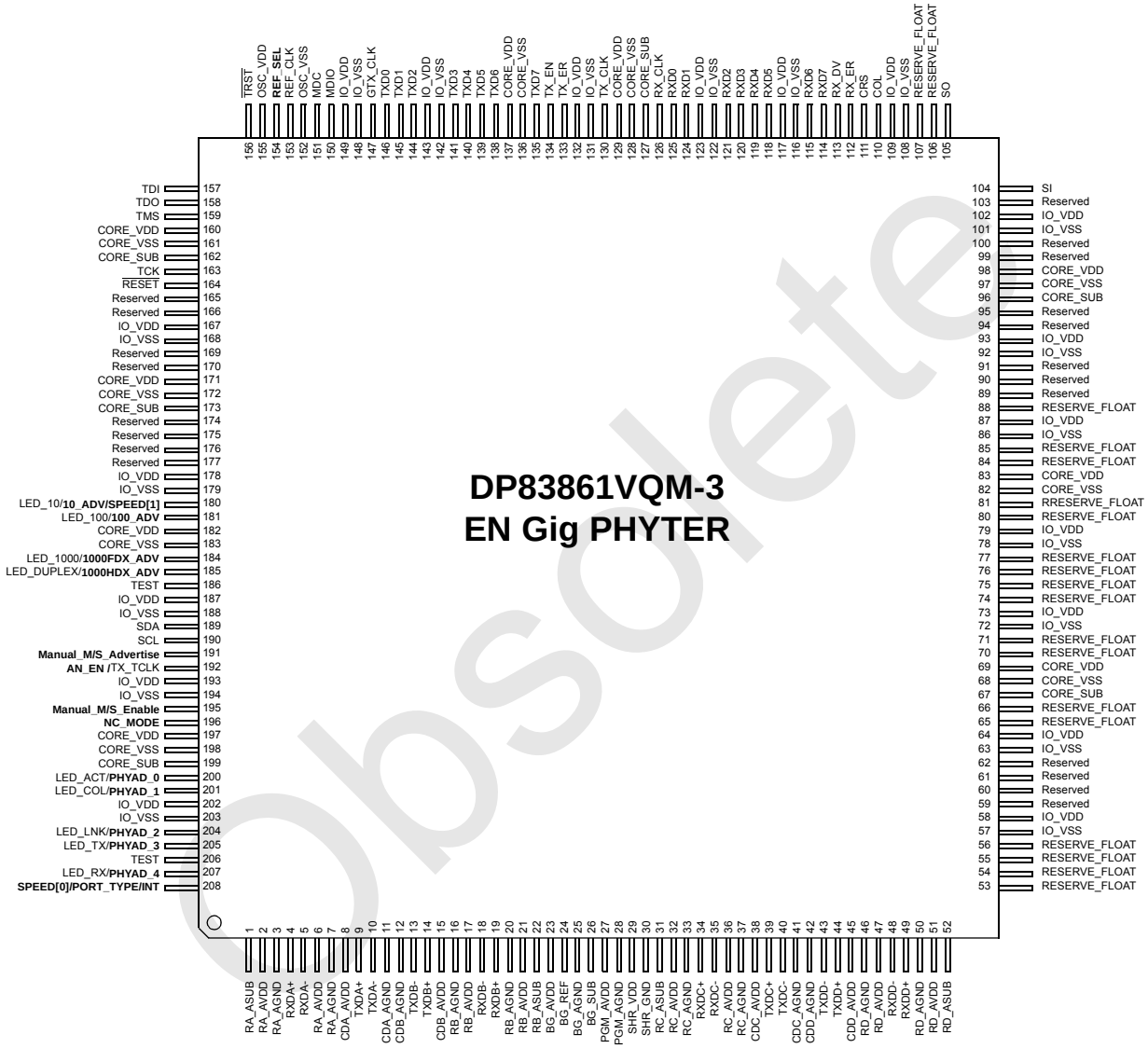
PQFP (VQM) Pin Layout



Bold pin names are strap options (e.g. **AN_EN)**

208 Lead Plastic Quad Flat Pack
Order Number DP83861VQM-3
NS Package VQM-208A

1.0 Pin Descriptions

The DP83861 pins are classified into the following interface categories (each is described in the sections that follow):

— MAC Interface
— TP Interface
— JTAG Interface
— E^2PROM Interface
— Clock Interface
— LED Interface
— Device Configuration / Strapping Options
— Reset
— Power and Ground Pins
— Special Connect Pins

Note: Strapping pin option (**BOLD**) (e.g. **AN_EN**)

Type: I	Inputs
Type: O	Output
Type: O_Z	Tristate Output
Type: I/O_Z	Tristate Input_Output
Type: S	Strapping Pin
Type: PU	Pull-up
Type: PD	Pull-down

1.1 MAC Interface

Signal Name	Type	Pin #	Description
MDC	I	151	**MANAGEMENT DATA CLOCK:** Synchronous clock to the MDIO management data input/output serial interface which may be asynchronous to transmit and receive clocks. The maximum clock rate is 2.5 MHz with no minimum clock rate.
MDIO	I/O	150	**MANAGEMENT DATA I/O:** Bi-directional management instruction/data signal that may be sourced by the station management entity or the PHY. This pin requires a 1.5 kΩ pullup resistor.
CRS	O	111	**CARRIER SENSE:** Asserted high to indicate the presence of carrier due to receive or transmit activity in Half Duplex mode. This signal is not defined (LOW) for 1000BASE-T Full Duplex mode. For 1000BASE-T, 100BASE-TX and 10BASE-T Full Duplex operation CRS is asserted only for receive activity.
COL	O	110	**COLLISION DETECT:** Asserted high to indicate detection of a collision condition (assertion of CRS due to simultaneous transmit and receive activity) in Half Duplex modes. This signal is not synchronous to either MII clock (GTX_CLK, TX_CLK or RX_CLK). This signal is not defined (LOW) for Full Duplex modes.
TX_CLK	O	130	**TRANSMIT CLOCK (10 Mb/s and 100 Mb/s):** Continuous clock signal generated from REF_CLK and driven by the PHY during 10Mb/s and 100 Mb/s operation. It is used on the MII to clock all MII Transmit (data, error) signals into the PHY. The Transmit Clock frequency is constant and the frequency is 2.5 MHz for 10Mb/s mode and 25 MHz for 100Mb/s mode. TX_CLK should not be confused with the TX_TCLK signal.
TXD0 TXD1 TXD2 TXD3 TXD4 TXD5 TXD6 TXD7	I	146 145 144 141 140 139 138 135	**TRANSMIT DATA:** These signals carry 4B data nibbles (TXD[3:0]) during 10 Mb/s and 100 Mb/s MII mode and 8-bit data (TXD[7:0]) in 1000 Mb/s GMII mode. They are synchronous to the Transmit Clocks (TX_CLK, GTX_CLK. Transmit data is input enabled by TX_EN for all modes all sourced by the controller.
TX_EN	I	134	**TRANSMIT ENABLE:** Active high input driven by the MAC requesting transmission of the data present on the TXD lines (nibble data for 10 Mb/s and 100 Mb/s mode and 8-bit data for 1000 Mb/s GMII mode.)
GTX_CLK	I	147	**GMII-TRANSMIT CLOCK:** This continuous clock signal is sourced from the upper level MAC to the PHY. Nominal frequency of 125 MHz, derived in the MAC from its 125 MHz reference clock.

Signal Name	Type	Pin #	Description
TX_ER	I	133	**TRANSMIT ERROR:** Active high input during 100 Mb/s nibble mode or 1000 Mb/s GMII mode. This forces the PHY to transmit invalid symbols. The TX_ER signal must be synchronous to the Transmit Clocks (TX_CLK and GTX_CLK). In 4B nibble mode, assertion of Transmit Error by the controller causes the PHY to issue invalid symbols followed by Halt (H) symbols until deassertion occurs. In 1000 Mb/s GMII mode, assertion causes the PHY to emit one or more code-groups that are not valid data or delimiter set in the transmitted frame.
RX_CLK	O	126	**RECEIVE CLOCK:** Provides the recovered receive clocks for different modes of operation: 2.5 MHz nibble clock in 10 Mb/s MII mode. 25 MHz nibble clock in 100 Mb/s MII mode. 125 MHz byte clock in 1000 Mb/s GMII mode.
RXD0 RXD1 RXD2 RXD3 RXD4 RXD5 RXD6 RXD7	O	125 124 121 120 119 118 115 114	**RECEIVE DATA:** These signals carry 4-bit data nibbles (RXD[3:0]) during 10Mb/s and 100 Mb/s MII mode and 8-bit data (RXD[7:0]) in 1000 Mb/s GMII mode. They are synchronous to the Receive Clock (RX_CLK). Receive data is driven by the PHY to the controller, and is strobed by Receive Data Valid (RX_DV) which is also sourced by the PHY.
RX_ER	O	112	**RECEIVE ERROR:** In 100 Mb/s MII mode and 1000 Mb/s GMII mode this active high output indicates that the PHY has detected a Receive Error. The RX_ER signal must be synchronous with the Receive Clock (RX_CLK).
RX_DV	O	113	**RECEIVE DATA VALID:** Asserted high to indicate that valid data is present on the corresponding RXD[3:0] for 10 Mb/s or 100 Mb/s MII mode and RXD[7:0] in 1000 Mb/s GMII mode.

1.2 TP Interface

Signal Name	Type	PIn #	Description
TXDA+ TXDA- TXDB- TXDB+ TXDC+ TXDC- TXDD- TXDD+	O	9 10 13 14 39 40 43 44	**TRANSMIT DATA:** The TP Interface connects the DP83861 to the CAT-5 cable through a single common magnetics transformer. The Transmit (TXD) and Receive (RXD) Twisted Pair pins carry bit-serial data at 125 MHz baud rate. These differential outputs are configurable to either 100 BASE-T, 100BASE-TX or 1000BASE-T signalling: 10BASE-T: Transmission of MANCHESTER encoded signals. The 10BASE-T signal does not meet IEEE transmit output voltages. See Section 7.1. 100BASE-TX: Transmission of 3-level MLT-3 data. 1000BASE-T: Transmission of 17-level PAM-5 with PR-shaping data. The DP83861 will automatically configure the common driver outputs for the proper signal type as a result of either forced configuration or Auto-Negotiation. **NOTE:** During 10/100 Mb/s operation only TXDA+ and TXDA- or TXDB+ and TXDB- are active. (See DP83861 Datasheet for automatic crossover configuration.)

Signal Name	Type	PIn #	Description
RXDA+ RXDA- RXDB- RXDB+ RXDC+ RXDC- RXDD- RXDD+	I	4 5 18 19 34 35 48 49	**RECEIVE DATA:** Differential receive signals. **NOTE:** During 10/100 Mb/s operation only RXDB+ and RXDB- or RXDA+ and RXDA- are active (See DP83861 Datasheet for automatic crossover configuration.)

1.3 JTAG Interface

Signal Name	Type	PIn #	Description
$\overline{\text{TRST}}$	I	156	**TEST RESET:** IEEE 1149.1 Test Reset pin, active low reset provides for asynchronous reset of the Tap Controller. This reset has no effect on the device registers. This pin should be tied low during regular chip operation.
TDI	I	157	**TEST DATA INPUT:** IEEE 1149.1 Test Data Input pin, test data is scanned into the device via TDI. This pin should be tied low during regular chip operation.
TDO	O	158	**TEST DATA OUTPUT:** IEEE 1149.1 Test Data Output pin, the most recent test results are scanned out of the device via TDO. This pin can be left floating if not used.
TMS	I	159	**TEST MODE SELECT:** IEEE 1149.1 Test Mode Select pin, the TMS pin sequences the Tap Controller (16-state FSM) to select the desired test instruction. This pin should be tied low during regular chip operation.
TCK	I	163	**TEST CLK:** IEEE 1149.1 Test Clock input, primary clock source for all test logic input and output controlled by the testing entity. This pin should be tied low during regular chip operation.

1.4 E^{2}PROM Interface

Signal Name	Type	Pin #	Description
SDA	I/O, PU	189	**Serial Data:** See application note "DP83861 EN Gig PHYTER E^{2}PROM Usage Guide" on how to use this interface. This pin should be left floating if the E^{2}PROM interface is not used.
SCL	I/O, PD	190	**SERIAL CLOCK:** See application note "DP83861 EN Gig PHYTER E^{2}PROM Usage Guide" on how to use this interface. This pin should be left floating if the E^{2}PROM interface is not used.

1.5 Clock Interface

Signal Name	Type	Pin #	Description
REF_CLK	I	153	**CLOCK INPUT:** 125 MHz or 25 MHz (both require +/-50ppm tolerance and less than 200 ps of jitter) See Section 3.4.
REF_SEL	I	154	**Clock Select:** This pin enables the use of a 125 MHz clock source to REF_CLK when pulled directly or through a 2KΩ resistor to 3.3V supply. When pulled low directly or through a 2KΩ resistor to ground enables a 25 MHz clock source. This pin should never be floated.

1.6 LED/Interrupt Interface

Signal Name	Type	Pin #	Description
LED_RX	I/O, S, PD	207	**RECEIVE ACTIVITY LED:** The Receive LED output indicates that the PHY is receiving.
LED_TX	I/O, S, PD	205	**TRANSMIT ACTIVITY LED:** The Transmit LED output indicates that the PHY is transmitting.
LED_LNK	I/O, S, PD	204	**GOOD LINK LED STATUS:** Indicates status for Good Link the criteria for good link are: 10BASE-T: Link is established by detecting Normal Link Pulses separated by 16 ms or by packet data received. 100BASE-T: Link is established as a result of an input receive amplitude compliant with TP-PMD specifications which will result in internal generation of Signal Detect. LED_LNK will assert after the internal Signal Detect has remained asserted for a minimum of 500 µs. LED_LNK will de-assert immediately following the de-assertion of the internal Signal Detect. 1000BASE-T: Link is established as a result of training, Auto-Negotiation completed, valid 1000BASE-T link established and reliable reception of signals transmitted from a remote PHY is established.
LED_DUPLEX	I/O, S, PD	185	**DUPLEX LED STATUS:** If the LED is on, it indicates Full Duplex mode of operation, else Half Duplex operation.
LED_COL	I/O, S, PD	201	**COLLISION LED STATUS:** Indicates that the PHY has detected a collision condition (simultaneous transmit and receive activity while in Half Duplex mode).
LED_ACT	I/O, S, PU	200	**TX/RX ACTIVITY LED STATUS:** Indicates either transmit or receive activity.
LED_10	I/O, S, PD	180	**10 Mb/s SPEED LED:** If LED is on, then the current speed of operation is 10 Mb/s. [1]
LED_100	I/O, S, PU	181	**100 Mb/s SPEED LED:** If LED is on, then the current speed of operation is 100 Mb/s. [1]
LED_1000	I/O, S, PU	184	**1000 Mb/s SPEED LED:** If LED is on, then the current speed of operation is 1000 Mb/s. [1]

INT	I/O, S, PD	208	**INTERRUPT:** Generates a interrupt upon PHY status changes. The interrupt function is enabled in the extended register set. This pin is not an Open Drain Output and can not be wired OR to other pins. **See Section 2.10**

1. Each of the Speed LEDs (LED_10, LED_100, LED_1000) is AND'ed with good link LEDs. They will only come on when the PHY has established good link at the speed indicated.

1.7 Device Configuration Interface

Signal Name	Type	Pin #	Description
AN_EN TX_TCLK	I/O, S, PU	192	**AUTO-NEGOTIATION ENABLE:** Input to set value of Auto-Negotiation Enable bit (register 0 bit-12). '1' Enables Auto-Negotiation '0' Disables Auto-Negotiation **TX_TCLK:** Output used to measure jitter during Test Mode 3 as described by IEEE 802.3ab specification. TX_TCLK should not be confused with the TX_CLK signal.
MANUAL_M/S_Enable	I/O, S, PD	195	**MANUAL MASTER/SLAVE ENABLE:** Input to set value of manual Master/Slave Configuration Enable bit (register 9 bit-12). The DP83861 still goes through the Auto-Negotiation process. '1' Enables manual Master/Slave Configuration '0' Disables manual Master/Slave Configuration
Manual M/S Advertise	I/O, S, PD	191	**Manual MASTER/ SLAVE CONFIGURATION VALUE:** Input to set value of Master/Slave Advertise bit (register 9 bit 11). DP83861 still goes through the Auto-Negotiation process. '1' Configures PHY to Master during Master/Slave negotiation '0' Configures PHY to Slave during Master/Slave negotiation. This bit is only used if the Manual_M/S_Configuration is enabled.
1000FDX_ADV	I, S, PU	184	**AUTO_NEG 1000 FDX ADVERTISE:** The value strapped during power/on reset determines the mode of operation advertised during Auto-Negotiation. '1' Advertises 1000 Mb/s Full Duplex capability '0' Does not advertise 1000 Mb/s Full Duplex capability
LED_DUPLEX **1000HDX_ADV**	I/O, S, PD	185	**DUPLEX MODE SELECT/ 1000 Mb/s HALF DUPLEX ADVERTISE:** This strap option has two functions depending on whether Auto-Negotiation is enabled or not: Auto-Negotiation disabled: '1' straps on Full Duplex mode of operation '0' straps on Half Duplex mode of operation. Auto-Negotiation enabled: '1' Advertises 1000 Mb/s Half Duplex capability '0' Does not advertise 1000 Mb/s Half Duplex capability.
100_ADV	I/O, S, PU	181	**100 Mb/s FULL/HALF DUPLEX ADVERTISE:** This strap option pin determines if 100 Mb/s Full/Half Duplex capability will be advertised during Auto-Negotiation. '1' Advertises both Full and Half Duplex capability '0' Advertises neither 100 Mb/s capability
10_ADV	I/O, S, PD	180	**10 Mb/s FULL/HALF DUPLEX ADVERTISE:** This strap option pin determines if 10 Mb/s Full/Half Duplex capability will be advertised during Auto-Negotiation. '1' Advertises both Full and Half Duplex capability '0' Advertises neither 10 Mb/s capability

Signal Name	Type	Pin #	Description
NC MODE	I/O, S, PD	196	**NON-COMPLIANT MODE:** This mode allows interoperability with certain NON-IEEE compliant 1000BASE-T transceivers. See Section 8.17. '1' Enables Non-Compliant mode '0' Disables Non-Compliant mode
SPEED[1]/10_ADV **SPEED[0]/PORT_TYPE**	I/O, S,PD I/O, S, PD	180 208	**SPEED SELECT:** These strap option pins have 2 different functions depending on whether Auto-Negotiation is enabled or not. SPEED[1:0] Auto-Negotiation disabled (Forced Speed mode:) 00 10BASE-T 01 100BASE-TX 10 1000BASE-T 11 Reserved SPEED[1] Auto-Negotiation enabled (Advertised capability:) '1' Advertises 10 Mb/s capability (Both Full Duplex and Half Duplex.) '0' Does not advertise 10 Mb/s capability. (Neither Full Duplex nor Half Duplex is advertised.) SPEED[0]/PORT_TYPE Auto-Negotiation enabled (Advertised capability:) '1' Advertises Multi-Node (e.g. Repeater or Switch) '0' Advertises Single-Node mode. (e.g. NIC)
PHYAD_0 **PHYAD_1** **PHYAD_2** **PHYAD_3** **PHYAD_4**	I/O, S, PU I/O, S, PD I/O, S, PD I/O, S, PD I/O, S, PD	200 201 204 205 207	**PHY ADDRESS [4:0]:** The DP83861 provides five PHY address-sensing pins for multiple applications. The five PHYAD[4:0] are registered as inputs at reset with PHYAD_4 being the MSB of the 5-bit PHY address. The PHY address can only be set through the strapping option.

1.8 Reset

Signal Name	Type	Pin #	Description
$\overline{\text{RESET}}$	I	164	**RESET:** The active low $\overline{\text{RESET}}$ input allows for hard-reset, soft-reset, and TRI-STATE output reset combinations. The $\overline{\text{RESET}}$ input must be low for a minimum of 140 µs.

1.9 Power And Ground Pins

TTL/CMOS INPUT/OUTPUT SUPPLY

Signal Name	Pin #	Description
IO_VDD	58, 64, 73, 79, 87, 93, 102, 109, 117, 123, 132, 143, 149, 167, 178, 187, 193, 202	3.3V I/O Supply
IO_VSS	57, 63, 72, 78, 86, 92, 101, 108, 116, 122, 131, 142, 148, 168, 179, 188, 194, 203	I/O Ground

TRANSMIT/RECEIVE SUPPLY

Signal Name	PQFP Pin #	Description
CD#_AVDD	8, 15, 38, 45	3.3V Common Driver Supply

CD#_AGND	11, 12, 41, 42	Common Driver Ground
R#_AVDD#	2, 6, 17, 21, 32, 36, 47, 51	3.3V Receiver Analog Supply
R#_AGND#	3, 7, 16, 20, 33, 37, 46, 50	Receiver Analog Ground
R#_ASUB	1, 22, 31, 52	Receiver Substrate Ground

INTERNAL SUPPLY PAIRS

Signal Name	PQFP Pin #	Description
CORE_VDD	69, 83, 98, 129, 137, 160, 171, 182, 197	1.8V Digital Supply
CORE_VSS	68, 82, 97, 128, 136, 161, 172, 183, 198	Digital Ground
CORE_SUB	67, 96, 127, 162, 173, 199	Substrate Ground
PGM_AVDD	27	3.3V PGM/CGM Supply. We recommend a low pass RC filter of a 18-22 Ω resistor and a 22 μF capacitor connected to this pin.
PGM_AGND	28	PGM/CGM Ground
BG_SUB	26	BG Substrate Ground
BG_AVDD	23	3.3V BG Supply
BG_AGND	25	BG Ground
SHR_VDD	29	3.3V Share Logic Supply
SHR_GND	30	Share Logic Ground
OSC_VDD	155	3.3V Oscillator Supply
OSC_VSS	152	Oscillator Ground

1.10 Special Connect Pins

Signal Name	PQFP Pin #	Description
BG_REF	24	Internal Reference Bias (requires connection to ground via a 9.31 kΩ resistor).
TEST	186, 206	These pins should be tied to 3.3 V.
SI,SO	104,105	These two pins should be floated.
RESERVE_FLOAT (Please also see next row. There are two sets of reserved pins-- one set needs to be pulled-down to gnd while the other set needs to be floated.)	53-56, 59-62, 65, 66, 70, 71, 74-77, 80, 81, 84, 85, 88-91, 94, 95, 99, 100, 103,106, 107	These pins are reserved. These pins are to be left floating.
RESERVE_GND	165, 166, 169, 170,174,175, 176,177	These pins are reserved and need to be tied to gnd.

Note:I = Input, O = Output, I/O = Bidirectional, Z = Tri-state output, S = Strapping pin

2.0 Configuration

This section includes information on the various configuration options available with the DP83861. The configuration options described herein include:

— Speed/Duplex Mode Selection
— Manual Mode Configurations
— Auto-Negotiation
— Isolate Mode
— Loopback Mode
— MII/GMII MAC Interface
— Test Modes
— Auto MDI / MDI-X Configuration
— Polarity Correction
— Firmware Interrupt

2.1 Speed/Duplex Mode Selection

The DP83861 supports six different Ethernet protocols: 10BASE-T Full Duplex, 10BASE-T Half Duplex, 100BASE-TX Full Duplex, 100BASE-TX Half Duplex, 1000BASE-T Full Duplex and 1000BASE-T Half Duplex. Both the speed and the Duplex mode of operation can be determined by either Auto-Negotiation or set by manual configuration. Both Auto-Negotiation and manual configuration can be controlled by strap values applied to certain pins during power-on/reset. They can be also controlled by access to internal registers.

2.2 Manual Mode Configurations

2.2.1 Forced Speed/Duplex Selection

The manual configuration of the speed and duplex modes of operation must be done with the Auto-Negotiation function has to be disabled. This can be achieved by strapping AN_EN low during power-on/reset. Auto-Negotiation can also be disabled by writing a "0" to bit 12 of the BMCR register. (0x00). Once AN_EN is disabled then the strap value of the SPEED[1:0] pins will be used to determine speed of operation, and the strap value of the LED_DUPLEX will be used to determine duplex mode.

Table 1. Non Auto-Negotiation Modes

AN_EN	SPEED [1]	SPEED [0]	Forced Mode
0	0	0	10BASE-T
0	0	1	100BASE-TX
0	1	0	1000BASE-T **(Test Mode Only)**
0	1	1	Reserved

For all of the modes above, DUPLEX strap value "1" selects Full Duplex, while "0" selects Half Duplex. The strap values latched-in during power-on/reset can be overwritten by access to the BMCR register 0x00 bits 13,12, 8 and 6.

It should be noted that Force 1000BASE-T mode is not supported by IEEE. This mode should be used for test purposes only. The DP83861 when in forced 1000BASE-T mode will only communicate with another DP83861 where one Phy is set for Slave operation and the other is set for Master operation.

2.2.2 Manual MASTER/SLAVE Resolution

In 1000BASE-T mode, one device needs to be configured as a Master and the other as a Slave. The Master device by definition uses a local clock to transmit data on the wire; while the Slave device uses the clock recovered from the incoming data for transmitting its own data. The DP83861 uses the Ref_CLK as the local clock for transmit purposes when configured as a Master. The Master and Slave assignments can be manually set by using strap options or register writes. Manual M/S Advertise(Pin 191, Reg. 9.11), Manual M/S Enable(Pin 195, Reg. 9.12), and Port Type(Pin 208, Reg. 9.10).

MASTER/SLAVE resolution for 1000BASE-T between a PHY and it's Link Partner can be resolved to sixteen possible out comes (See Table 3). The resolution outcome is based on the rankings which are shown in Table 2, where a Rank of 1 has the highest priority.

Table 2. Master/Slave Rankings and Settings

Rank	Configuration	Port Type Reg. 9.10 Pin 208	M/S Advertise Reg. 9.11 Pin 191	M/S Enable Reg. 9.12 Pin 195
1	Manual Master	Don't Care Don't Care	1 Pull High	1 Pull High
2	Multi-Port	1 Pull High	Don't Care Don't Care	Don't Care Don't Care
3	Single-Port	0 Pull Low	Don't Care Don't Care	Don't Care Don't Care
4	Manual Slave	Don't Care Don't Care	0 Pull Low	1 Pull High

Table 3. Master/Slave Outcome

DP83861 Advertise	Link Partner Advertise]	DP83861 Outcome	Link Partner Outcome
Manual Master	Manual Master	**Unresolved No Link**	**Unresolved No Link**
Manual Master	Manual Slave	Master	Slave
Manual Master	Multi-Port	Master	Slave
Manual Master	Single-Port	Master	Slave
Mult-Port	Manual Master	Slave	Master
Mult-Port	Manual Slave	Master	Slave
Mult-Port	Multi-Port	M/S resolved by random seed	M/S resolved by random seed
Mult-Port	Single-Port	Master	Slave
Single-Port	Manual Master	Slave	Master
Single-Port	Manual Slave	Master	Slave
Single-Port	Multi-Port	Slave	Master
Single-Port	Single-Port	M/S resolved by random seed	M/S resolved by random seed
Manual Slave	Manual Master	Slave	Master
Manual Slave	Manual Slave	**Unresolved No Link**	**Unresolved No Link**
Manual Slave	Multi-Port	Slave	Master
Manual Slave	Single-Port	Slave	Master

If both the link partner and the local device are manually given the same MASTER/SLAVE assignment, then an error condition will exist as indicated by bit 15 of register 0x0A. If one of the link partners is manually assigned a Master/Slave status while the other is not, then the manual assignment will take higher priority during the resolution process.

When Manual Slave or Manual Master mode is enabled Auto-Negotiation should also be enabled as per the 802.3 IEEE specification. The DP83861, however will link up to another DP83861 when Auto-Negotiation is disabled and one DP83861 is manually configured as a Master and the other is manually configured as a Slave.

An alternative way of specifying Master or Slave mode is to use the Port_Type strapping option pin 208 or by writing to register 0x09 bit 10. When pin 208 is pulled high or a 1 is written to bit 10 the part will advertise that it wants to be a Master. When pin 208 is pulled low or a 0 is written to bit 10 the part will advertise that it wants to be a Slave. If two devices advertise that they want to both be Master or both to be Slaves then the Auto-Negotiation statemachine will go through a random number arbitration sequence to pick which one will be the Master and which one will be the Slave. Using this method will eliminate the chance of an unresolved link.

2.3 Auto-Negotiation

All 1000BASE-T PHYs are required to support Auto-Negotiation. The Auto-Negotiation function in 1000BASE-T has four primary purposes:

— Auto-Negotiation Priority Resolution

— Auto-Negotiation MASTER/SLAVE Resolution

— Auto-Negotiation PAUSE/ ASYMMETRICAL PAUSE Resolution

— Auto-MDIX resolution

2.3.1 Auto-Negotiation Priority Resolution

First the Auto-Negotiation function provides a mechanism for exchanging configuration information between two ends of a link segment and automatically selecting the highest performance mode of operation supported by both devices.

Fast Link Pulse (FLP) Bursts provide the signalling used to communicate Auto-Negotiation abilities between two devices at each end of a link segment. For further details regarding Auto-Negotiation, refer to Clause 28 of the IEEE 802.3u specification. The DP83861 supports six different Ethernet protocols: 10BASE-T Full Duplex, 10BASE-T Half Duplex, 100BASE-TX Full Duplex, 100BASE-TX Half Duplex, 1000BASE-T Full Duplex and 1000BASE-T Half Duplex, so the inclusion of Auto-Negotiation ensures that the highest performance protocol will be selected based on the advertised ability of the Link Partner.

Auto-Negotiation Priority Resolution for the DP83861:

1. 1000BASE-T Full Duplex (Highest Priority)
2. 1000BASE-T Half Duplex
3. 100BASE-TX Full Duplex
4. 100BASE-TX Half Duplex
5. 10BASE-T Full Duplex
6. 10BASE-T Half Duplex (Lowest Priority)

2.3.2 Auto-Negotiation MASTER/SLAVE Resolution

The second goal of Auto-Negotiation in 1000BASE-T devices is to resolve MASTER/SLAVE configuration. If both devices have disabled manual Master/Slave configuration, MASTER priority is given to the devices which support multiport nodes (i.e. Switches and Repeaters take higher priority over DTEs or single node systems.). SPEED[0]/PORT_TYPE is a strap option for advertising the Multi-node functionality. (See Table 4) If both PHYs advertise the same options then the Master/Slave resolution is resolved by a random number generation. See IEEE 802.3ab Clause 40.5.1.2 and Table 3 for more details.

2.3.3 Auto-Negotiation PAUSE and Asymmetrical PAUSE Resolution

Auto-Negotiation is also used to determine the Flow Control capabilities of the two link partners. Flow control was originally introduced as a mechanism to force a busy station's Link Partner to stop sending data when in Full Duplex mode of operation. Unlike Half Duplex mode of operation where a link partner could be forced to back off by simply causing collisions, the Full Duplex operation needed a formal mechanism to slow down a link partner in the event of the receiving station's buffers becoming full. A new MAC control layer was added to handle the generation and reception of Pause Frames which contained a timer indicating the amount of Pause requested. Each MAC/Controller has to advertise whether it can handle PAUSE frames, and whether they support PAUSE frames in both directions. (i.e. receive and transmit. If the MAC/Controller will only generate PAUSE frames but will not respond to PAUSE frames generated by a link partner, then this is called Asymmetrical PAUSE.) Advertisement of these capabilities can be achieved by writing a '1' to bits 10 and 11 of the Auto-Neg Advertisement register (Address 0x04). The link partners PAUSE capabilities can be determined from register 0x05 using these same bits. The MAC/controller has to write to and read from these registers and determine which mode of PAUSE operation to choose. The PHY layer is not involved in Pause resolution other than the simple advertising and reporting of PAUSE capabilities. These capabilities are MAC specific. The MAC conveys these capabilities by writing to the appropriate PHY registers.

2.3.4 Auto-Negotiation Auto-MDIX Resolution

The DP83861 can determine if a "straight" or "cross-over" cable is being used to connect to the link partner and can automatically re-assign channel A and channel B to establish link with the link partner. Although not part of the Auto-Negotiation FLP exchange process, the Auto-MDIX resolution requires that Auto-Negotiation is enabled. Auto-MDIX resolution will precede the actual Auto-Negotiation process which involves exchange of FLPs to advertise capabilities. If Auto-Negotiation is not enabled, then the MDIX function can be manually configured by disabling Auto-MDIX. See Section 8.16 on FAQs for details.

2.3.5 Auto-Negotiation Strap Option Control

The Auto-Negotiation function within the DP83861 can be controlled either by internal register access or by the use of the AN_EN, and various strap pin values during power-on/reset. Table 4 shows how the various strap pin values

are used during Auto-Negotiation to advertise different capabilities.

Table 4. Auto-Negotiation Modes AN_EN = 1

Pin #	Pin Name	Comments
184	1000FDX_ADV /LED_1000	'1' Advertises 1000 Mb/s FDX capability.
185	LED_DUPLEX/ 1000HDX_ADV	'1' Advertises 1000 Mb/s HDX capability.
181	LED_100/ 100_ADV	'1' Advertises both 100 Mb/s FDX & HDX capability.
180	LED_10/ 10_ADV/ SPEED[1]	'1' Advertises 10 Mb/s FDX and HDX. '0' advertises neither FDX nor HDX 10 Mb/s capability.
208	SPEED[0]/ PORT_TYPE	'1' Advertises Multi-Node functionality. (e.g. Switch or Repeater, in contrast to NIC single node operation.)

2.3.6 Auto-Negotiation Register Control

The state of AN_EN, SPEED [1:0], DUPLEX pins as well as the xxx_ADV pins during power-on/reset determines whether the Auto-Negotiation is enabled and what specific ability (or set of abilities) are advertised as given in Table 4. These strapping option pins allow configuration options to be selected without requiring internal register access.

The Auto-Negotiation function selected at power-up or reset can be changed at any time by writing to the Basic Mode Control Register (BMCR) at address 0x00, Auto-Negotiation Advertisement Register 0x04 or to 1000BASE-T Control Register (1KTCR) 0x09.

When Auto-Negotiation is enabled, the DP83861 transmits the abilities programmed into the Auto-Negotiation Advertisement register (ANAR) at address 0x04, and 1000BASE-T Control register at address 0x09 via FLP Bursts. Any combination of 10 Mb/s,100 Mb/s, 1000 Mb/s, Half Duplex, and Full Duplex modes may be selected. The Auto-Negotiation protocol compares the contents of the ANLPAR and ANAR registers (for 10/100 Mb/s operation) and the contents of 1000BASE-T status and control registers, and uses the results to automatically configure to the highest performance protocol between the local and far-end port. The results of Auto-Negotiation may be accessed in registers BMCR (Duplex Status and Speed Status), and BMSR (Auto-Neg Complete, Remote Fault, Link).

The Basic Mode Control Register (BMCR) at address 00h provides control for enabling, disabling, and restarting the Auto-Negotiation process.

The Basic Mode Status Register (BMSR) at address 01h indicates the set of available abilities for technology types, Auto-Negotiation ability, and Extended Register Capability. These bits are permanently set to indicate the full functionality of the DP83861.

The BMSR also provides status on:

— Whether Auto-Negotiation is complete (bit 5)

— Whether the Link Partner is advertising that a remote fault has occurred (bit 4)

— Whether a valid link has been established (bit 2)

The Auto-Negotiation Advertisement Register (ANAR) at address 04h indicates the Auto-Negotiation abilities to be advertised by the DP83861. All available abilities are transmitted by default, but any ability can be suppressed by writing to the ANAR. Updating the ANAR to suppress an ability is one way for a management agent to change (force) the technology that is used.

The Auto-Negotiation Link Partner Ability Register (ANLPAR) at address 05h is used to receive the base link code word as well as all Next Page code words during Auto-Negotiation.

If Next Page is NOT being used, then the ANLPAR will store the base link code word (link partner's abilities) and retain this information from the time the page is received, as indicated by a 1 in bit 1 of the ANER register (address 06h), through the end of the negotiation and beyond.

When using the Next Page operation, the DP83861 cannot wait for Auto-Negotiation to complete in order to read the ANLPAR because the register is used to store both the base and next pages. Software must be available to perform several functions. The ANER (register 06h) must have a page received indication (bit 1), once the DP83861 receives the first page, software must store it in memory if it wants to keep the information. Auto-Negotiation keeps a copy of the base page information but it is no longer accessible by software. After reading the base page information, software needs to write to ANNPTR (register 07h) to load the next page information to be sent; continue to poll the page received bit in the ANER and when active, read the ANLPAR. The contents of the ANLPAR will tell if the partner has further pages to be sent. As long as the partner has more pages to send, software must write to the next page transmit register and load another page.

The Auto-Negotiation Expansion Register (ANER) at address 06h indicates additional Auto-Negotiation status. The ANER provides status on:

— Whether a Parallel Detect Fault has occurred (bit 4, register address 06h.)

— Whether the Link Partner supports the Next Page function (bit 3, register address 06h.)

— Whether the DP83861 supports the Next Page function (bit 2, register address 06h). (The DP83861 does support the Next Page function.)

— Whether the current page being exchanged by Auto-Negotiation has been received (bit1, register address 06h.)

— Whether the Link Partner supports Auto-Negotiation (bit 0, register address 06h.)

The Auto-Negotiation Next Page Transmit Register (ANNPTR) at address 07h contains the next page code word to be sent. See Auto-Negotiation Next Page Transmit Register (ANNPTR) address 07h for a bit description of this register.

2.3.7 Auto-Negotiation Parallel Detection

The DP83861 supports the Parallel Detection function as defined in the IEEE 802.3u specification. Parallel Detection requires the 10/100 Mb/s receivers to monitor the receive signal and report link status to the Auto-Negotiation function. Auto-Negotiation uses this information to configure the correct technology in the event that the Link Partner does not support Auto-Negotiation, yet is transmitting link signals that the 10BASE-T or 100BASE-X PMA recognize as valid link signals.

If the DP83861 completes Auto-Negotiation as a result of Parallel Detection, without Next Page operation, bits 5 and 7 within the ANLPAR register (address 05h) will be set to reflect the mode of operation present in the Link Partner. Note that bits 4:0 of the ANLPAR will also be set to 00001 based on a successful parallel detection to indicate a valid 802.3 selector field. Software may determine that Auto-Negotiation completed via Parallel Detection by reading a zero in the Link Partner Auto-Negotiation Ability register (bit 0, register address 06h) once the Auto-Negotiation Complete bit (bit 5, register address 01h) is set. If configured for parallel detect mode and any condition other than a single good link occurs then the parallel detect fault bit will set (bit 4, register 06h).

2.3.8 Auto-Negotiation Restart

Once Auto-Negotiation has completed, it may be restarted at any time by setting bit 9 (Restart Auto-Negotiation) of the BMCR to one. If the mode configured by a successful Auto-Negotiation loses a valid link, then the Auto-Negotiation process will resume and attempt to determine the configuration for the link. This function ensures that a valid configuration is maintained if the cable becomes disconnected.

A re-Auto-Negotiation request from any entity, such as a management agent, will cause the DP83861 to halt any transmit data and link pulse activity until the break_link_timer expires (~1 500 ms). Consequently, the Link Partner will go into link fail and normal Auto-Negotiation resumes. The DP83861 will resume Auto-Negotiation after the break_link_timer has expired by issuing FLP (Fast Link Pulse) bursts.

2.3.9 Enabling Auto-Negotiation via Software

It is important to note that if the DP83861 has been initialized upon power-up as a Non-Auto-Negotiating device (forced technology), and it is then required that Auto-Negotiation or re- Auto-Negotiation be initiated via software, bit 12 (Auto-Negotiation Enable) of the Basic Mode Control Register must first be cleared and then set for any Auto-Negotiation function to take effect.

2.3.10 Auto-Negotiation Complete Time

Parallel detection and Auto-Negotiation take approximately 2-3 seconds for 10/100 Mb/s devices and 5-6 seconds for 1000 Mb/s devices to complete. In addition, Auto-Negotiation with Next Page should take an additional 2-3 seconds to complete, depending on the number of next pages sent.

Refer to Clause 28 of the IEEE 802.3u standard for a full description of the individual timers related to Auto-Negotiation.

2.3.11 Auto-Negotiation Next Page Support

The DP83861 supports the optional Auto-Negotiation Next Page protocol. The ANNPTR register (address 07h) allows for the configuration and transmission of Next Page. Refer to clause 28 of the IEEE 802.3u standard for detailed information regarding the Auto-Negotiation Next Page function. This functionality is also discussed in Section 2.3.6 above and in the Section 7.0 (User Information).

2.4 MII Isolate Mode

2.4.1 10/100 Mb/s Isolate Mode

The DP83861 can be put into MII Isolate mode by writing to bit 10 of the BMCR register.

With bit 10 in the BMCR set to one, the DP83861 will not respond to packet data present at TXD[3:0], TX_EN, and TX_ER inputs and the TX_CLK, RX_CLK, RX_DV, RX_ER, RXD[3:0], COL, and CRS outputs will be TRI-STATED. The DP83861 will continue to respond to all management transactions on the MDIO line.

While in Isolate mode, the TD± outputs will not transmit packet data but will continue to source 100BASE-TX scrambled idles or the 10 Mb/s link pulses.

2.4.2 1000 Mb/s Isolate Mode

During 1000 Mb/s operation, entering the isolate mode will TRI-STATE the GMII outputs of the EN Gig PHYTER. When the DP83861 enters into the isolate mode all media access operations are halted and the DP83861 goes into power-down mode. The only way to communicate to the PHY is through the MDIO management port.

2.5 Loopback

The DP83861 includes a Loopback Test mode for easy board diagnostics. The Loopback mode is selected through bit 14 (Loopback) of the Basic Mode Control Register (BMCR). Writing 1 to this bit enables MII/GMII transmit data to be routed to the MII/GMII receive outputs. While in Loopback mode the data will not be transmitted onto the media. This is true for 10 Mb/s, 100 Mb/s, as well 1000 Mb/s data.

In 10BASE-T, 100BASE-TX, 1000BASE-T Loopback mode the data is routed through the PCS and PMA layers into the PMD sublayer before it is looped back. Therefore, in addition to serving as a board diagnostic, this mode serves as a quick functional verification of the device.

2.6 MII/GMII Interface and Speed of Operation

The DP83861 supports 2 different MAC interfaces. MII for 10 and 100 Mb/s, GMII for 1000 Mb/s. The speed of operation determines the interface chosen. The speed can be determined by Auto-Negotiation, or by strap options, or by register writes.

Table 5. Auto-Negotiation Disabled:

SPEED[1:0]	Link Strapped	Controller I/F
00	10BASE-T	MII
01	100BASE-TX	MII
10	1000BASE-T	GMII

Table 6. Auto-Negotiation Enabled:

Link Negotiated	Controller I/F
10BASE-T	MII
100BASE-TX	MII
1000BASE-T	GMII

2.7 Test Modes

IEEE 802.3ab specification for 1000BASE-T requires that the Physical layer device be able to generate certain well defined test patterns. Clause 40 section 40.6.1.1.2 "Test Modes" describes these tests in detail. There are four test modes as well as a normal mode. These modes can be selected by writing to the 1000BASE-T control register (0x09) as shown.

Table 7. Test Mode Select:

bit 15	bit 14	bit 13	Test Mode Selected
1	0	0	= Test Mode 4
0	1	1	= Test Mode 3
0	1	0	= Test Mode 2
0	0	1	= Test Mode 1
0	0	0	= Normal Operation

See IEEE 802.3ab section 40.6.1.1.2 "Test modes" for more information.

2.8 Automatic MDI / MDI-X Configuration

The DP83861 implements the automatic MDI/MDI-X configuration functionality as described in IEEE 802.3ab Clause 40, Section 40.4.4.1. This functionality eliminates the need for crossover cables between similar devices. The switching between the +/- A port with the +/- B port will be automatically taken care of, as well as switching between the +/- C port and the +/- D port.

The spec. calls for the physical layer device to detect it's Link Partners link pulses within 62 ms. During the MDIX detection phase the DP83861 sends out link pulses that are spaced 150 µs apart. The 150 µs link pulse spacing was purposely selected to transmit non-FLP bursts (FLP pulses are spaced 124 µs +/- 14 µs) so that the link partner would not mistakenly attempt to "link up" on the MDIX link pulses.

2.9 Polarity Correction

The EN Gig PHYTER will automatically detect and correct for polarity reversal in wiring between the +/- wires for each of the 4 ports.

2.10 Firmware Interrupt

DP83861 can be configured to generate an interrupt on pin 208 when changes of internal status occur. The interrupt allows a MAC to act upon the status in the PHY without polling the PHY registers. The interrupt source can be selected through the interrupt register set. This register set consists of:

— Interrupt Status Registers
  – ISR0 0x810D
  – ISR1 0x810E
— Interrupt Enable Registers
  – IER0 0x8113
  – IER1 0x8114
— Interrupt Clear Registers
  – ICLR0 0x8115
  – ICLR1 0x8116
— Interrupt Control Register
  – ICTR 0x8117
— Interrupt Raw Reason Registers
  – RRR0 0x8111
  – RRR1 0x8112
— Interrupt Reason Registers
  – IRR0 0x810F
  – IRR1 0x8110

Upon reset, interrupt is disabled and the interrupt registers are initialized with their default values.

The interrupt signal's polarity can be easily programmed in the ICTR. The polarity can be configured active high or active low. In the latched mode, the interrupt signal is asserted and remains asserted while the corresponding enabled status bit is asserted. **The Interrupt pin is not an Open Drain Output and should not be wired OR'ed to other pins.** The status bits are the sources of the interrupt. These bits are mapped in the ISR. When the interrupt status bit is "1", the interrupt signal is asserted if the corresponding IER bit is enabled. An interrupt status bit can be cleared by writing a "1" to the corresponding bit in the ICLR. The clear bit returns to "0" automatically after the interrupt status bit is cleared.

The RRR contains the current status of the signals being monitored. Note that the status of the configuration, duplex, and speed are recorded in the most recent period while the link was up.

The IRR records the "reason" that an interrupt status bit is asserted. For example, if the isr_link bit is asserted in the ISR because a link is achieved, then a "1" is stored in the corresponding IRR bit field. This IRR bit field is not changed until the interrupt is serviced, regardless how many times the source status (in RRR) changes in the intervening period. The IRR bit can be cleared by writing a "1" to the corresponding bit in the ICLR register.

The purpose of the IRR is for the interrupt logic to determine the next state change to cause an interrupt. In reality, the PHY may operate at much faster pace than the interrupt service provider. The IRR provides a mechanism for the higher layers to decipher the context of the interrupt although the context of the system may have changed by the time the interrupt is serviced. For instance, when link is lost and regained in quick succession, it is likely that a sequence of interrupts are generated by the same event. The IRR preserves the status of the event that may have changed during the interrupt service. A new interrupt may be generated if the status is changed based on the comparison between the IRR and the RRR.

Note that all the interrupt registers are extended registers located in the expanded memory space. Please refer to Register Block section for details.

3.0 Design and Layout Guide

This guide will provide information to assist in the design and layout of the DP83861 Gigabit Ethernet Transceiver. This guide will cover the following areas:

— Power Supply Filtering
— Twisted Pair Interface
— MAC Interface
— Clocks
— LED/Strapping Configuration
— Unused Pins/ Reserved Pins
— Hardware Reset
— Temperature Considerations
— List of Pins and Pin Connection Guide

3.1 Power Supply Filtering

It is recommended that the PCB have at least one solid ground plane, one solid 3.3 V plane, and one solid 1.8 V plane, with no breaks in any of these planes. The inter-plane capacitance between the supply and ground planes should be maximized by minimizing the distance between these planes. Filling unused signal planes with copper and connecting them to the proper power plane will also increase the interplane capacitance. The inter-plane capacitance acts like a short at high frequencies to reduce supply plane impedance. Not all designs will be able to incorporate the recommended suggestions because of board cost constraints. Working designs have been done using only 4 layers. National has a reference design built using the ENGig PHYTER and our GigMAC. This reference design is a PCI NIC card, using only 4 layers and having component placement on only one side of the board to reduce cost. The schematic, layout and gerber files for this reference design are available upon request.

The 3.3 V & the 1.8 V supply pins come in pairs with their corresponding ground pins (i.e. a 3.3 V supply-ground pair is formed by pin 2 [RA_AVDD] and pin 3 [RA_AGND]). These paired pins are physically adjacent to each other. The matching pins should be bypassed with low impedance surface mount capacitors of value 0.1 µF connected directly into the power planes with vias as close as possible to the pins. This will reduce the inductance in series with the bypass capacitor. Any increase in inductance will lower the capacitor's self resonant frequency which will degrade the high frequency performance of the capacitor. It's also recommended that 0.01 µF capacitors are connected in parallel with the 0.1 µF capacitors, or at least "dispersed", replacing some of the 0.1 µF capacitors. The lower value capacitance will increase the frequency range of effectiveness of the bypassing scheme. This is due to the unavoidable inductance of the leads and connections on the board, which cause resonance at low frequencies for large value capacitors.

The Analog PGM supply requires special filtering to attenuate high frequencies. High frequencies will increase the jitter of the PGM. We recommend a low pass filter formed by a 18-22 Ω resistor and two capacitors in parallel. One of the capacitors should be 22 µF and the other 0.01 µF. (This will implement a single pole low pass filter with 3 dB freq. around 360 - 400 Hz.). The maximum current on this supply is 5 mA.

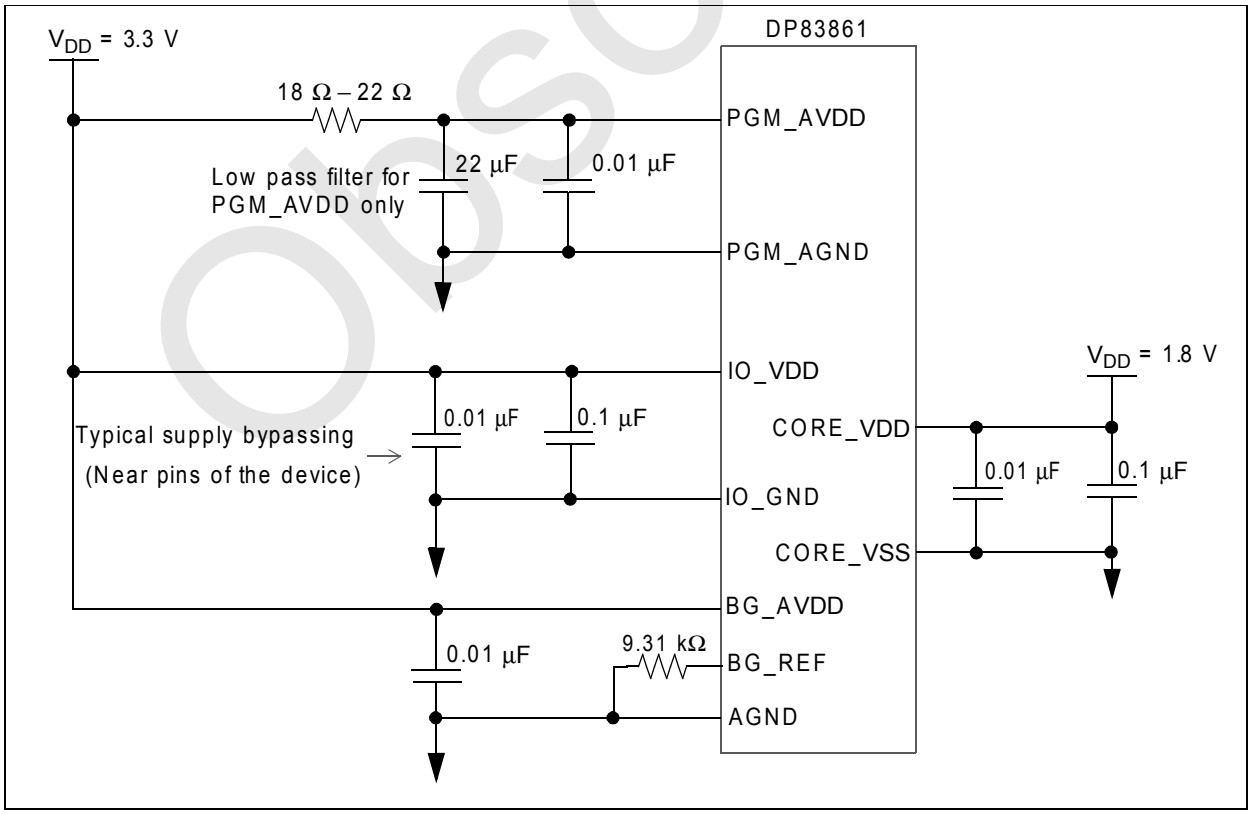


Figure 1. Power Supply Filtering

A 10 µF capacitor should also be placed close to the DP83861 (possibly on the bottom side of the PCB) bypassing the VCC and ground planes.

There has been considerable discussion in the literature about the use of ferrite beads to isolate power plane noise from certain noisy VCC pins and preventing this noise from coupling into sensitive analog VCC pins. This is typically achieved by using ferrite beads (inductors) between noisy VCC and quiet VCC line. An inductor in conjunction with the bypass capacitor at the VCC pins will form a low pass filter which will prevent the high frequency noise from coupling into the quite VCC. However, using this scheme can give mixed results. There is considerable debate about whether this approach is necessary or even useful. In most of our boards we put in a stuffing option for inductors (zero Ohm resistors). In general we have not found any improvements with the use of ferrite beads, however noise considerations are very dependent on PCB's specific layout, function and power supplies. The board designer should evaluate whether they will benefit from ferrite beads in their particular board.

The pin check list on Table 14 show the suggested connections of these capacitors for every supply, ground and substrate pin.

3.2 Twisted Pair Interface

The Twisted Pair Interface consists of four differential transmit pairs (Channels A, B, C, and D) and four differential receive pairs (Channels A, B, C, and D). Each transmit pair is connected to its' corresponding receive pair through 47 Ω and 150 Ω resistors respectively (The two 47 Ω resistors in combination with the source impedance of the transmitter will form a 100 Ω differential input impedance as seen from the line. This is required to minimize reflections.). Figure 2 shows a typical connection for Channel A. Channels B, C, and D are identical. The combined transmit and receive trace then goes directly to 1:1 magnetics. We currently recommend using the Pulse H-5007 or Pulse H-5008. Both magnetics are pin for pin compatible, but with different package orientations. The H-5007/8 has an isolation transformer followed by a common mode choke to reduce EMI. There is an additional auto-transformer which is center tapped. These 2 transformers as well as other suppliers' transformers from Halo, Bel fuse, Midcom, etc. should be evaluated for best performance for each design. See Table 9 and Table 10.

— Place the 47 Ω 1% transmit resistors as close as possible to the TXDA+/-, TXDB+/-, TXDC+/-, and TXD+/- pins

— Place the 150 Ω 1% receive resistors close as possible to the RXDA+/-, RXDB+/-, RXDC+/-, and RXDD+/- pins.

— All traces to and from the twisted pair interface should have a controlled impedance of 50 Ω to the ground plane. This is a strict requirement. They should be as close in length to each other as possible to prevent mismatches in delay which will increase common mode noise.

Ideally there should be no crossovers or vias on the signal paths of these traces.

3.3 MAC Interface

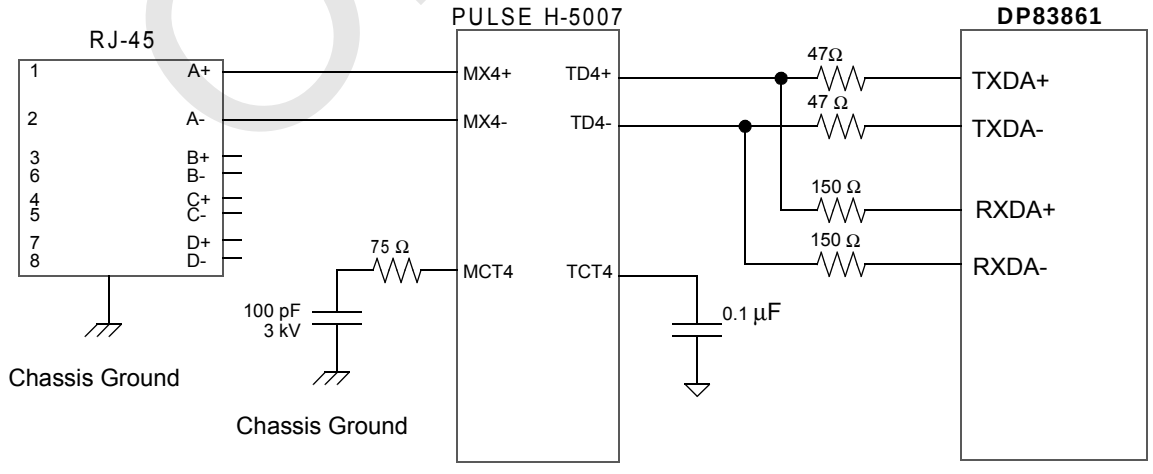
The DP83861 can be configured in one of two different modes:

— GMII (Gigabit Media Independent Interface) MODE: This interfaces is used to support 802.3z compliant 1000 Mb/s MACs.

— MII (Media Independent Interface) MODE: This interface is used to support 10/100 Mb/s MACs.

Only one mode can be supported at a time, since the GMII and MII share some pins in common.

These outputs are capable of driving 35 pF under worst case conditions. These outputs were not designed to drive multiple loads, connectors, backplanes, or cables. It is recommended that the outputs be series terminated through a resistor as close to the output pins as possible. The purpose of the series termination is to reduce reflections on the line. The value of the series termination and length of trace the output can drive will depend on the driver output impedance, the characteristic impedance of the PCB trace (we recommend 50 Ω), the distributed trace capacitance (capacitance/inch), and the load capacitance (MAC input). For short traces, less than 0.5 inches, the series resistors may not be required, thus reducing component count. However, each specific board design should be evaluated for reflections and signal integrity to determine the need for the series terminations. As a general rule of thumb, if the trace length is less than 1/6 of the equivalent length of the



Only the connections for one of the twisted pair channels is shown. Connections for channels B, C, D are similar.

Figure 2. Twisted Pair / Magnetics Interface (Channel A Only)

rise and fall times then the series terminations might not be needed. Equivalent length of rise time = Rise time (ps) / Delay (ps/inch). Rise and fall times are required to be less than 1 ns for some GMII signals, typically being in the order of 500 ps for those pins. (i.e. RX_CLK, GTX_CLK). Delay typically = 170 ps/inch on a FR4 board. Using the above numbers we get critical trace length = (1/6) *(500/ 170) = 0.5 inches.

.In summary:

— Place series termination resistors as close to the pins as possible.

— Keep capacitance < 35 pF as seen by the output.

— Keep output trace lengths approximately the same length to avoid skew problems.

— Keep input trace lengths approximately the same length to avoid skew problems.

All GMII traces should be impedance controlled. 50 ohms to ground plane is recommended, but this is not a strict requirement and the board designer can experiment with different values if needed, to minimize reflections

3.4 Clocks

REF_CLK is capable of using either a 125 MHz oscillator or a 25 MHz oscillator. The 125 MHz or 25 MHz clock is used by the internal PLL to generate the various clocks needed both internally and externally. This input should come from an 125 MHz oscillator (+/- 50 ppm, < 25ps cycle to cycle jitter, < 200 ps accumulative jitter) or a 25 MHz oscillator (+/- 50 ppm, < 25ps cycle to cycle jitter, < 200 ps accumulative jitter). For 125 MHz operation, REF_SEL (pin 154) must be either connected directly to a 3.3 V supply or pulled high through a 2 KΩ resistor to a 3.3 V supply. When using a 25 MHz oscillator the REF_SEL (pin 154) should be pulled to ground through a 2 KΩ resistor.

The cycle to cycle jitter and the long term accumulative jitter (accumulative jitter can be measured using an oscilloscope with a delay trigger set at 10 µs or using a Wavecrest TIA). Both the 125 MHz and 25 MHz oscillators should have less than 25 ps of cycle to cycle jitter and less than 200 ps accumulative jitter for optimal cable performance. **Testing using the 25 MHz oscillator showed that the DP83861 will exceed the 100 meter cable length requirement in 1000 Mb/s, 100 Mb/s and 10 Mb/s, but the transmit jitter in 1000 mb/s mode will be outside the IEEE spec. 40.6.1.2.5 (transmit clock jitter + transmit output jitter) of less than 300 ps.**

The clock signal requires the same termination considerations mentioned in the MAC interface section. The clock signal might require both series source termination (R_S) at the output of the clock source and/or load termination (R_T) close to the PHY to eliminate reflections. This will depend on the distance of the clock source from the PHY clock input, the source impedance of the clock source, as well as the board impedance for the clock line considered as a transmission line. Typically no series or load termination is required for short traces. For long traces a series resistor is recommended. Unlike load termination, this doesn't add to the load current. The value of the series termination resistor has to be chosen to match the line impedance. As an example, if the clock source has output impedance of 20Ω and the clock trace has transmission line impedance Zo = 50Ω then Rs = 50 - 20 = 30Ω.

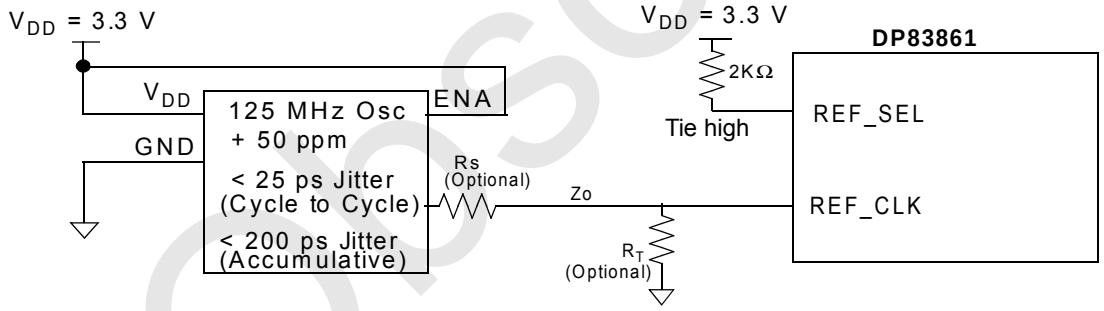


Figure 3. 125 MHz Oscillator Option

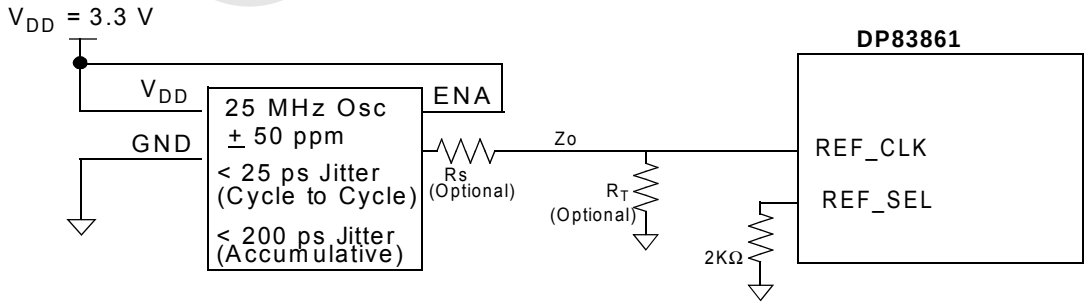


Figure 4. 25 MHz Oscillator Option

3.5 Strapping Options

3.5.1 PHY ADDRESS/ LED STRAPPING

The five PHY address inputs pins are shared with the LED pins as shown below.

Table 8. PHY Address Mapping

Pin #	PHYAD Function	LED Function
200	PHYAD_0	ACT
201	PHYAD_1	COL
204	PHYAD_2	LNK
205	PHYAD_3	TX
207	PHYAD_4	RX

The DP83861 can be set to respond to any of 32 possible PHY addresses. (However PHY Address = 0 will put the ENGig PHYTER in power-down/isolate mode. When in power-down/isolate mode the part turns off it's transmitter, receiver and GMII inputs/outputs. When in this mode the part will only respond to MDIO/MDC activity. After power-on, the PHY should be taken out of power-down isolation by resetting bit 11 of register 0x00.) Each DP83861 or port sharing an MDIO bus in a system must have a unique physical address.

The pull-up or pull-down state of each of the PHYAD inputs is latched (register 0x10) at system power-up/reset. For further detail relating to the latch-in timing requirements of the PHY Address pins, as well as the other hardware configuration pins, refer to the Reset timing in Section 5.7.

Since the PHYAD strap options share the LED output pins, the external components required for strapping and LED usage must be considered in order to avoid contention.

Specifically, when the LED outputs are used to drive LEDs directly, the active state of each output driver is dependent on the logic level sampled by the corresponding PHYAD input upon power-up/reset. For example, if a given PHYAD input is resistively pulled low then the corresponding output will be configured as an active high driver. Conversely, if a given PHYAD input is resistively pulled high then the corresponding output will be configured as an active low driver. Refer to Figure 5 for an example of LED & PHYAD connection to external components. In this example, the PHYAD strapping results in address 00011 (03h).

This adaptive nature for choosing the active high or active low configuration applies to all the LED pins; not just the LED pins associated with PHYAD strap options. So all LED pins will be high active if the strap value during reset on that specific LED pin was a '0'. Else if the strap value was a '1' then the LED will be low active.

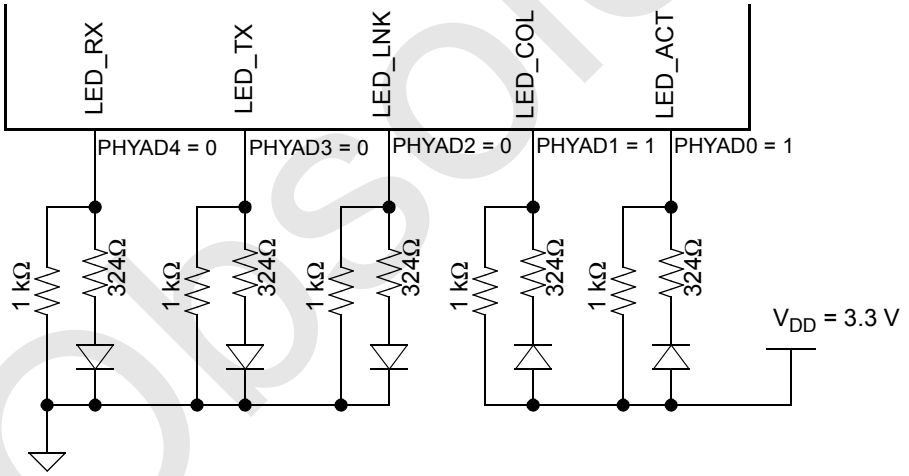


Figure 5. PHYAD Strapping and LED Loading Example

3.6 Unused Pins/Reserved Pins

It is well known that unused CMOS input pins should not be left floating. This could result in inputs floating to intermediate values halfway between VCC and ground and turning on both the NMOS and the PMOS transistors, thus resulting in high DC currents. It could also result in oscillations. Therefore unused inputs should be tied high or low. In theory CMOS inputs can be directly tied to VCC or GND. This method has the advantage of minimizing component count and board area. However, it's considered safer to pull the unused input pins high or low with a pull-up or pull-down resistor. This will prevent excessive currents in case of a defect in the input structure, shorting either VCC or GND to the input. Another advantage of this method is to reduce chances of latch-up. As a compromise between the two approaches, one can group together adjacent unused input pins, and as a group pull them up or down using a single resistor. See "Reference design schematics" for a detailed example of how unused pins can be grouped to be pulled-down using a single resistor.

Typical unused input pins can be the JTAG pins TDI, TRST, TMS and TCK which can be all tied together and pulled-down using a 2 kΩ resistor. Some of the other reserved or unused pins include pins 186 and 206 (TEST); pins 165, 166,169,170,174,175,176, and 177 (RESERVE_GND); pin 104 (SI). All these pins except TEST pins can be pulled-down using a 2 kΩ resistor per group of pins. TEST pins can be pulled up or tied to VCC.

In general, using pull-up and pull-down resistors instead of tying unused inputs directly to VCC or ground has the following disadvantages:

— Additional cost of components

— Additional board area. (May prevent fitting into fewer layers of PCB, having components only on the top side, or fitting into small profile cards.)

— Reliability problems (Due to bad solder joints, etc.)

— Need to test components: Might necessitate additional vias to be drilled to have test points on the back side, for in circuit test. This adds to PCB manufacturing time, and cost. Also testing additional components add to in circuit test duration, and makes the test program longer to write.

— Inventory costs for the additional components

3.7 Hardware Reset

$\overline{\text{RESET}}$ pin 164 which is active low should be held low for a minimum of 140 µs to allow hardware reset. During hardware reset the strap option pins are re-latched, and register and state machines are reset. For timing details see Figure 5.7. There is no on-chip internal power-on reset and the DP83861 requires an external reset signal be applied to the $\overline{\text{RESET}}$ pin.

3.8 Temperature Considerations

The DP83861 utilizes an enhanced 208 PQFP package that eliminates the need for heatsinks. The package has a built in copper heat slug at the top of the package which provides a very efficient method of removing heat from the die through convection. Since the heat slug is on the top of the package the PCB board stays cooler. The enhance package has a low Theta Junction to Case of 2.13 ^{o}C/W and a Theta Junction to Ambient of 11.7 ^{o}C/W.

For reliability purposes the die temperature of the DP83861 should be kept below 120 ^{o}C, this translates to a package case temperature of 112 ^{o}C. For more information on how this calculation is done see Section 8.15 (Frequently Asked Questions)

3.9 Pin List and Connections

Table 14 provides pin listings and their connections. This list should be used to make sure all pin connections are correct.

Table 9. Magnetic Requirements

Parameter	Min.	Typ.	Max.	Units	Conditions
Turns Ratio	-	1:1	-	-	+/- 2%
Insertion Loss	0.0	-	1.1	dB	0.1 - 1 MHz
	-	-	0.5	dB	1.0 - 60 MHz
	-	-	1.0	dB	60 - 100 MHz
	-	-	1.2	dB	100 - 125 MHz
Return Loss	-18	-	-	dB	1.0 - 30 MHz
	-14.4	-	-	dB	30 - 40 MHz
	-13.1	-	-	dB	40 - 50 MHz
	-12.0	-	-	dB	50 - 80 MHz
	-10.0	-	-	dB	80 - 100 MHz
Differential to Common Mode Rejection	-43.0	-	-	dB	1.0 - 30 MHz
	-37.0	-	-	dB	30 - 60 MHz
	-33.0	-	-	dB	60 - 100 MHz
Cross Talk	-45.0	-	-	dB	1.0 - 30 MHz
	-40.0	-	-	dB	30 - 60 MHz
	-35.0	-	-	dB	60 - 100 MHz
Isolation	1500	-	-	V	-
Rise Time	-	1.6	1.8	ns	10 - 90%
Primary Inductance	350	-	-	µH	-

Table 10. Magnetic Manufacturers

Manufacture	Website	Part Number
Pulse Engineering	www.pulseeng.com	H5007 H5008
Bel Fuse	www.belfuse.com	S558-5999-P3 S558-599-T3
Delta	www.delta.tw	LF9203
Halo	www.haloelectronics.com	TG1G-S002NZ
Midcom	www.midcom-inc.com	000-7044-37R 000-7093-37R
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Note: Contact Magnetics manufactures for latest part numbers and product specifications. All Magnetics should be thoroughly tested and validated before using them in production.		

Table 11. 25 MHz Oscillator Requirements

Parameter	Min.	Typ.	Max.	Units	Conditions
Frequency	-	25	-	MHz	-
Frequency Stability	- 50	0	50	ppm	0 to 70 ^{o}C
Rise/Fall Time				ns	20 - 80%
Symmetry	40		60	%	duty cycle
Jitter (Cycle to Cycle)		-	25	ps	rising edge to rising edge
Jitter (Accumulative)			200	ps	delay trigger 10 µs
Logic 0			10% VDD	V	VDD = 2.5 or 3.3 V nominal
Logic 1	90% Vdd			V	VDD = 2.5 or 3.3 V nominal

Table 12. 125 MHz Oscillator Requirements

Parameter	Min.	Typ.	Max.	Units	Conditions
Frequency	-	125	-	MHz	-
Frequency Stability	- 50	0	50	ppm	0 to 70 ^{o}C
Rise/Fall Time			2.5	ns	20 - 80%
Symmetry	40		60	%	duty cycle
Jitter (Cycle to Cycle)		-	25	ps	rising edge to rising edge
Jitter (Accumulative)			200	ps	delay trigger 10 µs
Logic 0			10% VDD	V	VDD = 2.5 or 3.3 V nominal
Logic 1	90% Vdd			V	VDD = 2.5 or 3.3 V nominal

Table 13. Oscillator Manufacturers

Manufacture	Website	Part Number
Vite Technology	www.viteonline.com	25 MHz (VCC1-B2B-25M000) 125 MHz (VCC1-B2B-125M000)
SaRonix	www.saronix.com	125 MHz (SCS-NS-1132)
Valpey Fisher	www.valpeyfisher.com	125 MHz (VAC570BL) 125 MHz (VFAC38L)
Note: Contact Oscillator manufactures for latest information on part numbers and product specifications. All Oscillators should be thoroughly tested and validated before using them in production.		

Table 14. Pin List

Pin #	DataSheet Pin Name	Type	Connections/ Comments
1	RA_ASUB	Ground	**Substrate Ground**: Connect to ground plane.
2	RA_AV_{DD}	Power	**Receive Analog 3.3 V Supply**: Bypass to pin 3 using a 0.1 µF capacitor.
3	RA_AGND	Ground	**Receive Analog Ground**: Connect to ground plane.
4	RXDA+	Input	**Channel A Receive Data Positive**: Connect to pin 12 of the H-5007 magnetics through a 150 Ω, 1% resistor. See Figure 2
5	RXDA-	Input	**Channel A Receive Data Negative**: Connect to pin 11 of the H-5007 magnetics through a 150 Ω, 1% resistor. See Figure 2.
6	RA_AV_{DD}	Power	**Receive Analog 3.3V Supply**: Bypass to pin 7 using a 0.1 µF capacitor.
7	RA_AGND	Ground	**Receive Analog Ground**: Connect to ground plane.
8	CDA_AV_{DD}	Power	**Transmit Analog 3.3V Supply**: Bypass to pin 11 using a 0.1 µF capacitor.
9	TXDA+	Output	**Channel A Transmit Data Positive**: Connect to pin 12 of the H-5007 magnetics through a 47 Ω, 1% resistor. See Figure 2.
10	TXDA-	Output	**Channel A Transmit Data Negative**: Connect to pin 11 of the H-5007 magnetics through a 47 Ω, 1% resistor. See Figure 2.
11	CDA_AGND	Ground	**Transmit Analog Ground**: Connect to ground plane.
12	CDB_AGND	Ground	**Transmit Analog Ground**: Connect to ground plane.
13	TXDB-	Output	**Channel B Transmit Data Negative**: Connect to pin 9 of the H-5007 magnetics through a 47 Ω, 1% resistor. See See Figure 2.
14	TXDB+	Output	**Channel B Transmit Data Positive**: Connect to pin 8 of the H-5007 magnetics through a 47 Ω, 1% resistor. See See Figure 2.
15	CDB_AV_{DD}	Power	**Transmit Analog 3.3V Supply**: Bypass to pin 12 using a 0.1 µF capacitor.
16	RB_AGND	Ground	**Receive Analog Ground**: Connect to ground plane.
17	RB_AV_{DD}	Power	**Receive Analog 3.3V Supply**: Bypass to pin 16 using a 0.1 µF capacitor.
18	RXDB-	Input	**Channel B Receive Data Negative**: Connect to pin 9 of the H-5007 magnetics through a 150 Ω, 1% resistor. See Figure 2.
19	RXDB+	Input	**Channel B Receive Data Positive**: Connect to pin 8 of the H-5007 magnetics through a 150 Ω, 1% resistor. See Figure 2.
20	RB_AGND	Ground	**Receive Analog Ground**: Connect to ground plane.
21	RB_AV_{DD}	Power	**Receive Analog 3.3V Supply**: Bypass to pin 20 using a 0.1 µF capacitor.

Pin #	DataSheet Pin Name	Type	Connections/ Comments
22	RB_ASUB	Ground	**Substrate Ground**: Connect to ground plane.
23	BG_AV_{DD}	Power	**Bandgap 3.3V Supply**: Connect to pin 25 using a 0.01 µF capacitor.
24	BG_REF	Input	**Bandgap Reference**: Connect to pin 25 using a 9.31K Ω, 1% resistor. The resistor should be placed as close to pin 24 as possible to reduce trace inductance and reduce the possibility of picking up noise through crosstalk.
25	BG_AGND	Ground	**Bandgap Ground**: Connect to ground plane.
26	BG_SUB	Ground	**Bandgap Substrate**: Connect to ground plane.
27	PGM_AV_{DD}	Power	**PGM Analog 3.3V Supply**: See Figure 1
28	PGM_AGND	Ground	**PGM Ground**: Connect to ground plane.
29	SHR_V_{DD}	Power	**Analog 3.3V Supply**: Connect to pin 30 using a 0.1 µF capacitor.
30	SHR_GND	Ground	**Analog ground**: Connect to ground plane.
31	RC_ASUB	Ground	**Substrate Ground**: Connect to ground plane.
32	RC_AV_{DD}	Power	**Receive Analog 3.3V Supply**: Bypass to pin 33 using a 0.1 µF capacitor.
33	RC_AGND	Ground	**Receive Analog Ground**: Connect to ground plane.
34	RXDC+	Input	**Channel C Receive Data Positive**: Connect to pin 6 of the H-5007 magnetics through a 150 Ω resistor (1%). See Figure 2.
35	RXDC-	Input	**Channel C Receive Data Negative**: Connect to pin 5 of the H-5007 magnetics through a 150 Ω resistor (1%). See Figure 2.
36	RC_AV_{DD}	Power	**Receive Analog 3.3V Supply**: Bypass to pin 37 using a 0.1 µF capacitor.
37	RC_AGND	Ground	**Receive Analog Ground**: Connect to ground plane.
38	CDC_AV_{DD}	Power	**Transmit Analog 3.3V Supply**: Bypass to pin 41 using a 0.1 µF capacitor.
39	TXDC+	Output	**Channel C Transmit Data Positive**: Connect to pin 6 of the H-5007 magnetics through a 47 Ω, 1% resistor. See Figure 2.
40	TXDC-	Output	**Channel C Transmit Data Negative** Connect to pin 5 of the H-5007 magnetics through a 47 Ω resistor (1%). See Figure 2.
41	CDC_AGND	Ground	**Transmit Analog Ground**: Connect to ground plane.
42	CDD_AGND	Ground	**Transmit Analog Ground**: Connect to ground plane.
43	TXDD-	Output	**Channel D Transmit Data Negative**: Connect to pin 3 of the H-5007 magnetics through a 47 Ω resistor (1%). See Figure 2.

Pin #	DataSheet Pin Name	Type	Connections/ Comments
44	TXDD+	Output	**Channel D Transmit Data Positive**: Connect to pin 2 of the H-5007 magnetics through a 47 Ω, 1% resistor. See Figure 2.
45	CDD_AV_{DD}	Power	**Transmit Analog 3.3V Supply**: Bypass to pin 42 using a 0.1 µF capacitor.
46	RD_AGND	Ground	**Receive Analog Ground**: Connect to ground plane.
47	RD_AV_{DD}	Power	**Receive Analog 3.3V Supply**: Bypass to pin 46 using a 0.1 µF capacitor.
48	RXDD-	Input	**Channel D Receive Data Negative**: Connect to pin 3 of the H-5007 magnetics through a 150 Ω resistor (1%). See Figure 2.
49	RXDD+	Input	**Channel D Receive Data Positive**: Connect to pin 2 of the H-5007 magnetics through a 150 Ω resistor (1%). See Figure 2.
50	RD_AGND	Ground	**Receive Analog Ground**: Connect to ground plane.
51	RD_AV_{DD}	Power	**Receive Analog 3.3V Supply**: Bypass to pin 50 using a 0.1 µF capacitor.
52	RD_ASUB	Ground	**Substrate Ground**: Connect to ground plane.
53	RESERVE_FLOAT		**Reserved**: Leave floating.
54	RESERVE_FLOAT		**Reserved**: Leave floating.
55	RESERVE_FLOAT		**Reserved**: Leave floating.
56	RESERVE_FLOAT		**Reserved**: Leave floating.
57	IO_VSS	Ground	**I/O Ground**: Connect to ground plane.
58	IO_V_{DD}	Power	**I/O 3.3V Supply**: Bypass to pin 57 using a 0.1 µF capacitor.
59	RESERVE_FLOAT		**Reserved**: Leave floating.
60	RESERVE_FLOAT		**Reserved**: Leave floating.
61	RESERVE_FLOAT		**Reserved**: Leave floating.
62	RESERVE_FLOAT		**Reserved**: Leave floating.
63	IO_VSS	Ground	**I/O Ground**: Connect to ground plane.
64	IO_V_{DD}	Power	**I/O 3.3V Supply**: Bypass to pin 63 using a 0.1 µF capacitor.
65	RESERVE_FLOAT		**Reserved**: Leave floating.
66	RESERVE_FLOAT		**Reserved**: Leave floating.
67	CORE_SUB	Ground	**Digital Core Substrate**: Connect to ground plane.
68	CORE_VSS	Ground	**Digital Core Ground**: Connect to ground plane.
69	CORE_V_{DD}	Power	**Digital Core 1.8 V Supply**: Bypass to pin 68 using a 0.1 µF capacitor.
70	RESERVED_FLOAT		**Reserved**: Leave floating.

Pin #	DataSheet Pin Name	Type	Connections/ Comments
71	RESERVED_FLOAT		**Reserved**: Leave floating.
72	IO_VSS	Ground	**I/O Ground**: Connect to ground plane.
73	IO_V_{DD}	Power	**I/O 3.3V Supply**: Bypass to pin 72 using a 0.1 µF capacitor.
74	RESERVE_FLOAT		**Reserved**: Leave floating.
75	RESERVE_FLOAT		**Reserved**: Leave floating.
76	RESERVE_FLOAT		**Reserved**: Leave floating.
77	RESERVE_FLOAT		**Reserved**: Leave floating.
78	IO_VSS	Ground	**I/O Ground**: Connect to ground plane.
79	IO_V_{DD}	Power	**I/O 3.3V Supply**: Bypass to pin 78 using a 0.1 µF capacitor.
80	RESERVE_FLOAT		**Reserved**: Leave floating.
81	RESERVE_FLOAT		**Reserved**: Leave floating.
82	CORE_VSS	Ground	**Digital Core Ground**: Connect to ground plane.
83	CORE_V_{DD}	Power	**Digital Core1.8 V Supply**: Bypass to pin 82 using a 0.1 µF capacitor.
84	RESERVE_FLOAT		**Reserved**: Leave floating.
85	RESERVE_FLOAT		**Reserved**: Leave floating.
86	IO_VSS	Ground	**I/O Ground**: Connect to ground plane.
87	IO_V_{DD}	Power	**I/O 3.3V Supply**: Bypass to pin 86 using a 0.1 µF capacitor.
88	RESERVE_FLOAT		**Reserved**: Leave floating.
89	RESERVE_FLOAT		**Reserved**: Leave floating.
90	RESERVE_FLOAT		**Reserved**: Leave floating.
91	RESERVE_FLOAT		**Reserved**: Leave floating.
92	IO_VSS	Ground	**I/O Ground**: Connect to ground plane.
93	IO_V_{DD}	Power	**I/O 3.3V Supply**: Bypass to pin 92 using a 0.1 µF capacitor.
94	RESERVE_FLOAT		**Reserved**: Leave floating.
95	RESERVE_FLOAT		**Reserved**: Leave floating.
96	CORE_SUB	Ground	**Digital Core Substrate**: Connect to ground plane.
97	CORE_VSS	Ground	**Digital Core Ground**: Connect to ground plane.
98	CORE_V_{DD}	Power	**Digital Core 1.8 V Supply**: Bypass to pin 97 using a 0.1 µF capacitor.
99	RESERVE_FLOAT		**Reserved**: Leave floating.
100	RESERVE_FLOAT		**Reserved**: Leave floating.

Pin #	DataSheet Pin Name	Type	Connections/ Comments
101	IO_VSS	Ground	**I/O Ground**: Connect to ground plane.
102	IO_V_{DD}	Power	**I/O 3.3V Supply**: Bypass to pin 101 using a 0.1 µF capacitor.
103	RESERVE_FLOAT		**Reserved**: Leave floating.
104	SI		**SI**: Leave floating.
105	SO		**SO**: Leave floating.
106	RESERVE_FLOAT		**Reserved**: Leave floating.
107	RESERVE_FLOAT		**Reserved**: Leave floating.
108	IO_VSS	Ground	**I/O Ground**: Connect to ground plane.
109	IO_V_{DD}	Power	**I/O 3.3V Supply**: Bypass to pin 108 using a 0.1 µF capacitor.
110	COL	Output	**Collision**: Connect to MAC chip through a single 50 Ω impedance trace. This output is capable of driving 35 pF load and is not intended to drive connectors, cables, backplanes or multiple traces. This applies if the part is in 100 Mb/s mode or 1000 Mb/s mode.
111	CRS	Output	**Carrier Sense**: Connect to MAC chip through a single 50Ω impedance trace. This output is capable of driving 35 pf load and is not intended to drive connectors, cables, backplanes or multiple traces. This applies if the part is in 100 Mb/s mode or 1000 Mb/s mode.
112	RX_ER	Output	**Receive Error/Receive Data 9**: Connect to MAC chip through a single 50 Ω impedance trace. This output is capable of driving 35 pf load and is not intended to drive connectors, cables, backplanes or multiple traces. This applies if the part is in 100 Mb/s mode or 1000 Mb/s mode.
113	RX_DV	Output	**Receive Data Valid/Receive Data 8**: Connect to MAC chip through a single 50 Ω impedance trace. This output is capable of driving 35 pf load and is not intended to drive connectors, cables, backplanes or multiple traces. This applies if the part is in 100 Mb/s mode or 1000 Mb/s mode.
114	RXD7	Output	**Receive Data 7:** Connect to MAC chip through a single 50 Ω impedance trace. This output is capable of driving 35 pf load and is not intended to drive connectors, cables, backplanes or multiple traces. This applies if the part is in 100 Mb/s mode or 1000 Mb/s mode.
115	RXD6	Output	**Receive Data 6:** Connect to MAC chip through a single 50 Ω impedance trace. This output is capable of driving 35 pf load and is not intended to drive connectors, cables, backplanes or multiple traces. This applies if the part is in 100 Mb/s mode or 1000 Mb/s mode.
116	IO_VSS	Ground	**I/O Ground**: Connect to ground plane.
117	IO_V_{DD}	Power	**I/O 3.3V Supply**: Bypass to pin 116 using a 0.1 µF capacitor.

Pin #	DataSheet Pin Name	Type	Connections/ Comments
118	RXD5	Output	**Receive Data 5:** Connect to MAC chip through a single 50 Ω impedance trace. This output is capable of driving 35 pf load and is not intended to drive connectors, cables, backplanes or multiple traces. This applies if the part is in 100 Mb/s mode or 1000 Mb/s mode.
119	RXD4	Output	**Receive Data 4:** Connect to MAC chip through a single 50 Ω impedance trace. This output is capable of driving 35 pf load and is not intended to drive connectors, cables, backplanes or multiple traces. This applies if the part is in 100 Mb/s mode or 1000 Mb/s mode.
120	RXD3	Output	**Receive Data 3:** Connect to MAC chip through a single 50 Ω impedance trace. This output is capable of driving 35 pf load and is not intended to drive connectors, cables, backplanes or multiple traces. This applies if the part is in 100 Mb/s mode or 1000 Mb/s mode.
121	RXD2	Output	**Receive Data 2:** Connect to MAC chip through a single 50 Ω impedance trace. This output is capable of driving 35 pf load and is not intended to drive connectors, cables, backplanes or multiple traces. This applies if the part is in 100 Mb/s mode or 1000 Mb/s mode.
122	IO_VSS	Ground	**I/O Ground**: Connect to ground plane.
123	IO_V_{DD}	Power	**I/O 3.3V Supply**: Bypass to pin 122 using a 0.1 µF capacitor.
124	RXD1	Output	**Receive Data 1:** Connect to MAC chip through a single 50 Ω impedance trace. This output is capable of driving 35 pf load and is not intended to drive connectors, cables, backplanes or multiple traces. This applies if the part is in 100 Mb/s mode or 1000 Mb/s mode.
125	RXD0	Output	**Receive Data 0:** Connect to MAC chip through a single 50 Ω impedance trace. This output is capable of driving 35 pf load and is not intended to drive connectors, cables, backplanes or multiple traces. This applies if the part is in 100 Mb/s mode or 1000 Mb/s mode.
126	RX_CLK	Output	**Receive Clock/ Receive Byte Clock 1**: Connect to MAC chip through a single 50 Ω impedance trace. This output is capable of driving 35 pf load and is not intended to drive connectors, cables, backplanes or multiple traces. This applies if the part is in 100 Mb/s mode or 1000 Mb/s mode.
127	CORE_SUB	Ground	**Digital Core Substrate**: Connect to ground plane.
128	CORE_VSS	Ground	**Digital Core Ground**: Connect to ground plane.
129	CORE_V_{DD}	Power	**Digital Core 1.8 V Supply**: Bypass to pin 128 using a 0.1 µF capacitor.
130	TX_CLK	Output	**Transmit Clock/Receive Byte Clock 0**: Connect to MAC chip through a single 50 Ω impedance trace. This input has a typical input capacitance of 6 pF.
131	IO_VSS	Ground	**I/O Ground**: Connect to ground plane.
132	IO_V_{DD}	Power	**I/O 3.3V Supply**: Bypass to pin 131 using a 0.1 µF capacitor.

Pin #	DataSheet Pin Name	Type	Connections/ Comments
133	TX_ER	Input	**Transmit Error/Transmit Data 9**: Connect to MAC chip through a single 50 Ω impedance trace. This input has a typical input capacitance of 6 pF.
134	TX_EN Inp	ut	**Transmit Enable/Transmit Data 9**: Connect to MAC chip through a single 50 Ω impedance trace. This input has a typical input capacitance of 6 pF.
135	TXD7	Input	**Transmit Data 7**: Connect to MAC chip through a single 50 Ω impedance trace. This input has a typical input capacitance of 6 pF.
136	CORE_VSS	Ground	**Digital Core Ground**: Connect to ground plane.
137	CORE_V_{DD}	Power	**Digital Core 1.8 V Supply**: Bypass to pin 136 using a 0.1 µF capacitor.
138	TXD6	Input	**Transmit Data 6**: Connect to MAC chip through a single 50 Ω impedance trace. This input has a typical input capacitance of 6 pF
139	TXD5	Input	**Transmit Data 5**: Connect to MAC chip through a single 50 Ω impedance trace. This input has a typical input capacitance of 6 pF
140	TXD4	Input	**Transmit Data 4**: Connect to MAC chip through a single 50 Ω impedance trace. This input has a typical input capacitance of 6 pF
141	TXD3	Input	**Transmit Data 3**: Connect to MAC chip through a single 50 Ω impedance trace. This input has a typical input capacitance of 6 pF
142	IO_VSS	Ground	**I/O Ground**: Connect to ground plane.
143	IO_V_{DD}	Power	**I/O 3.3V Supply**: Bypass to pin 142 using a 0.1 µF capacitor.
144	TXD2	Input	**Transmit Data 2**: Connect to MAC chip through a single 50 Ω impedance trace. This input has a typical input capacitance of 6 pF
145	TXD1	Input	**Transmit Data 1**: Connect to MAC chip through a single 50 Ω impedance trace. This input has a typical input capacitance of 6 pF
146	TXD0	Input	**Transmit Data 0**: Connect to MAC chip through a single 50 Ω impedance trace. This input has a typical input capacitance of 6 pF
147	GTX_CLK	Input	**GMII Transmit Clock**: Connect to MAC chip through a single 50 Ω impedance trace. This input has a typical input capacitance of 6 pF
148	IO_VSS	Ground	**I/O Ground**: Connect to ground plane.
149	IO_V_{DD}	Power	**I/O 3.3V Supply**: Bypass to pin 148 using a 0.1 µF capacitor.
150	MDIO	I/O	**Management Data I/O**: Pull-up to VCC with a 1.54 kΩ resistor.
151	MDC	Input	**Management Data Clock**: Connect to MAC or controller using a 50 Ω impedance trace.

Pin #	DataSheet Pin Name	Type	Connections/ Comments
152	OSC_VSS	Ground	**Oscillator Ground**: Connect to ground plane.
153	REF_CLK	Input	**Reference Clock**: Connect to oscillator or crystal or board clock.
154	REF_SEL	Input	**Reference Select**: Pulled high to 3.3 V supply through a 2 KΩ resistor or tied directly to a 3.3 V supply for 125 MHz operation. Pull low for 25 MHz operation.
155	OSC_V_{DD}	Power	**Oscillator 3.3V Supply**: Bypass to pin 152 using a 0.1 µF capacitor.
156	$\overline{TRST}$	Input	**JTAG Test Reset**: If not used connect to ground plane.
157	TDI	Input	**JTAG Test Data Input:** If not used connect to ground plane.
158	TDO	Output	**JTAG Test Data Output**: If not used leave floating.
159	TMS	Input	**JTAG Test Mode Select:** If not used connect to ground plane.
160	CORE_V_{DD}	Power	**Digital Core 1.8 V Supply**: Bypass to pin 161 using a 0.1 µF capacitor.
161	CORE_VSS	Ground	**Digital Core Ground**: Connect to ground plane.
162	CORE_SUB	Ground	**Digital Core Substrate**: Connect to ground plane.
163	TCK	Input	**JTAG Test Clock**: If not used connect to ground plane.
164	$\overline{RESET}$	Input	**Reset**: Connect to board reset signal.
165	RESERVE_GND		**Reserved**: Pull-down to ground plane.
166	RESERVE_GND		**Reserved**: Pull-down to ground plane.
167	IO_V_{DD}	Power	**I/O 3.3V Supply**: Bypass to pin 168 using a 0.1 µF capacitor.
168	IO_VSS	Ground	**I/O Ground**: Connect to ground plane.
169	RESERVE_GND		**Reserved**: Pull-down to ground plane.
170	RESERVE_GND		**Reserved**: Pull-down to ground plane.
171	CORE_V_{DD}	Power	**Digital Core 1.8 V Supply**: Bypass to pin 172 using a 0.1 µF capacitor.
172	CORE_VSS	Ground	**Digital Core Ground**: Connect to ground plane.
173	CORE_SUB	Ground	**Digital Core Substrate**: Connect to ground plane.
174	RESERVE_GND		**Reserved**: Pull-down to ground plane.
175	RESERVE_GND		**Reserved**: Pull-down to ground plane.
176	RESERVE_GND		**Reserved**: Pull-down to ground plane.
177	RESERVE_GND		**Reserved**: Pull-down to ground plane.
178	IO_V_{DD}	Power	**I/O 3.3V Supply**: Bypass to pin 179 using a 0.1 µF capacitor.
179	IO_VSS	Ground	**I/O Ground**: Connect to ground plane.

Pin #	DataSheet Pin Name	Type	Connections/ Comments
180	LED_10/10_ADV/SPEED [1]	I/O, Strap	**LED_10:** See Figure 5 for how to connect this pin.
181	LED_100/100_ADV	I/O, Strap	**LED_100**: See Figure 5 for how to connect this pin.
182	CORE_V_{DD}	Power	**Digital Core 1.8 V Supply**: Bypass to pin 183 using a 0.1 µF capacitor.
183	CORE_VSS	Ground	**Digital Core Ground**: Connect to ground plane.
184	LED_1000/ 1000FDX_ADV	I/O, Strap	**LED_1000:** See Figure 5 for how to connect this pin. (If this pin is strapped low, then pin 192 should be strapped high.)
185	LED_DUPLEX/ 1000HDX_ADV	I/O, Strap	**LED_DUPLEX**: See Figure 5 for how to connect this pin.
186	TEST		**Special pin:** Pull-up to VCC.
187	IO_V_{DD}	Power	**I/O 3.3V Supply**: Bypass to pin 188 using a 0.1 µF capacitor.
188	IO_VSS	Ground	**I/O Ground**: Connect to ground plane.
189	SDA	I/O	**SDA**: This pin should be left floating if the E^2PROM interface is not used. Else see E^2PROM Usage Guide.
190	SCL	I /O	**SCL**: This pin should be left floating if the E^2PROM interface is not used. Else see E^2PROM Usage Guide
191	Manual M/S Advertise	I/O, Strap	**Manual Master/Slave Configuration**: 2 kΩ pull-up or pull-down strap option.
192	AN_EN/TX_TCLK	I/O, Strap	**Auto-Negotiation Enable**: 2 kΩ pull-up or pull-down strap option. (If this pin is strapped low, then pin 184 should be strapped high.)
193	IO_V_{DD}	Power	**I/O 3.3V Supply**: Bypass to pin 194 using a 0.1 µF capacitor.
194	IO_VSS	Ground	**I/O Ground**: Connect to ground plane.
195	Manual_M/S_Enable	I, Strap	**Manual Master/Slave Config Enable**: 2 kΩ pull-up or pull-down strap option.
196	NC_MODE	I/O, Strap	**Non Compliant Mode**: Pull high to inter-operate with non-IEEE compliant transceivers.
197	CORE_V_{DD}	Power	**Digital Core 1.8 V Supply**: Bypass to pin 198 using a 0.1 µF capacitor.
198	CORE_VSS	Ground	**Digital Core Ground**: Connect to ground plane.
199	CORE_SUB	Ground	**Digital Core Substrate**: Connect to ground plane.
200	LED_ACT/PHYAD_0	I/O, Strap	**Activity LED/Phy Address 0**: See Figure 5 for how to connect this pin.
201	LED_COL/PHYAD_1	I/O, Strap	**Collision LED/Phy Address 1**: See Figure 5 for how to connect this pin.
202	IO_V_{DD}	Power	**I/O 3.3V Supply**: Bypass to pin 203 using a 0.1 µF capacitor.

Pin #	DataSheet Pin Name	Type	Connections/ Comments
203	IO_VSS	Ground	**I/O Ground**: Connect to ground plane.
204	LED_LNK/PHYAD_2	I/O, Strap	**Link LED/Phy Address 2**: See Figure 5 on how to connect this pin.
205	LED_TX/PHYAD_3	I/O, Strap	**Transmit LED/Phy Address 3**: See Figure 5 on how to connect this pin.
206	TEST		**Special pin:** Pull-up to VCC
207	LED_RX/PHYAD_4	I/O, Strap	**Receive LED/Phy Address 4**: See Figure 5 on how to connect this pin.
208	SPEED [0]/PORT_TYPE	I/O, Strap	**Speed Select [0] / Port Type**: 2 kΩ pull-up or pull-down strap option.

4.0 Functional Description

The DP83861 is a full featured 10/100/1000 Ethernet Physical layer chip consisting of digital 10/100/1000 Mb/s core which is integrated into a single device with a common TP interface, combined MII/GMII controller interface and Management. interface.

4.1 1000BASE-T Functional Description

The 1000BASE-T transceiver consisting of a PCS Transmitter, PMA Transmitter, PMA Receiver and a PCS Receiver are shown below (Figure 6) in functional block diagram form.

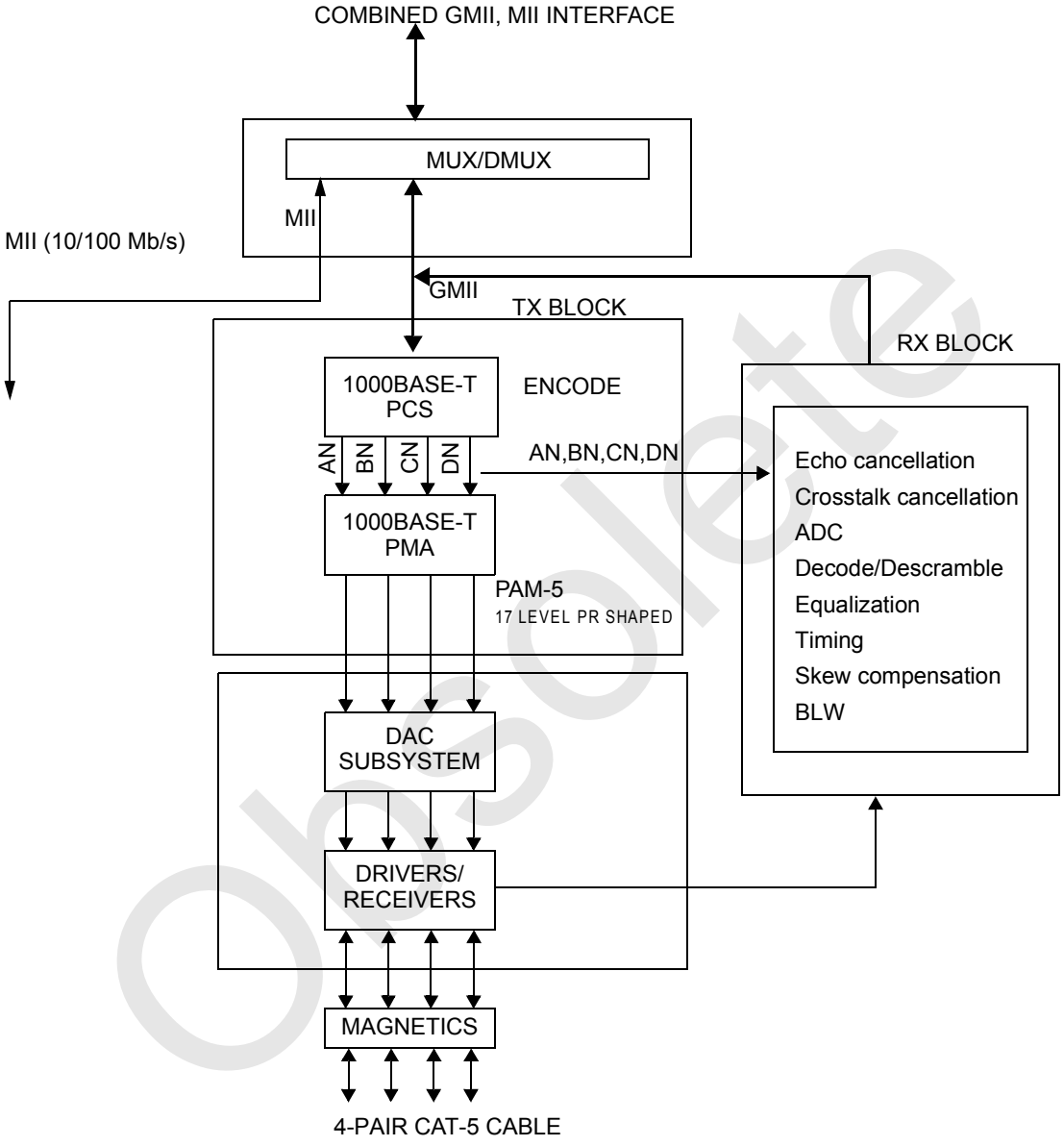


Figure 6. 1000BASE-T Functional Block Diagram

4.2 1000BASE-T PCS TX

The PCS transmitter consists of several functional blocks that convert the 8-bit TXD_n data from the GMII to PAM-5 symbols to be passed onto the PMA (Physical Medium Attachment) function. The block diagram of the PCS transmitter data path functions in Figure 7, provides an overview of each of the functional blocks within the PCS transmitter.

The transmitter consists of eight functional blocks:

— LFSR (Linear Feedback Shift Register)

— Data scrambler and symbol sign scrambler word generator

— Scrambler bit generator

— Data scrambler

— Convolutional encoder

— Bit-to-symbol quinary symbol mapping

— Sign scrambler nibble generator

— Symbol sign scrambler

The requirements for the PCS transmit functionality are also defined in the IEEE 802.3ab specification section 40.3.1.3 “PCS Transmit function”.

4.2.1 Linear Feedback Shift Register (LFSR)

The side-stream scrambler function uses a LFSR implementing one of 2 equations, based on the mode of operation being either a master or a slave. For master operation, the equation is as follows:

$g_M(x) = 1 + x^{13} + x^{33}$

For slave operation, use the equation:

$g_S(x) = 1 + x^{20} + x^{33}$

The 33-bit data output, $Scr_n[32:0]$, of this block is then fed into the data scrambler and symbol sign scrambler word generator.

4.2.2 Data and Symbol Sign Scrambler Word Generator

The word generator uses the $Scr_n[32:0]$ to generate further scrambled values. The following signals are generated: $Sx_n[3:0]$, $Sy_n[3:0]$, and $Sg_n[3:0]$.

The 4-bit $Sx_n[3:0]$ and $Sy_n[3:0]$ values are then fed into the scrambler bit generator. The 4-bit $Sg_n[3:0]$ sign values are fed into the sign scrambler nibble generator.

4.2.3 Scrambler Bit Generator

This function uses the Sx_n and Sy_n signals along with the tx_mode and tx_enable signals to generate the $Sc_n[7:0]$, which is further scrambled based on the condition of the tx_mode and tx_enable signal. The tx_mode signal can indicate sending idles (SEND_I), sending zeros (SEND_Z) or sending idles/data (SEND_N). The tx_mode signal is generated by the micro controller function. The tx_enable signal is either asserted to indicate data transmission is occurring or not asserted for no data transmission. The PCS Data Transmission Enable state machine generates the tx_enable signal.

The 8-bit $Sc_n[7:0]$ signals are then fed into the data scrambler functional block.

4.2.4 Data Scrambler

This function generates scrambled data by accepting the $TxD_n[7:0]$ data from the GMII and scrambling it based on various inputs.

The data scrambler generates the 8-bit $Sd_n[7:0]$ value, which scrambles the TxD_n data based primarily on the Sc_n values and the accompanying control signals.

All 8-bits of $Sd_n[7:0]$ are passed into the bit-to-quinary symbol mapping block, while 2-bits, $Sd_n[7:6]$, are fed into the convolutional encoder.

4.2.5 Convolutional Encoder

The encoder uses $Sd_n[7:6]$ bits and tx_enable to generate an additional data bit, which is called $Sd_n[8]$.

The one clock delayed versions $cs_{n-1}[1:0]$ are passed into the data scrambler functional block. This $Sd_n[8]$ bit is then passed into the bit-to-symbol quinary symbol mapping function.

4.2.6 Bit-to-Symbol Quinary Symbol Mapping

This function implements Table 40-1 and 40-2 Bit-to-Symbol Mapping for even and odd subsets, located in the IEEE 802.3ab specification. It takes the 9-bit $Sd_n[8:0]$ data and converts it to the appropriate quinary symbols as defined by the tables.

The output of this functional block generates the TA_n, TB_n, TC_n, and TD_n symbols, which are then passed into the symbol sign scrambler.

Before describing the symbol sign scrambler, the sign scrambler nibble generator is described, since this also feeds the symbol sign scrambler.

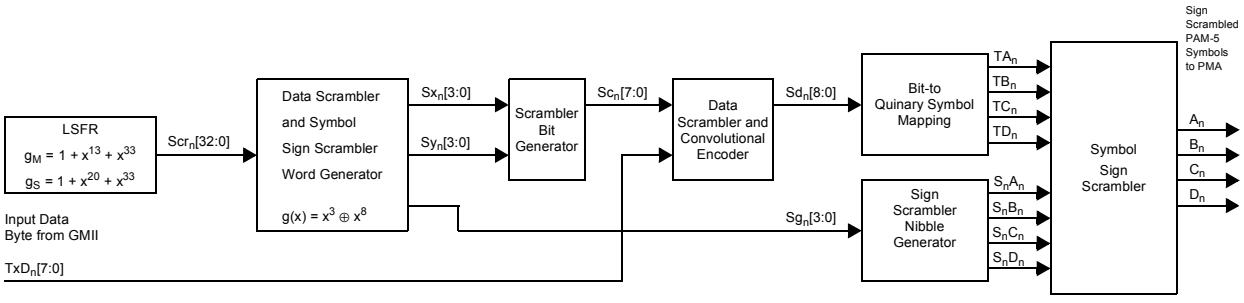


Figure 7. PCS TX Functional Block Diagram

4.2.7 Sign Scrambler Nibble Generator

This function performs some further scrambling of the sign values, $Sg_n[3:0]$, generated by the data scrambler and symbol sign scrambler word generator. This sign scrambling is dependent on the tx_enable signal.

The S_nA_n, S_nB_n, S_nC_n, and S_nD_n outputs are then fed into the symbol sign scrambler function.

4.2.8 Symbol Sign Scrambler

This function scrambles the sign of the TA_n, TB_n, TC_n, and TD_n input values from the bit-to-symbol quinary symbol mapping function, by either inverting or not inverting the signs. This is done as follows:

$A_n = TA_n \times S_nA_n$

$B_n = TB_n \times S_nB_n$

$C_n = TC_n \times S_nC_n$

$D_n = TD_n \times S_nD_n$

The output of this functional block, which are A_n, B_n, C_n, and D_n are the sign scrambled PAM-5 symbols. They are then passed onto the PMA for further processing.

4.3 1000BASE-T PMA TX Block

The PMA transmit block shown in Figure 8 contains the following blocks:

— Partial Response Encoder

— 100/1000 DAC Line Driver

4.3.1 Partial Response Encoder

Partial Response (PR) coding (shaping) is used on the PAM-5 coded signals to spectrally shape the transmitted PAM-5 signal in order to reduce emissions in the critical frequency band ranging from 30 MHz to 60 MHz. The PR Z-transform implemented is:

$0.75 + 0.25\ Z^{-1}$

The result of the PR coding on the PAM-5 signal results in 17-level PAM-5 or PAM-17 signal that is used to drive a common 100/1000 DAC and line driver. (Without the PR coding each signal can have 5 levels given by $\pm 1, \pm 0.5$ and 0 V. If all combinations of the 5 levels are used for the present and previous outputs, then a simple table shows that there are 17 unique outputs levels when PR coding is used.)

Figure 8 shows the PMA Transmitter and the embedded PR encoder block with its inputs and outputs. Figure 9 shows the effect on the spectrum of PAM-5 after PR shaping.

4.3.2 10/100/1000 DAC Line Driver

The PAM-17 information from the PR encoder is used to drive a common 10/100/1000 DAC and line driver that converts digital data to suitable analog line voltages.

4.4 PMA Receiver

The PMA Receiver (the "Receiver") consists of several functional blocks that process the four digitized voltage waveforms representing the received quartet of quinary PAM-5 symbols. The DSP processing implemented in the receiver extracts a best estimate of the quartet of quinary symbols originated by the transmitter at the far end of the CAT-5 cable and delivers them to the PCS RX block for further processing. There are four separate Receivers, one for each twisted pair.

The main processing blocks include:

— Adaptive Equalizer

— Echo and Crosstalk Cancellers

— Automatic Gain Control (AGC)

— Baseline Wander (BLW) Correction

— Slicer

4.4.1 Adaptive Equalizer

The Adaptive Equalizer compensates for the cable's non-ideal (i.e., not flat) frequency vs. attenuation characteristics which results in signal distortion. The cable attenuates the higher frequencies more than the lower frequencies, and this attenuation difference must be equalized. The Adaptive Equalizer is a digital filter with tap coefficients continually adapted to minimize the (Mean Square Error) MSE value of the slicer's error signal output. Continuous adaptation of the equalizer coefficients means that the optimum set of coefficients will always be achieved for any given length or quality of cable.

4.4.2 Echo and Crosstalk Cancellers

The Echo and Crosstalk Cancellers cancel the echo and crosstalk produced while transmitting and receiving simultaneously. Echo is produced when the transmitted signal interferes with the received signal on the same wire. Crosstalk is caused by the transmitted signal on each of the other three wire pairs interfering with the receive signal of the fourth wire pair. An Echo and Crosstalk Canceller is needed for each of the wire pairs.

4.4.3 Automatic Gain Control (AGC)

The Automatic Gain Control acts upon the output of the Echo and Crosstalk Cancellers to adjust the receiver gain. Different AGC methods are available within the chip and the optimum one is selected based on the operational state the chip (master, slave, start-up, etc.).

4.4.4 Baseline Wander (BLW) Correction

Baseline wander is the slow variation of the DC level of the incoming signal due to the non-ideal electrical characteristics of the magnetics and the inherent DC component of the transmitted waveform. The BLW correction circuit utilizes the slicer error signal to estimate and then correct for BLW.

4.4.5 Slicer

The Slicer selects the PAM-5 symbol value (+2,+1,0,-1,-2) closest to the voltage input value after the signal has been corrected for line Inter Symbol Interference (ISI), attenuation, echo, crosstalk and BLW.

The slicer produces an error output and symbol value decision output. The error output is the difference between the actual voltage input and the ideal voltage level representing the symbol value. The error output is fed back to the BLW, AGC, Crosstalk Canceller and Echo Canceller blocks to be used in their respective algorithms.

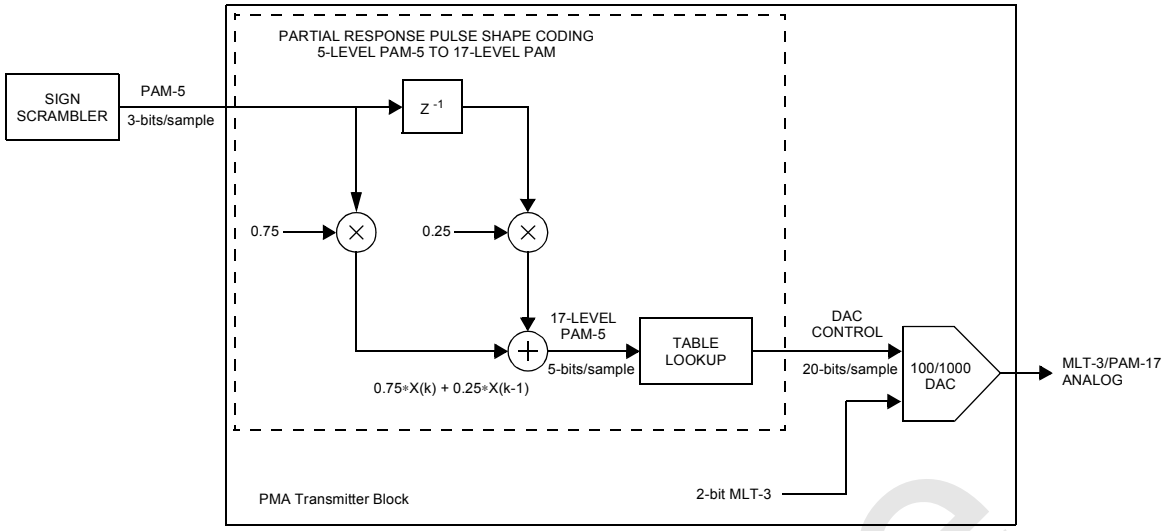


Figure 8. PMA Transmitter Block

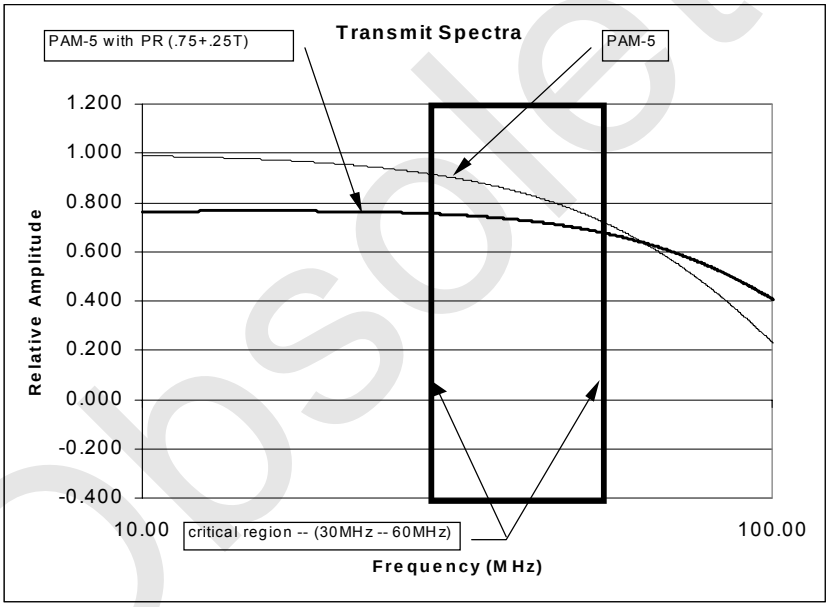


Figure 9. Effect on Spectrum of PR-shaped PAM-5 coding

4.5 1000BASE-T PCS RX

The PCS receiver consists of several functional blocks that convert the incoming quartet of quinary symbols (PAM-5) data from the PMA RX A, B, C, and D to 8-bit receive data (RXD[7:0]), data valid (RX_DV), and receive error (RX_ER) signals on the GMII. The block diagram of the 1000BASE-T Functional Block in Figure 6 provides an overview of the 1000BASE-T transceiver and shows the functionality of the PCS receiver.

The major functional blocks of the PCS Receiver include:

— Delay Skew Compensation

— Delay Skew Control

— Forward Error Correction (FEC)

— Descrambler Subsystem

— Receive State Machine

The requirements for the PCS receive functionality are also defined in the IEEE 802.3ab specification in section 40.3.1.4 “PCS Receive function”.

4.5.1 Delay Skew Compensation

This function is used to align the received data from the four PMA receivers and to determine the correct spacial ordering of the four incoming twisted pairs, i.e., which twisted pair carries A_n, which one carries B_n, etc. The de-skewed and ordered symbols are then presented to the Forward Error Correction (FEC) Decoder. The differential time or time delay skew is due to the differences in length of each of the four pairs of twisted wire in the CAT-5 cable, manufacturing variation of the insulation of the wire pairs,

and in some cases, differences in insulation materials used in the wire pairs. Correct symbol order to the FEC is required, since the receiver does not have prior knowledge of the order of the incoming twisted pairs within the CAT-5 cable.

4.5.2 Delay Skew Control

This function controls the delay skew compensation function by providing the necessary controls and selects to allow for compensation in two dimensions. The two dimensions being time and position. The time factor is the delay skew between the four incoming data streams from the PMA RX A, B, C, and D. This delay skew originates back at the input to the ADC/DAC/TIMING subsystem. Since the receiver initially does not know the ordering of the twisted pairs, correct ordering must be determined automatically by the receiver during start-up. Delay skew compensation and twisted pair ordering is part of the training function performed during start-up mode of operation.

4.5.3 Forward Error Correction (FEC) Decoder

This function decodes the quartet of quinary symbols from the PMA receivers and generates the Sd_n binary values. The FEC decoder uses a standard 8 state Trellis code operation.

The FEC decoder decodes the quartet of quinary (PAM-5) symbols and generates the corresponding Sd_n binary words. Initially, $Sd_n[3:0]$ may not have the proper bit ordering, however, correct ordering is established by the reordering algorithm at start-up.

4.5.4 Descrambler Subsystem

The descrambler block performs the reverse scrambling function that was implemented in the transmit section. This function works in conjunction with the delay skew control. It provides the receiver generated $Sd_n[3:0]$ bits for comparison in the delay skew control function.

4.5.5 Receive State Machine

This state machine operation is defined in IEEE 802.3ab section 40.3.1.4. In summary, it provides the necessary receive control signals of RX_DV and RX_ER to the GMII. In specific conditions, as defined in the IEEE 802.3ab specification, it will generate RXD[7:0] data.

4.6 Gigabit MII (GMII)

The Gigabit Media Independent Interface (GMII) is intended for use between Ethernet PHYs and Station Management (STA) entities and is selected by either hardware or software configuration. The purpose of this interface is to differentiate between the various media that are transparent to the MAC layer.

The GMII Interface accepts either GMII or MII data, control and status signals and routes them either to the 1000BASE-T, 100BASE-TX, or 10BASE-T modules, respectively.

The mapping between GMII and MII is illustrated in Table 4.

Table 15. GMII/MII Mapping

GMII	MII
RXD[3:0]	RXD[3:0]
RXD[4:7]	
RX_DV	RX_DV
RX_ER	RX_ER
RX_CLK	RX_CLK
	TX_CLK
TXD[3:0]	TXD[3:0]
TXD[4:7]	
TX_EN	TX_EN
TX_ER	TX_ER
GTX_CLK	
COL	COL
CRS	CRS

The GMII interface has the following characteristics:

— Supports 10/100/1000 Mb/s operation

— Data and delimiters are synchronous to clock references

— Provides independent 8-bit wide transmit and receive data paths

— Provides a simple management interface

— Uses signal levels that are compatible with common CMOS digital ASIC processes and some bipolar processes

— Provides for Full Duplex operation

The GMII interface is defined in the IEEE 802.3z document Clause 35. In each direction of data transfer, there are Data (an eight-bit bundle), Delimiter, Error, and Clock signals. GMII signals are defined such that an implementation may multiplex most GMII signals with the similar PCS service interface defined in IEEE 802.3u Clause 22.

Two media status signals are provided. One indicates the presence of carrier (CRS), and the other indicates the occurrence of a collision (COL). The GMII uses the MII management interface composed of two signals (MDC, MDIO) which provide access to management parameters and services as specified in IEEE 802.3u Clause 22.

The MII signal names have been retained and the functions of most signals are the same, but additional valid combinations of signals have been defined for 1000 Mb/s operation.

The Reconciliation sublayer maps the signal set provided at the GMII to the PLS service primitives provided to the MAC.

4.7 ADC/DAC/Timing Subsystem

The 1000BASE-T receive section consists of 4 channels, each receiving IEEE 802.3ab compliant PAM-5 coded data including Partial Response (PR) shaping at 125 MBaud over a maximum of a 100 m of CAT-5 cable. The 4 pairs of receive input pins are AC coupled through the magnetics to the CAT-5 cable. Each receive pin pair is externally con-

nected to the transmit pairs through 150Ω resistors. Each receive channel consists of a high precision Analog to Digital data converter (ADC) which quantizes the incoming data into a digital word at the rate of 125 Mb/s. The ADC is sampled with an internal clock of 125 MHz which has been recovered from the incoming data stream.

The 1000BASE-T transmit section consists of 4 channels, each transmitting IEEE 802.3ab compliant 17-level PAM-5 data at 125 M symbols/second. The 4 pairs of transmit output pins are AC coupled through the magnetics to the CAT-5 cable. Each transmit pin pair is serially terminated with 47 Ω resistors to match the cable impedance. Each transmit channel consists of a Digital to Analog data converter (DAC) and line driver capable of producing 17 discrete levels corresponding to the PR shaping of a PAM-5 coded data stream. Each DAC is clocked with an internal 125 MHz clock which is derived from the Ref clock in the MASTER mode of operation, and the recovered receive clock in the SLAVE mode of operation.

The DP83861 incorporates a sophisticated Phase Generation Module (PGM) which supports 10 0/1000 modes of operation with an external 125 MHz clock reference (±50 ppm). The PGM module internally generates multiple phases of clocks at various frequencies to support high precision and low jitter clocks for robust data recovery, and to support accurate low jitter transmission of data symbols in the MASTER and SLAVE mode of operation.

4.8 10BASE-T and 100BASE-TX Transmitter

The 10BASE-T and 100BASE-TX transmitter consists of several functional blocks which convert synchronous 4-bit nibble data, as provided by the MII, to a 10 Mb/s MLT signal for 10BASE-T operation or scrambled MLT-3 125 Mb/s serial data stream for 100BASE-TX operation. Since the 10BASE-T and 100BASE-TX transmitters are integrated with the 1000BASE-T, the differential output pins, TD+/– are routed to channel A of the AC coupling magnetics.

The block diagram in Figure 10 provides an overview of each functional block within the 10BASE-T and 100BASE-TX transmit section.

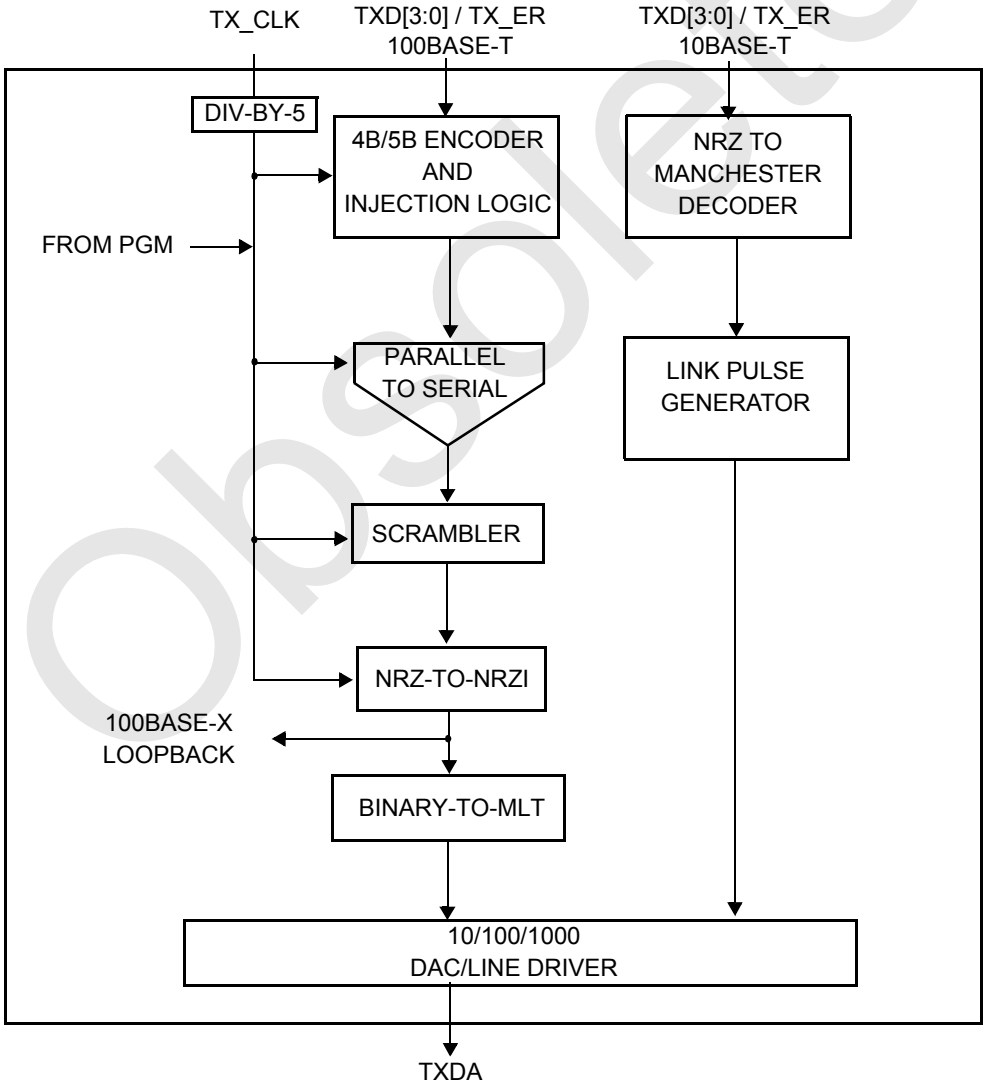


Figure 10. 100BASE-TX Transmit Block Diagram

The Transmitter section consists of the following functional blocks:

10BASE-T BLOCK

— NRZ to Manchester Encoder

— Link Pulse Generator

— DAC / Line Driver

—

100BASE-TX BLOCK

— Code-group Encoder and Injection block

— Parallel-to-Serial block

— Scrambler block

— NRZ to NRZI encoder block

— Binary to MLT-3 converter / DAC / Line Driver

In 10BASE-T mode the transmitter does not meet the IEEE 802.3 specification Clause 14. This specification requires that the the 10 Mb/s output levels are within the following limits:

VOD = 2.2 to 2.8V peak-differential when terminated by a 100Ω resistor directly at the RJ45 outputs. The DP83861 10 Mb/s output levels are typically 1.58V peak differential. In 10 Mb/s operation the DP83861 is able to transmit and receive up to 187 meters of CAT5 cable and over a 100 meters using CAT3 cable. No impact was seen on the receive ability of the link partner due to the reduced levels of VOD.

The DP83861 implements the 100BASE-X transmit state machine diagram as specified in the IEEE 802.3u Standard, Clause 24.

4.8.1 Code-group Encoding and Injection

The code-group encoder converts 4-bit (4B) nibble data generated by the MAC into 5-bit (5B) code-groups for transmission. This conversion is required to allow control data to be combined with packet data code-groups. Refer to Table 5 for 4B to 5B code-group mapping details.

The code-group encoder substitutes the first 8-bits of the MAC preamble with a /J/K/ code-group pair (11000 10001) upon transmission. The code-group encoder continues to replace subsequent 4B preamble and data nibbles with corresponding 5B code-groups. At the end of the transmit packet, upon the deassertion of Transmit Enable signal from the MAC, the code-group encoder injects the /T/R/ code-group pair (01101 00111) indicating the end of frame.

After the /T/R/ code-group pair, the code-group encoder continuously injects IDLEs into the transmit data stream until the next transmit packet is detected (re-assertion of Transmit Enable).

4.8.2 Parallel-to-Serial Converter

The 5-bit (5B) code-groups are then converted to a serial data stream at 125 MHz.

4.8.3 Scrambler

The scrambler is required to control the radiated emissions at the media connector and on the twisted pair cable (for 100BASE-TX applications). By scrambling the data, the total energy launched onto the cable is randomly distributed over a wide frequency range. Without the scrambler, energy levels at the PMD and on the cable could peak beyond FCC limitations at frequencies related to repeating 5B sequences (e.g., continuous transmission of IDLEs).

The scrambler is configured as a closed loop linear feedback shift register (LFSR) with an 11-bit polynomial. The output of the closed loop LFSR is X-ORed with the serial NRZ data from the serializer block. The result is a scrambled data stream with sufficient randomization to decrease radiated emissions at certain frequencies by as much as 20 dB. The DP83861 uses the PHY_ID (pins PHYAD [4:0]) to set a unique seed value for the scramblers. The resulting energy generated by each channel is out of phase with respect to each channel, thus reducing the overall electromagnetic radiation.

4.8.4 NRZ to NRZI Encoder

After the transmit data stream has been serialized and scrambled, the data is NRZI encoded to comply with the TP-PMD standard for 100BASE-TX transmission over Category-5 unshielded twisted pair cable. There is no ability to bypass this block within the DP83861.

Table 16. 4B5B Code-Group Encoding/Decoding

Name	PCS 5B Code-group	MII 4B Nibble Code
DATA CODES		
0	11110	0000
1	01001	0001
2	10100	0010
3	10101	0011
4	01010	0100
5	01011	0101
6	01110	0110
7	01111	0111
8	10010	1000
9	10011	1001
A	10110	1010
B	10111	1011
C	11010	1100
D	11011	1101
E	11100	1110
F	11101	1111
IDLE AND CONTROL CODES		
H	00100	HALT code-group - Error code
I	11111	Inter-Packet IDLE - 0000 (Note 1)
J	11000	First Start of Packet - 0101 (Note 1)
K	10001	Second Start of Packet - 0101 (Note 1)
T	01101	First End of Packet - 0000 (Note 1)
R	00111	Second End of Packet - 0000 (Note 1)
INVALID CODES		
V	00000	0110 or 0101 (Note 2)
V	00001	0110 or 0101 (Note 2)
V	00010	0110 or 0101 (Note 2)
V	00011	0110 or 0101 (Note 2)
V	00101	0110 or 0101 (Note 2)
V	00110	0110 or 0101 (Note 2)
V	01000	0110 or 0101 (Note 2)
V	01100	0110 or 0101 (Note 2)
V	10000	0110 or 0101 (Note 2)
V	11001	0110 or 0101 (Note 2)

Note 1: Control code-groups I, J, K, T and R in data fields will be mapped as invalid codes, together with RX_ER asserted.

Note 2: Normally, invalid codes (V) are mapped to 6h on RXD[3:0] with RX_ER asserted.

4.8.5 MLT-3 Converter / DAC / Line Driver

The Binary to MLT-3 conversion is accomplished by converting the serial NRZI data stream output from the NRZI encoder into two binary data streams with alternately phased logic one events. These two binary streams are then passed to a 100/1000 DAC and line driver which converts the pulses to suitable analog line voltages. Refer to Figure 11.

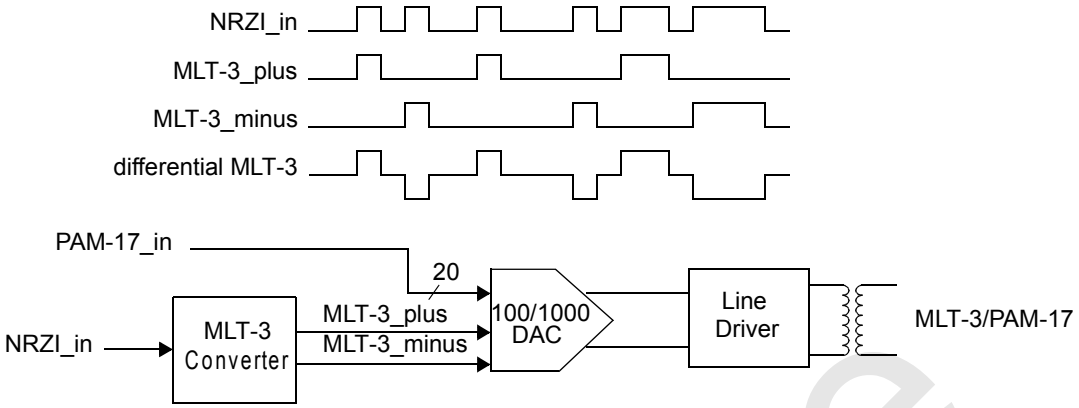


Figure 11. NRZI to MLT-3 Conversion

The 100BASE-TX MLT-3 signal sourced by the TXDA+/– line driver output pins is slew rate controlled. This should be considered when selecting AC coupling magnetics to ensure TP-PMD Standard compliant transition times (3 ns < t_r < 5 ns).

The 100BASE-TX transmit TP-PMD function within the DP83861 is capable of sourcing only MLT-3 encoded data. Binary output from the TXDA+/– outputs is not possible in 100 Mb/s mode.

4.8.6 TX_ER

Assertion of the TX_ER input while the TX_EN input is also asserted will cause the DP83861 to substitute HALT code-groups for the 5B data present at TXD[3:0]. However, the Start-of-Stream Delimiter (SSD) /J /K/ and End-of-Stream Delimiter (ESD) /T/R/ will not be substituted with HALT code-groups. As a result, the assertion of TX_ER while TX_EN is asserted will result in a frame properly encapsulated with the /J/ K/ and /T /R/ delimiters which contains HALT code-groups in place of the data code-groups.

4.9 100BASE-TX Receiver

The 100BASE-TX receiver consists of several functional blocks which convert the scrambled MLT-3 125 Mb/s serial data stream to synchronous 4-bit nibble data that is provided to the MII. Because the 100BASE-TX TP-PMD is integrated with the 1000BASE-T, the differential input data RXDB+/– is routed from channel B of the AC coupling magnetics.

See Figure 12 for a block diagram of the 100BASE-TX receive function. This provides an overview of each functional block within the 100BASE-TX receive section.

The Receive section consists of the following functional blocks:

— ADC Block
— Signal Detect
— BLW/EQ/AAC Correction
— Clock Recovery Module
— MLT-3 to NRZ Decoder
— Descrambler (bypass option)
— Serial to Parallel
— 5B/4B Decoder (bypass option)
— Code Group Alignment
— 4B/5B Decoder
— Link Integrity Monitor
— Bad SSD Detection

4.9.1 ADC Block

The DP83861 requires no external attenuation circuitry at its receive inputs, RXDB+/–. It accepts TP-PMD compliant waveforms directly, requiring only a 100Ω termination plus a simple 1:1 transformer. The analog MLT-3 signal (with noise and system impairments) is received and converted to the digital domain via an Analog to Digital Converter (ADC) to allow for Digital Signal Processing (DSP) to take place on the received signal.

4.9.2 Signal Detect

The signal detect function of the DP83861 is incorporated to meet the specifications mandated by the ANSI FDDI TP-PMD Standard as well as the IEEE 802.3 100BASE-TX Standard for both voltage thresholds and timing parameters.

Note: the reception of fast link pulses per IEEE 802.3u Auto-Negotiation by the 100BASE-X receiver will not cause the DP83861 to assert signal detect.

4.9.3 BLW / EQ / AAC Correction

The digital data from the ADC block flows into the DSP Block (BLW/EQ/AAC Correction) for processing. The DSP block applies proprietary processing algorithms to the received signal and are all part of an integrated DSP receiver. The primary DSP functions applied are:

— BLW can generally be defined as the change in the average DC content, over time, of an AC coupled digital transmission over a given transmission medium. (i.e. copper wire). BLW results from the interaction between the low frequency components of a transmitted bit

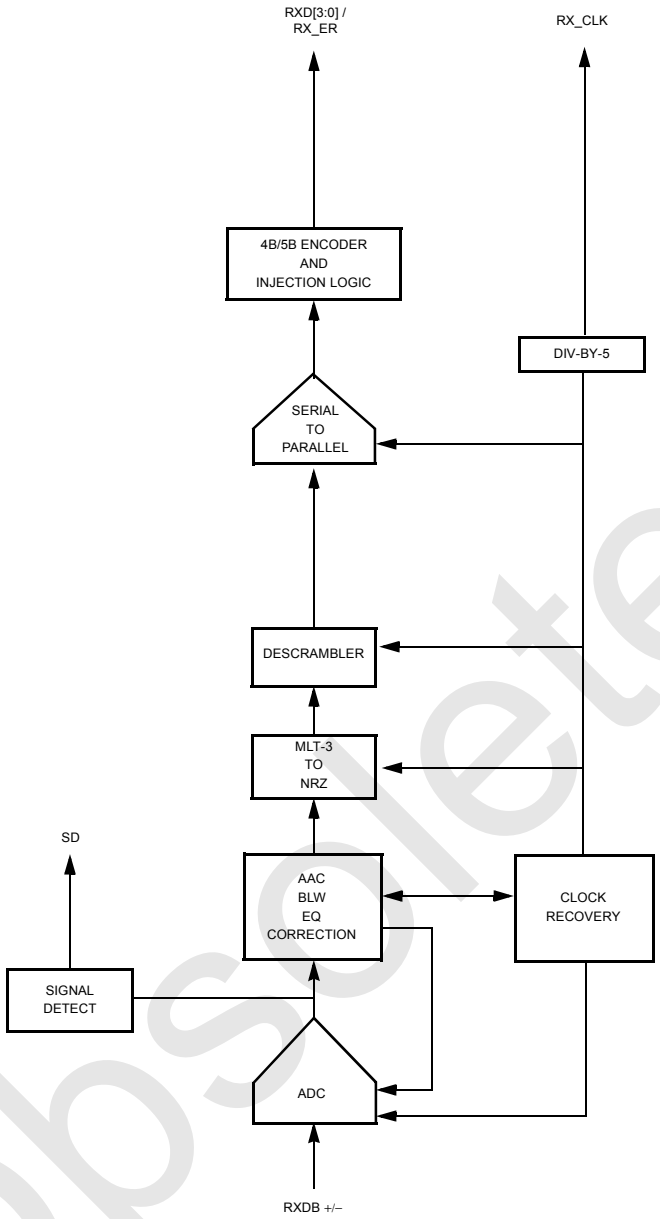


Figure 12. Receive Block Diagram

stream and the frequency response of the AC coupling component(s) within the transmission system. If the low frequency content of the digital bit stream goes below the low frequency pole of the AC coupling transformer then the droop characteristics of the transformer will dominate resulting in potentially serious BLW. The digital oscilloscope plot provided in Figure 13 illustrates the severity of the BLW event that can theoretically be generated during 100BASE-TX packet transmission. This event consists of approximately 800 mV of DC offset for a period of 120 µs. Left uncompensated, events such as this can cause packet loss.

— In high-speed twisted pair signalling, the frequency content of the transmitted signal can vary greatly during normal operation based primarily on the randomness of the scrambled data stream and is thus susceptible to frequency dependent attenuation (see Figure 14). This variation in signal attenuation caused by frequency variations must be compensated for to ensure the integrity of the transmission. In order to ensure quality transmission when using MLT-3 encoding, the compensation must be able to adapt to various cable lengths and cable types depending on the installed environment. The selection of long cable lengths for a given implementation, requires significant compensation which will over-compensate for shorter, less attenuating lengths. Conversely, the selection of short or intermediate cable lengths requiring less compensation will cause serious under-compensation for longer length cables. Therefore, the compensation or equalization must be adaptive to ensure proper conditioning of the received signal independent of the cable length.

— Automatic Attenuation Control (AAC) allows the DSP block to fit the resultant output signal to match the limit characteristic of its internal decision block to ensure error free sampling.

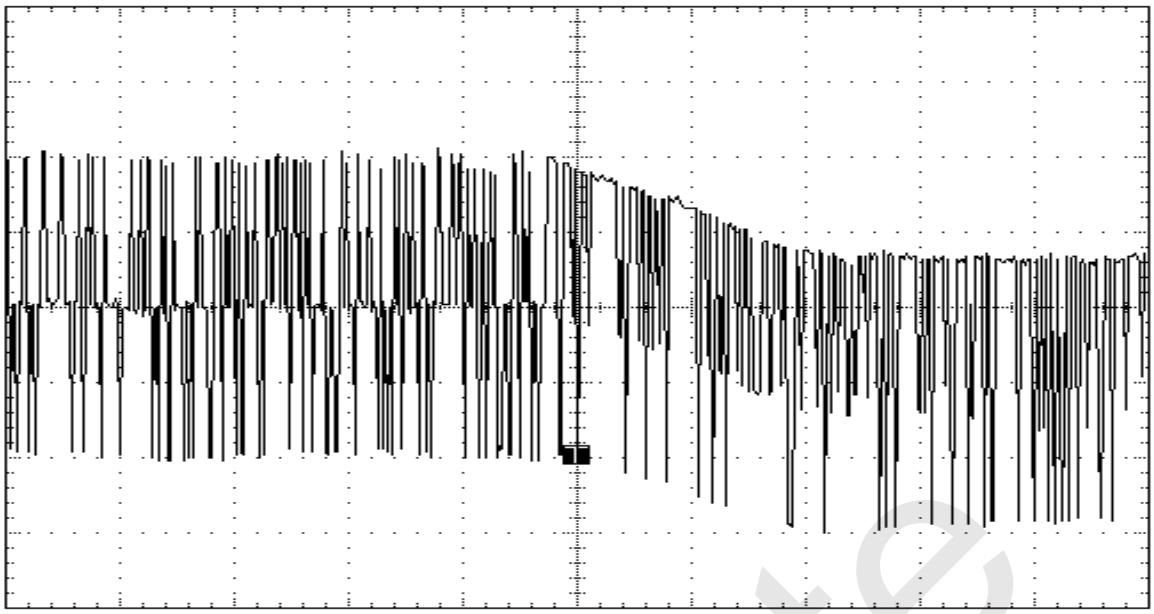


Figure 13. 100BASE-TX BLW Event

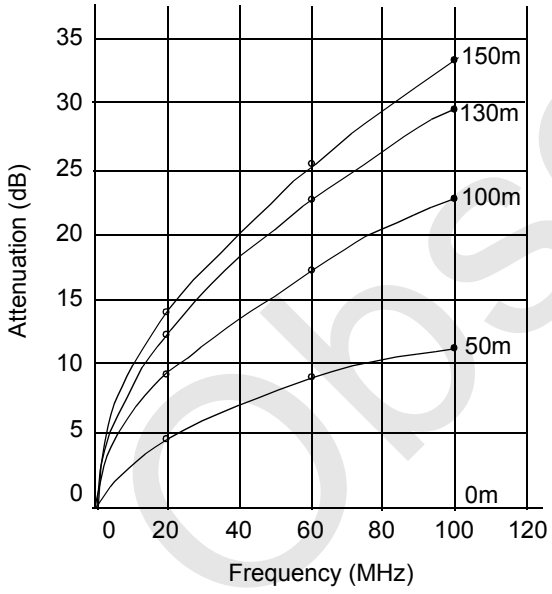


Figure 14. EIA/TIA Attenuation vs. Frequency for 0, 50, 100, 130 & 150 meters of CAT 5 cable

4.9.4 Clock Recovery Module

The Clock Recovery Module (CRM) uses the output information from the DSP Block to generate a phase corrected 125 MHz clock for the 100BASE-T receiver.

The CRM is implemented using an advanced digital Phase Locked Loop (PLL) architecture that replaces sensitive analog circuitry. Using digital PLL circuitry allows the DP83861 to be manufactured and specified to tighter tolerances.

4.9.5 MLT-3 to NRZ Decoder

The DP83861 decodes the MLT-3 information from the DSP block to binary NRZI form and finally to NRZ data.

4.9.6 Descrambler

A serial descrambler is used to de-scramble the received NRZ data. The descrambler has to generate an identical data scrambling sequence (N) in order to recover the original unscrambled data (UD) from the scrambled data (SD) as represented in the equations:

$$SD = (UD \oplus N)$$
$$UD = (SD \oplus N)$$

Synchronization of the descrambler to the original scrambling sequence (N) is achieved based on the knowledge that the incoming scrambled data stream consists of scrambled IDLE data. After the descrambler has recognized 12 consecutive IDLE code-groups, where an unscrambled IDLE code-group in 5B NRZ is equal to five consecutive ones (11111), it will synchronize to the receive data stream and generate unscrambled data in the form of unaligned 5B code-groups.

In order to maintain synchronization, the descrambler must continuously monitor the validity of the unscrambled data that it generates. To ensure this, a line state monitor and a hold timer are used to constantly monitor the synchronization status. Upon synchronization of the descrambler the hold timer starts a 722 µs countdown. Upon detection of sufficient IDLE code-groups (16 idle symbols) within the 722 µs period, the hold timer will reset and begin a new countdown. This monitoring operation will continue indefinitely given a properly operating network connection with good signal integrity. If the line state monitor does not recognize sufficient unscrambled IDLE code-groups within the 722 µs period, the entire descrambler will be forced out of the current state of synchronization and reset in order to reacquire synchronization.

4.9.7 Serial to Parallel Converter

The 100BASE-X receiver includes a Serial to Parallel converter this operation also provides code-group alignment, and operates on unaligned serial data from the descrambler (or, if the descrambler is bypassed, directly from the MLT-3 to NRZ decoder) and converts it into 5B code-group data (5 bits). Code-group alignment occurs after the /J/K/ code-group pair is detected. Once the /J/ K/ code-group pair (11000 10001) is detected, subsequent data is aligned on a fixed boundary.

4.9.8 4B/5B Decoder

The code-group decoder functions as a look up table that translates incoming 5B code-groups into 4B nibbles. The code-group decoder first detects the /J/K/ code-group pair preceded by IDLE code-groups and replaces the /J/K/ with MAC preamble. Specifically, the /J/K/ 10-bit code-group pair is replaced by the nibble pair (0101 0101). All subsequent 5B code-groups are converted to the corresponding 4B nibbles for the duration of the entire packet. This conversion ceases upon the detection of the /T/R/ code-group pair denoting the End of Stream Delimiter (ESD) or with the reception of a minimum of two IDLE code-groups.

4.9.9 100BASE-X Link Integrity Monitor

The 100BASE-X Link monitor ensures that a valid and stable link is established before enabling both the Transmit and Receive PCS layer. Signal Detect must be valid for at least 500 µs to allow the link monitor to enter the “Link Up” state, and enable transmit and receive functions.

4.9.10 Bad SSD Detection

A Bad Start of Stream Delimiter (Bad SSD) is any transition from consecutive idle code-groups to non-idle code-groups which is not prefixed by the code-group pair /J/K/.

If this condition is detected, the DP83861 will assert RX_ER and present RXD[3:0] = 1110 to the MII for the cycles that correspond to received 5B code-groups until at least two IDLE code groups are detected.

Once at least two IDLE code groups are detected, RX_ER and CRS become de-asserted.

4.10 10BASE-T Functional Description

4.10.11 Carrier Sense

Carrier Sense (CRS) may be asserted due to receive activity once valid data is detected via the Smart squelch function.

For 10 Mb/s Half Duplex operation, CRS is asserted during either packet transmission or reception.

For 10 Mb/s Full Duplex operation, CRS is asserted only due to receive activity.

CRS is de-asserted following an end of packet.

4.10.12 Collision Detect and Heartbeat

A collision is detected on the twisted pair cable when the receive and transmit channels are active simultaneously while in Half Duplex mode.

Also after each transmission, the 10 Mb/s block will generate a Heartbeat signal by applying a 1 us pulse on the COL lines which go into the MAC. This signal is called the Signal Quality Error (SQE) and it’s function as defined by IEEE 802.3 is to assure the continued functionality of the collision circuitry.

4.10.13 Link Detector/Generator

The link generator is a timer circuit that generates a link pulse as defined by the 10 Base-T specification that will be sent by the transmitter section. The pulse which is 100ns wide is transmitted on the transmit output, every 16ms, in the absence of transmit data. The pulse is used to check the integrity of the connection to the remote MAU.

The link detection circuit checks for valid pulses from the remote MAU and if valid link pulses are not received the link detector will disable the twisted pair transmitter, receiver and collision detection functions.

4.10.14 Jabber

The Jabber function disables the transmitter if it attempts to transmit a much longer than legal sized packet. The jabber timer monitors the transmitter and disables the transmission if the transmitter is active for greater than 20-30ms. The transmitter is then disabled for the entire time that the ENDEC module's internal transmit is asserted. The transmitter signal has to be de-asserted for approximately 400-600ms (the unjab time) before the Jabber re-enables the transmit outputs.

4.10.15 Transmit Driver

The 10 Mb/s transmit driver in the DP83861, uses the 100/1000 Mb/s common driver.

4.11 ENDEC Module

The ENDEC consists of two major blocks:

— The Manchester encoder accepts NRZ data from the controller, encodes the data to Manchester, and transmits it differentially to the transceiver, through the differential transmit driver.

— The Manchester decoder receives Manchester data from the transceiver, converts it to NRZ data and recovers clock pulses and sends them to the controller.

4.11.16 Manchester Encoder and Differential Driver

The encoder begins operation when the Transmit Enable input (TXE) goes high and converts the clock and NRZ data to Manchester data for the transceiver. For the duration of TXE remaining high, the Transmit Data (TXD) is encoded for the transmit-driver pair (TX±). TXD must be valid on the rising edge of Transmit Clock (TXC). Transmission ends when TXE goes low. The last transition is always positive; it occurs at the center of the bit cell if the last bit is a one, or at the end of the bit cell if the last bit is a zero.

4.11.17 Manchester Decoder

The decoder consists of a differential receiver and a PLL to separate the Manchester encoded data stream into internal clock signals and data. Once the input exceeds the squelch requirements, Carrier Sense (CRS) is asserted off the first edge presented to the decoder. Once the decoder has locked onto the incoming data stream, it provides data (RXD) and clock (RXC) to the MAC.

The decoder detects the end of a frame when no more mid-bit transitions are detected. Typically, within one and a half bit times after the last bit, carrier sense is de-asserted. Receive clock stays active for at least five more bit times after CRS goes low, to guarantee the receive timings of the controller.

4.12 802.3u MII

The DP83861 incorporates the Media Independent Interface (MII) as specified in Clause 22 of the IEEE 802.3u standard. This interface may be used to connect PHY devices to a MAC in 10/100 Mb/s mode. This section describes both the serial MII management interface as well as the nibble wide MII data interface.

The serial management interface of the MII allows for the configuration and control of multiple PHY devices, gathering of status, error information, and the determination of the type and capabilities of the attached PHY(s).

The nibble wide MII data interface consists of a receive bus and a transmit bus each with control signals to facilitate data transfer between the PHY and the upper layer (MAC).

4.12.1 Serial Management Register Access

The serial management MII specification defines a set of thirty-two 16-bit status and control registers that are accessible through the management interface pins MDC and MDIO for both 10/100/1000 Mb/s operation. The DP83861 implements all the required MII registers as well as several optional registers. These registers are fully described in Section 3. A description of the serial management access protocol follows.

4.12.2 Serial Management Access Protocol

The serial control interface consists of two pins, Management Data Clock (MDC) and Management Data Input/Output (MDIO). MDC has a maximum clock rate of 2.5 MHz and no minimum rate. The MDIO line is bi-directional and may be shared by up to 32 devices. The MDIO frame format is shown below in Table 6.

The MDIO pin requires a pull-up resistor (1.5 kΩ) which, during IDLE and turnaround, will pull MDIO high. In order to initialize the MDIO interface, the station management entity sends a sequence of 32 contiguous logic ones on MDIO to provide the DP83861 with a sequence that can be used to establish synchronization. This preamble may be generated either by driving MDIO high for 32 consecutive MDC clock cycles, or by simply allowing the MDIO pull-up resistor to pull the MDIO pin high during which time 32 MDC clock cycles are provided. In addition 32 MDC clock cycles should be used to re-sync the device if an invalid start, op code, or turnaround bit is detected.

The DP83861 waits until it has received this preamble sequence before responding to any other transaction. Once the DP83861 serial management port has been initialized no further preamble sequencing is required until after a power-on/reset, invalid Start, invalid Opcode, or invalid turnaround bit has occurred.

The Start code is indicated by a <01> pattern. This assures the MDIO line transitions from the default idle line state.

Turnaround is defined as an idle bit time inserted between the Register Address field and the Data field. To avoid contention during a read transaction, no device shall actively drive the MDIO signal during the first bit of Turnaround. The addressed DP83861 drives the MDIO with a zero for the second bit of turnaround and follows this with the required data. Figure 15 shows the timing relationship between MDC and the MDIO as driven/received by the Station (STA) and the DP83861 (PHY) for a typical register read access.

Table 17. Typical MDIO Frame Format

MII Management Serial Protocol	<idle><start><op code><device addr><reg addr><turnaround><data><idle>
Read Operation	<idle><01><10><AAAAA><RRRRR><Z0><xxxx xxxx xxxx xxxx><idle>
Write Operation	<idle><01><01><AAAAA><RRRRR><10><xxxx xxxx xxxx xxxx><idle>

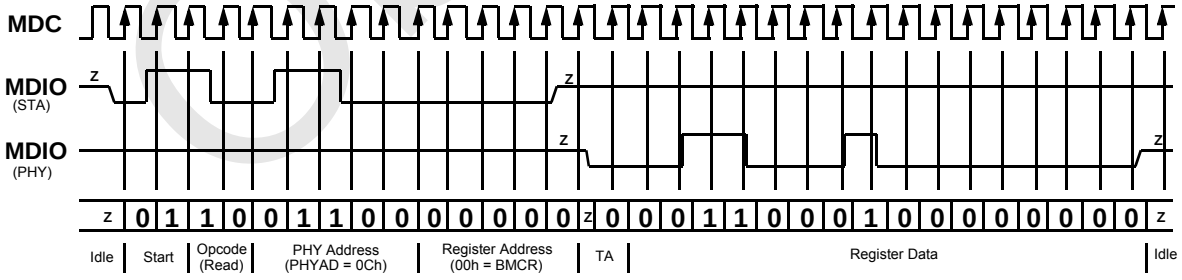


Figure 15. Typical MDC/MDIO Read Operation

For write transactions, the station management entity writes data to the addressed DP83861 thus eliminating the requirement for MDIO Turnaround. The Turnaround time is filled by the management entity by inserting <10>. Figure 16 shows the timing relationship for a typical MII register write access.

4.12.3 Serial Management Preamble Suppression

The DP83861 supports a Preamble Suppression mode as indicated by a one in bit 6 of the Basic Mode Status Register (BMSR, address 01h.) If the station management entity (i.e., MAC or other management controller) determines that all PHYs in the system support Preamble Suppression by returning a one in this bit, then the station management entity need not generate preamble for each management transaction.

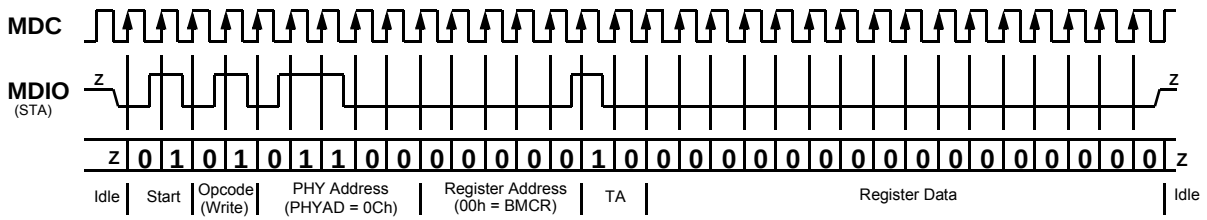


Figure 16. Typical MDC/MDIO Write Operation

The DP83861 requires a single initialization sequence of 32 bits of preamble following power-up/hardware reset. This requirement is generally met by the mandatory pull-up resistor on MDIO in conjunction with a continuous MDC, or the management access made to determine whether Preamble Suppression is supported.

While the DP83861 requires an initial preamble sequence of 32 bits for management initialization, it does not require a full 32-bit sequence between each subsequent transaction. A *minimum of one idle bit between management transactions is required* as specified in IEEE 802.3u.

4.12.4 PHY Address Sensing

The DP83861 provides five PHY address pins, the information is latched into the ECTLR1 register (address 10h, bits [10:6]) at device power-up/reset. The DP83861 supports PHY Address strapping values 0 (<00 000>) through 31 (<11111>). PHY Address 0 puts the part into Isolate Mode.

4.12.5 Nibble-wide MII Data Interface

Clause 22 of the IEEE 802.3u specification defines the Media Independent Interface. This interface includes a dedicated receive bus and a dedicated transmit bus. These two data buses, along with various control and indicate signals, allow for the simultaneous exchange of data between the DP83861 and the upper layer agent (MAC).

The receive interface consists of a nibble wide data bus RXD[3:0], a receive error signal RX_ER, a receive data valid flag RX_DV, and a receive clock RX_CLK for synchronous transfer of the data. The receive clock operates at 25 MHz to support 100 Mb/s operation.

The transmit interface consists of a nibble wide data bus TXD[3:0], a transmit error flag TX_ER, a transmit enable control signal TX_EN, and a transmit clock TX_CLK operates at 25 MHz.

Additionally, the MII includes the carrier sense signal CRS, as well as a collision detect signal COL. The CRS signal asserts to indicate the reception of data from the network or as a function of transmit data in Half Duplex mode. The COL signal asserts as an indication of a collision which can occur during Half Duplex operation when both a transmit and receive operation occur simultaneously.

4.12.6 Collision Detect

For Half Duplex, a 10/100BASE-TX collision is detected when the receive and transmit channels are active simultaneously. Collisions are reported by the COL signal on the MII.

4.12.7 Carrier Sense

Carrier Sense (CRS) may be asserted during 10/100 Mb/s operation when a valid link (SD) and two non-contiguous zeros are detected on the line.

For 10/100 Mb/s Half Duplex operation, CRS is asserted during either packet transmission or reception.

For 10/100 Mb/s Full Duplex operation, CRS is asserted only due to receive activity.

CRS is deasserted following an end of packet.

4.12.8 MII Isolate Mode

The DP83861 can be set to Isolate Mode by setting bit 10 in the BASIC MODE Control Register (00h) to 1.

With bit 10 in the BMCR set to one, the DP83861 does not respond to packet data present at TXD[3:0], TX_EN, and TX_ER inputs and presents a high impedance on the TX_CLK, RX_CLK, RX_DV, RX_ER, RXD[3:0], COL, and CRS outputs. The DP83861 will continue to respond to all serial management transactions over the MDIO/MDC lines.

While in Isolate mode, the TXD+/– outputs are dependent on the current state of Auto-Negotiation. The DP83861 can Auto-Negotiate or parallel detect to a specific technology depending on the receive signal at the RXD+/– inputs. A valid link can be established for RXD even when the DP83861 is in Isolate mode.

It is recommended that the user have a basic understanding of Clause 22 of the 802.3u standard.

4.13 Status Information

There are 9 pins that are available to convey status information to the user through LEDs. The 9 pins indicate link status, collision status, duplex status, activity, device speed indication, and separate indications for Receive (RX) and transmit (TX) for the device.

1) LED_LNK status indicates Good Link Status for 10BASE-T, 100BASE-TX and 1000BASE-T.

10BASE-T: Link is established by detecting Normal Link Pulses separated by 16 ms or by receiving a valid packet.

100BASE-T: Link is established as a result of an input receive amplitude compliant with TP-PMD specifications which will result in internal generation of Signal Detect. LED_LNK will assert after the internal Signal Detect has remained asserted for a minimum of 500 µs. LED_LNK will de-assert immediately following the de-assertion of the internal Signal Detect.

1000BASE-T: Link is established by completing Auto-Negotiation completing (establishing who is the Master and who is the Slave), successfully completing the Training state (final convergence of the adaptive filter parameters) and both the rem_rcvr_status and loc_rcvr_status = OK.

2) LED_COL status indicates that the PHY has detected a collision condition (simultaneous transmit and receive activity while in Half Duplex mode).

3) LED_ACT status indicates Receive or Transmit activity.

4) LED_10 status indicates that the device has established a 10BASE_T link.

5) LED_100 status indicates that the device has established a 100BASE-T link.

6) LED_1000 status indicates that the device has established a 1000BASE-T link.

7) LED_TX status indicates that the PHY is transmitting.

8) LED_RX status indicates that the PHY is receiving.

9) LED_DUPLEX status indicates that the PHY is in Full-Duplex mode of operation.

4.0 Register Block

4.1 Register Definitions

Register maps and address definitions are given in the following tables:

Table 18. Register Block - DP83861 Register Map

Offset		Access	Tag	Description
Hex	Decimal			
0x00	0	RW	BMCR	Basic Mode Control Register
0x01	1	RO	BMSR	Basic Mode Status Register
0x02	2	RO	PHYIDR1	PHY Identifier Register #1
0x03	3	RO	PHYIDR2	PHY Identifier Register #2
0x04	4	RW	ANAR	Auto-Negotiation Advertisement Register
0x05	5	RW	ANLPAR	Auto-Negotiation Link Partner Ability Register
0x06	6	RW	ANER	Auto-Negotiation Expansion Register
0x07	7	RW	ANNPTR	Auto-Negotiation Next Page TX
0x08	8	RW	ANNPRR	Auto-Negotiation Next Page RX
0x09	9	RW	1KTCR	1000BASE-T Control Register
0x0A	10	RO	1KSTSR	1000BASE-T Status Register
0x0B-0x0E	11-14	RO	Reserved	Reserved
0x0F	15	RO	1KSCR	1000BASE-T Extended Status Register
0x10	16	RW	Strap_Reg	Strap Options Register
0x11	17	RO	PHY_SUP	PHY Support
0x12-0x14	18-20	RO	Reserved	Reserved
0x15	21	RW	MDIX_sel	MDIX select
0x16	22	RW	Expand_mem	Expanded Memory Access
0x17-0x1C	23-28	RO	Reserved	Reserved
0x1D	29	RW	Exp_mem_dat	Expanded Memory Data
0x1E	30	RW	Exp_mem_add	Expanded Memory Address
0x1F	31	RO	Reserved	Reserved

Table 19. Extended Register Map

Offset	Access	Tag	Description
Hex			
0x810D	RO	ISR0	Interrupt Status Register 0
0x810E	RO	ISR1	Interrupt Status Register 1
0x810F	RO	IRR0	Interrupt Reason Register 0
0x8110	RO	IRR1	Interrupt Reason Register 1
0x8111	RO	RRR0	Interrupt Raw Reason Register 0
0x8112	RO	RRR1	Interrupt Raw Reason Register 1
0x8113	RW	IER0	Interrupt Enable Register 0
0x8114	RW	IER1	Interrupt Enable Register 1
0x8115	RW	ICLR0	Interrupt Clear Register 0
0x8116	RW	ICLR1	Interrupt Clear Register 1

Offset Hex	Access	Tag	Description
0x8117	RW	ICTR	Interrupt Control Register
0x8118	RW	AN_THRESH	An_threshold Value Register
0x8119	RW	LINK_THRESH	Link_threshold Value Register
0x811A	RW	IEC_THRESH	IEC_threshold Value Register

In the register definitions under the 'Default' heading, the following definitions hold true:

— RW = **R**ead **W**rite access
— RO = **R**ead **O**nly access
— L(H) = **L**atched and **H**eld until read, based upon the occurrence of the corresponding event
— SC = Register sets on event occurrence and **S**elf-**C**lears when event ends
— P = Register bit is **P**ermanently set to a default value
— COR = **C**lear **O**n **R**ead
— Strap[x] = Default value read from **Strap**ped value at device pin at Reset, where x may take the values:
[0] internal pull-down
[1] internal pull-up
[Z] no internal pull-up or pull-down, floating

4.2 Register Map

Register Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Register 0 (0x00) Basic Mode Control Register (BMCR)	Reset 0	Loopback 0	Speed [0] Selection Strap / 1 Strap / 1	Auto-Neg Enable Strap / 1 Strap / 1	Power Down 0	Isolate 0	Restart Auto-Neg 0	Duplex Mode Strap / 1	Collision Test 0	Speed[1] Selection Strap / 1 Strap / 1	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
Register 1 (0x01) Basic Mode Status Register (BMSR)	100BASE-T4 0	100BASE-TX Full-Duplex 1	100BASE-TX Half-Duplex 1	10BASE-T Full-Duplex 0	10BASE-T Half-Duplex 0	100BASE-T2 Full-Duplex 0	100BASE-T2 Half-Duplex 0	1000BASE-T Ext'd Status 1	Reserved 0	Preamble Suppression 1	Auto-Neg Complete 0	Remote Fault 0	Auto-Neg Ability 1	Link Status 0	Jabber Detect 0	Extended Capability 1
Register 2 (0x02) PHY Identifier Register #1 (PHYIDR1)	OUI_MSB[15] 0	OUI_MSB[14] 0	OUI_MSB[13] 1	OUI_MSB[12] 0	OUI_MSB[11] 0	OUI_MSB[10] 0	OUI_MSB[9] 0	OUI_MSB[8] 0	OUI_MSB[7] 0	OUI_MSB[6] 0	OUI_MSB[5] 0	OUI_MSB[4] 0	OUI_MSB[3] 0	OUI_MSB[2] 0	OUI_MSB[1] 0	OUI_MSB[0] 0
Register 3 (0x03) PHY Identifier Register #2 (PHYIDR2)	OUI_LSB[15] 0	OUI_LSB[14] 1	OUI_LSB[13] 0	OUI_LSB[12] 1	OUI_LSB[11] 1	OUI_LSB[10] 1	VMDR_MDL[5] 0	VMDR_MDL[4] 0	VMDR_MDL[3] 0	VMDR_MDL[2] 1	VMDR_MDL[1] 1	VMDR_MDL[0] 0	MDL_REV[3] 0	MDL_REV[2] 0	MDL_REV[1] 0	MDL_REV[0] 1
Register 4 (0x04) Auto-Neg Advertisement Register (ANAR)	Next Page 1	Reserved 0	Remote Fault 0	Reserved 0	ASY_PAUSE 0	PAUSE 0	T4 0	TX_FD 1	TX_HD 1	10_FD 0	10_HD 0	PSB[4] 0	PSB[3] 0	PSB[2] 0	PSB[1] 0	PSB[0] 1
Register 5 (0x05) Auto-Neg Link Partner Ability Register (ANLPAR)	Next Page 0	ACK 0	Remote Fault 0	Reserved 0	ASY_PAUSE 0	PAUSE 0	T4 0	100_TX_FD 0	100_TX 0	10_FD 0	10 0	PSB[4] 0	PSB[3] 0	PSB[2] 0	PSB[1] 0	PSB[0] 0
Register 6 (0x06) Auto-Neg Expansion Register (ANER)	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	PDF 0	LP_NP Able 0	NP_Able 1	Page _RX 0	LP_AN Able 0
Register 7 (0x07) Auto-Neg NP TX Register (ANNPTR)	Next Page 1	Reserved 0	Message Page 1	ACK2 0	TOG_TX 0	NP_M[10] 0	NP_M[9] 0	NP_M[8] 0	NP_M[7] 0	NP_M[6] 0	NP_M[5] 0	NP_M[4] 0	NP_M[3] 1	NP_M[2] 0	NP_M[1] 0	NP_M[0] 0
Register 8 (0x08) Auto-Neg NP RX Register (ANNPRR)	Next Page 0	Reserved 0	Message Page 0	ACK3 0	TOG_RX 0	NP_M[10] 0	NP_M[9] 0	NP_M[8] 0	NP_M[7] 0	NP_M[6] 0	NP_M[5] 0	NP_M[4] 0	NP_M[3] 0	NP_M[2] 0	NP_M[1] 0	NP_M[0] 0
Register 9 (0x09) 1000BASE-T Control Register (1KTCR)	Test Mode[1] 0	Test Mode[2] 0	Test Mode[3] 0	Manual Master/Slave Enable Strap / 0	Manual Master/Slave Advertise Strap / 0	Port_Type 0	1000BASE-T Full-Duplex 1	1000BASE-T Half-Duplex 1	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
Register 10 (0x0A) 1000BASE-T Status Register (1KSTSR)	Master/Slave Manual Config Fault 0	Config. Resolved to Master 0	Local Receiver Status 0	Remote Receiver Status 0	LP1000T FD 0	LP 1000T 0	ASM_DIR 0	Reserved 0	Idle Error Count 0	Idle Error Count 0	Idle Error Count 0	Idle Error Count 0	Idle Error Count 0	Idle Error Count 0	Idle Error Count 0	Idle Error Count 0
Register 15 (0x0F) 1000BASE-T Extended Status Register (1KSCR)	1000BASE-X Full-Duplex 0	1000BASE-X Half-Duplex 0	1000BASE-T Full-Duplex 1	1000BASE-T Half-Duplex 1	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
Register 16 (0x10) Strap Option Register (Strap_reg)	PHY_ADD [4] Strap [0]	PHY_ADD [3] Strap [0]	PHY_ADD [2] Strap [0]	PHY_ADD [1] Strap [0]	PHY_ADD [0] Strap [1]	NC_MODE Strap [0]	M/S Manual Strap [0]	AN_Ena Strap [1]	M/S value Strap [0]	Reserved 0	Reserved 0	1000HDX_ ADV Strap [0]	1000FDX_ ADV Strap [1]	100FDX_HDX Strap [1]	Sel_Speed [1] Strap [0]	Sel_Speed [0] Strap [0]
Register 17(0x11) PHY Support Register (PHY_SUP)	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Speed_Res [1] 0	Speed_Res [0] 0	Link_Res 0	Duplex_Res 0	Reserved 0

Key: Bit Name / Read/Writable / Default Value — Bit Name / Read Only / Value

Table 20. Basic Mode Control Register (BMCR) address 0x00

Bit	Bit Name	Default	Description
15	Reset	0, RW, SC	**Reset:** 1 = Initiate software Reset / Reset in Process. 0 = Normal operation. This bit sets the status and control registers of the PHY to their default states. This bit, which is self-clearing, returns a value of one until the reset process is complete (approximately 1.2 ms for reset duration). Reset is finished once the Auto-Negotiation process has begun or the device has entered it's forced mode.
14	Loopback	0, RW	**Loopback:** 1 = Loopback enabled. 0 = Normal operation. The loopback function enables MII/GMII transmit data to be routed to the MII/GMII receive data path. Setting this bit may cause the descrambler to lose synchronization and produce a 500 µs "dead time" before any valid data will appear at the MII receive outputs in 100 Mb/s operation.
13	Speed[0]	Strap Pin 208 0, RW	**Speed Select:** When Auto-Negotiation is disabled, bits 6 and 13 select device speed selection per table below: Speed[1] Speed[0] Speed Enabled 1 1 = eserved R 1 0 = 1000 Mb/s 0 1 = 100 Mb/s 0 0 = 10 Mb/s The default value of this bit is = to the strap value of pin 208 during reset/power-on IF the AN_EN is low.
12	AN_ENable	Strap Pin 192 1, RW	**Auto-Negotiation Enable:** 1 = Auto-Negotiation Enabled - bits 6, 8 and 13 of this register are ignored when this bit is set. 0 = Auto-Negotiation Disabled - bits 6, 8 and 13 determine the link speed and mode.
11	Power_Down	0, RW	**Power Down:** 1 = Power down (only Management Interface and logic active.) 0 = Normal operation.
10	Isolate	0, RW	**Isolate:** 1 = Isolates the Port from the MII with the exception of the serial management. When this bit is asserted, the DP83861 does not respond to TXD[3:0], TX_EN, and TX_ER inputs, and it presents a high impedance on TX_CLK, RX_CLK, RX_DV, RX_ER, RXD[3:0], COL and CRS outputs. 0 = Normal operation.
9	Restart_AN	0, RW, SC	**Restart Auto-Negotiation:** 1 = Restart Auto-Negotiation. Re-initiates the Auto-Negotiation process. If Auto-Negotiation is disabled (bit 12 = 0), this bit is ignored. This bit is self-clearing and will return a value of 1 until Auto-Negotiation is initiated, whereupon it will self-clear. Operation of the Auto-Negotiation process is not affected by the management entity clearing this bit. 0 = Normal operation.

Table 20. Basic Mode Control Register (BMCR) address 0x00

Bit	Bit Name	Default	Description
8	Duplex	Strap Pin 185 1, RW	**Duplex Mode:** 1 = Full Duplex operation. Duplex selection is allowed only when Auto-Negotiation is disabled (bit 12 = 0). 0 = Half Duplex operation.
7	Collision Test	0, RW	**Collision Test:** 1 = Collision test enabled. 0 = Normal operation. When set, this bit will cause the COL signal to be asserted in response to the assertion of TX_EN within 512-bit times. The COL signal will be de-asserted within 4-bit times in response to the de-assertion of TX_EN.
6	Speed[1]	Strap Pin 180 0, RW	**Speed Select:** See description for bit 13. The default value of this bit is = to the strap value during reset/power-on IF the AN_EN is low.
5:0	Reserved	0, RO	**Reserved by IEEE:** Write ignored, read as 0.

Table 21. Basic Mode Status Register (BMSR) address 0x01

15	100BASE-T4	0, RO	**100BASE-T4 Capable:** 1 = Device able to perform 100BASE-T4 mode. 0 = Device not able to perform 100BASE-T4 mode. DP83861 does not support 100BASE-T4 mode and bit should always be read back as “0”.
14	100BASE-TX Full Duplex	1, RO	**100BASE-TX Full Duplex Capable:** 1 = Device able to perform 100BASE-TX in Half Duplex mode. 0 = Device unable to perform 100BASE-TX in Half Duplex mode.
13	100BASE-TX Half Duplex	1, RO	**100BASE-TX Half Duplex Capable:** 1 = Device able to perform 100BASE-TX in Half Duplex mode. 0 = Device unable to perform 100BASE-TX in Half Duplex mode.
12	10BASE-T Full Duplex	0, RO	**10BASE-T Full Duplex Capable:** 1 = Device able to perform 10BASE-T in Half Duplex mode. 0 = Device unable to perform 10BASE-T in Half Duplex mode.
11	10BASE-T Half Duplex	0, RO	**10BASE-T Half Duplex Capable:** 1 = Device able to perform 10BASE-T in Half Duplex mode. 0 = Device unable to perform 10BASE-T in Half Duplex mode. .
10	100BASE-T2 Full Duplex	0, RO	**100BASE-T2 Full Duplex Capable:** 1 = Device able to perform 100BASE-T2 Full Duplex mode. 0 = Device unable to perform 100BASE-T2 Full Duplex mode. DP83861 does not support 100BASE-T2 mode and bit should always be read back as “0”.
9	100BASE-T2 Half Duplex	0, RO	**100BASE-T2 Half Duplex Capable:** 1 = Device able to perform 100BASE-T2 Half Duplex mode. 0 = Device unable to perform 100BASE-T2 Full Duplex mode. DP83861 does not support 100BASE-T2 mode and bit should always be read back as “0”.

Table 21. Basic Mode Status Register (BMSR) address 0x01

8	1000BASE-T Extended Status	1, RO	**1000BASE-T Extended Status Register:** 1 = Device supports Extended Status Register 0x0F (15). 0 = Device does not supports Extended Status Register 0x0F (15).
7	Reserved	0, RO	**Reserved by IEEE:** Write ignored, read as 0.
6	Preamble Suppression	1, RO	**Preamble suppression Capable:** 1 = Device able to perform management transaction with preamble suppressed, 32-bits of preamble needed only once after reset, invalid opcode or invalid turnaround.
5	Auto-Negotiation Complete	0, RO	**Auto-Negotiation Complete:** 1 = Auto-Negotiation process complete, and contents of registers 0x05, 0x06, 0x07, & 0x08 are valid. 0 = Auto-Negotiation process not complete.
4	Remote Fault	0, RO	**Remote Fault:** 1 = Remote Fault condition detected (cleared on read or by reset). Fault criteria: Far End Fault Indication or notification from Link Partner of Remote Fault. 0 = No remote fault condition detected.
3	Auto-Negotiation Ability	1, RO	**Auto Configuration Ability:** 1 = Device is able to perform Auto-Negotiation. 0 = Device is not able to perform Auto-Negotiation.
2	Link Status	0, RO	**Link Lost Since Last Read Status:** 1 = Link was good since last read of this register. (10/100/1000 Mb/s operation). 0 = Link was lost since last read of this register. The occurrence of a link failure condition will causes the Link Status bit to clear. Once cleared, this bit may only be set by establishing a good link condition and a read via the management interface. This bit doesn't indicate the link status, but rather if the link was lost since last read. For actual link status, either this register should be read twice, or register 0x11 bit 2 should be read.
1	Jabber Detect	0, RO	**Jabber Detect:** Set to 1 if 10BASE-T Jabber detected locally. 1 = Jabber condition detected. 0 = No Jabber.
0	Extended Capability	1, RO	**Extended Capability:** 1 = Extended register capable.

The PHY Identifier Registers #1 and #2 together form a unique identifier for the DP83861. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), the vendor's model number and the model revision number. A PHY may return a value of zero in each of the 32 bits of the PHY Identifier if desired. The PHY Identifier is intended to support network management. National's IEEE assigned OUI is 080017h.

Table 22. PHY Identifier Register #1 (PHYIDR1) address 0x02

Bit	Bit Name	Default	Description
15:0	OUI_MSB	<0010_0000_0000_0000>, RO	**OUI Most Significant Bits**: Bits 3 to 18 of the OUI (080017h) are stored in bits 15 to 0 of this register. The most significant two bits of the OUI are ignored (the IEEE standard refers to these as bits 1 and 2).

Table 23. PHY Identifier Resister #2 (PHYIDR2) address 0x03

Bit	Bit Name	Default	Description
15:10	OUI_LSB	<01_0111>, RO	**OUI Least Significant Bits:** Bits 19 to 24 of the OUI (080017h) are mapped to bits 15 to 10 of this register respectively.
9:4	VNDR_MDL	6'b <00_0110>, RO	**Vendor Model Number:** The six bits of vendor model number are mapped to bits 9 to 4 (most significant bit to bit 9).
3:0	MDL_REV	4'b <0001>, RO	**Model Revision Number:** Four bits of the vendor model revision number are mapped to bits 3 to 0 (most significant bit to bit 3). This field will be incremented for all major device changes.

This register contains the advertised abilities of this device as they will be transmitted to its link partner during Auto-Negotiation.

Table 24. Auto-Negotiation Advertisement Register (ANAR) address 0x04

Bit	Bit Name	Default	Description
15	NP	**0, RO**	**Next Page Indication:** 1 = Next Page Transfer desired. 0 = Next Page Transfer not desired. **Does not conform to IEEE specs. See Section 7.3**
14	Reserved	0, RO	**Reserved by IEEE:** Writes ignored, Read as 0.
13	RF	0, RO	**Remote Fault:** 1 = Advertises that this device has detected a Remote Fault. 0 = No Remote Fault detected.
12	Reserved	0, RO	**Reserved for Future IEEE use:** Write as 0, Read as 0.
11	ASY_PAUSE	0, RO	**Asymmetrical PAUSE:** 1 = MAC/Controller supports Asymmetrical Pause direction. 0 = MAC/Controller does not support Asymmetrical Pause direction. **Does not conform to IEEE specs. See Section 7.2**
10	PAUSE	0, RW	**PAUSE:** 1 = MAC/Controller supports Pause frames. 0 = MAC/Controller does not support Pause frames.
9	T4	0, O	**100BASE-T4 Support:** 0 = No support for 100BASE-T4.
8	TX_FD	Strap Pin 181 1, RW	**100BASE-TX Full Duplex Support:** 1 = 100BASE-TX Full Duplex is supported by the local device. 0 = 100BASE-TX Full Duplex not supported. The default value of this bit is = to the strap value during reset/power-on, If the AN_EN is high.
7	TX_HD	Strap Pin 181 1, RW	**100BASE-TX Support:** 1 = 100BASE-TX is supported by the local device. 0 = 100BASE-TX not supported. The default value of this bit is = to the strap value during reset/power-on, If the AN_EN is high.

Table 24. Auto-Negotiation Advertisement Register (ANAR) address 0x04

Bit	Bit Name	Default	Description
6	10_FD	Strap Pin 180 0, RW	**10BASE-T Full Duplex Support:** 1 = 10BASE-T Full Duplex is supported. 0 = 10BASE-T Full Duplex is not supported. The default value of this bit is = to the strap value of during reset/power-on, If the AN_EN is high.
5	10_HD	Strap Pin 180 0, RW	**10BASE-T Support:** 1 = 10BASE-T is supported. 0 = 10BASE-T is not supported.
4:0	PSB	<00001>, RO	**Protocol Selection Bits:** These bits contain the binary encoded protocol selector supported by this port. <00001> indicates that this device supports IEEE 802.3.

This register contains the advertised abilities of the Link Partner as received during Auto-Negotiation.

Table 25. Auto-Negotiation Link Partner Ability Register (ANLPAR) address 0x05

Bit	Bit Name	Default	Description
15	NP	0, RO	**Next Page Indication:** 0 = Link Partner does not desire Next Page Transfer. 1 = Link Partner desires Next Page Transfer.
14	ACK	0, RO	**Acknowledge:** 1 = Link Partner acknowledges reception of the ability data word. 0 = Not acknowledged. The Device's Auto-Negotiation state machine will automatically control the this bit based on the incoming FLP bursts. Software should not attempt to write to this bit.
13	RF	0, RO	**Remote Fault:** 1 = Remote Fault indicated by Link Partner. 0 = No Remote Fault indicated by Link Partner.
12	Reserved	0, RO	**Reserved for Future IEEE use:** Write as 0, read as 0.
11	ASY_PAUSE	0, RO	**Asymmetrical PAUSE:** 1 = Link Partner supports Asymmetrical Pause direction. 0 = Link Partner does not support Asymmetrical Pause direction.
10	PAUSE	0, RO	**PAUSE:** 1 = Link Partner supports Pause frames. 0 = Link Partner does not support Pause frames.
9	T4	0, O	**100BASE-T4 Support:** 1 = 100BASE-T4 is supported by the Link Partner. 0 = 100BASE-T4 not supported by the Link Partner.
8	TX_FD	0, RO	**100BASE-TX Full Duplex Support:** 1 = 100BASE-TX Full Duplex is supported by the Link Partner. 0 = 100BASE-TX Full Duplex not supported by the Link Partner.
7	TX	0, O	**100BASE-TX Support:** 1 = 100BASE-TX is supported by the Link Partner. 0 = 100BASE-TX not supported by the Link Partner.
6	10_FD	0, RO	**10BASE-T Full Duplex Support:** 1 = 10BASE-T Full Duplex is supported by the Link Partner. 0 = 10BASE-T Full Duplex not supported by the Link Partner.

Table 25. Auto-Negotiation Link Partner Ability Register (ANLPAR) address 0x05

Bit	Bit Name	Default	Description
5	10	0, O	**10BASE-T Half Duplex Support:** 1 = 10BASE-T Half Duplex is supported by the Link Partner. 0 = 10BASE-T Half Duplex not supported by the Link Partner.
4:0	PSB	<00000>, RO	**Protocol Selection Bits:** Link Partners's binary encoded protocol selector.

This register contains additional Local Device and Link Partner status information.

Table 26. Auto-Negotiate Expansion Register (ANER) address 0x06

Bit	Bit Name	Default	Description
15:5	Reserved	0, RO	**Reserved by IEEE:** Writes ignored, Read as 0.
4	PDF	0, RO	**Parallel Detection Fault:** 1 = A fault has been detected via the Parallel Detection function. 0 = A fault has not been detected via the Parallel Detection function.
3	LP_NP_ABLE	0, RO	**Link Partner Next Page Able:** 1 = Link Partner does support Next Page. 0 = Link Partner supports Next Page negotiation.
2	NP_ABLE	1, RO	**Next Page Able:** 1 = Indicates local device is able to send additional "Next Pages".
1	PAGE_RX	0, RO	**Link Code Word Page Received:** 1 =Link Code Word has been received, cleared on read of this register. 0 = Link Code Word has not been received.
0	LP_AN_ABLE	0, RO	**Link Partner Auto-Negotiation Able:** 1 = Indicates that the Link Partner supports Auto-Negotiation. 0 = Indicates that the Link Partner does not support Auto-Negotiation.

This register contains the next page information sent by this device to its Link Partner during Auto-Negotiation.

Table 27. Auto-Negotiation Next Page Transmit Register (ANNPTR) address 0x07

Bit	Bit Name	Default	Description
15	NP	1, RW	**Next Page Indication:** 1 = Another Next Page desired. 0 = No other Next Page Transfer desired. **Does not conform to IEEE specifications. See User Info Section for more detail.**
14	Reserved	0, RO	**Reserved by IEEE**: Writes ignored, read as 0.
13	MP	1, RO	**Message Page:** 1 = Message Page. 0 = Unformatted Page.
12	ACK2	0, RO	**Acknowledge2:** 1 = Will comply with message. 0 = Cannot comply with message. Acknowledge2 is used by the next page function to indicate that Local Device has the ability to comply with the message received.

Table 27. Auto-Negotiation Next Page Transmit Register (ANNPTR) address 0x07

Bit	Bit Name	Default	Description
11	TOG_TX	0, RO	**Toggle:** 1 = Value of toggle bit in previously transmitted Link Code Word was logic 0. 0 = Value of toggle bit in previously transmitted Link Code Word was logic 1. Toggle is used by the Arbitration function within Auto-Negotiation to ensure synchronization with the Link Partner during Next Page exchange. This bit shall always take the opposite value of the Toggle bit in the previously exchanged Link Code Word.
10:0	CODE	<000_0000_1000>, RO	This field represents the code field of the next page transmission. If the MP bit is set (bit 13 of this register), then the code shall be interpreted as a "Message Page", as defined in annex 28C of IEEE 802.3u. Otherwise, the code shall be interpreted as an "Unformatted Page", and the interpretation is application specific. The default value of the CODE represents a Null Page as defined in Annex 28C of IEEE 802.3u.

This register contains the next page information sent by this device to its Link Partner during Auto-Negotiation.

Table 28. Auto-Negotiation Next Page Receive Register (ANNPRR) address 0x08

Bit	Bit Name	Default	Description
15	NP	0, RO	**Next Page Indication:** 1 = Another Next Page desired. 0 = No other Next Page Transfer desired.
14	Reserved	0, RO	**Reserved by IEEE**: Writes ignored, read as 0.
13	MP	0, RO	**Message Page:** 1 = Message Page. 0 = Unformatted Page.
12	ACK2	0, RO	**Acknowledge2:** 1 = Will comply with message. 0 = Cannot comply with message. Acknowledge2 is used by the next page function to indicate that Link Partner has the ability to comply with the message received.
11	TOG_TX	0, RO	**Toggle:** 1 = Value of toggle bit in previously transmitted Link Code Word was logic 0. 0 = Value of toggle bit in previously transmitted Link Code Word was logic 1. Toggle is used by the Arbitration function within Auto-Negotiation to ensure synchronization with the Link Partner during Next Page exchange. This bit shall always take the opposite value of the Toggle bit in the previously exchanged Link Code Word.
10:0	CODE	<0000 0000 000>, RO	This field represents the code field of the next page transmission. If the MP bit is set (bit 13 of this register), then the code shall be interpreted as a "Message Page", as defined in annex 28C of IEEE 802.3u. Otherwise, the code shall be interpreted as an "Unformatted Page", and the interpretation is application specific. The default value of the CODE represents a Reserved for future use as defined in Annex 28C of IEEE 802.3u.

Table 29. 1000BASE-T Control Register (1KTCR) address 0x09

Bit	Bit Name	Default	Description
15:13	Test Mode	0, RW	**Test Mode Select:** **bit 15 bit 14 bit 13 Test Mode Selected** 1 0 0 = Test Mode 4 0 1 1 = Test mode 3 0 1 0 = Test Mode 2 0 0 1 = Test Mode 1 0 0 0 = Normal Operation See IEEE 802.3ab section 40.6.1.1.2 “Test modes” for more information. Output for TX_TCLK when in Test Mode is on pin 192.
12	Manual Master/Slave Enable	Strap Pin 195 0,RW	**Enable Manual Master/Slave Configuration:** 1 = Enable Manual Master/Slave Configuration control. 0 = Disable Manual Master/Slave Configuration control. The default value of this bit is = to the strap value during reset/power-on.
11	Manual Master/Slave Advertise	Strap Pin 191 0,RW	**Advertise Master/Slave Configuration Value:** 1 = Advertise PHY as MASTER when register 09h bit 12 = 1. 0 = Advertise PHY as SLAVE when register 09h bit 12 = 1. The default value of this bit is = to the strap value during reset/power-on.
10	Port_Type	Strap Pin 208 0, RO	**Port Type: Multi or single port** 1 = Repeater or Switch (DP83861 does not support Repeater mode). 0 = DTE(NIC). The default value of this bit is = to the strap value during reset/power-on IF the AN_EN pin is high.
9	1000BASE-T Full Duplex	Strap Pin 184 1, RW	**Advertise 1000BASE-T Full Duplex Capable:** 1 = Advertise DTE as 1000BASE-T Full Duplex Capable. 0 = Advertise DTE as not 1000BASE-T Full Duplex Capable. The default value of this bit is = to the strap value during reset/power-on IF the AN_EN pin is high.
8	1000BASE-T Half Duplex	Strap Pin 185 1, RW	**Advertise 1000BASE-T Half Duplex Capable:** 1 = Advertise DTE as 1000BASE-T Half Duplex Capable. 0 = Advertise DTE as not 1000BASE-T Half Duplex Capable. The default value of this bit is = to the strap value during reset/power-on IF the AN_EN pin is high.
7:0	Reserved	0, RW	**Reserved by IEEE:** Writes ignored, Read as 0.

This register provides status for 1000BASE-T link.

Table 30. 1000BASE-T Status Register (1KSTSR) address 0x0A (10’d)

Bit	Bit Name	Default	Description
15	Master-Slave Manual Config Fault	0, RO	**MASTER/SLAVE manual configuration fault detected:** 1 = MASTER/SLAVE manual configuration fault detected. 0 = No MASTER/SLAVE manual configuration fault detected.
14	MS_Config_Results	0, RO	**MASTER SLAVE Configuration Results:** 1 = Configuration resolved to MASTER. 0 = Configuration resolved to SLAVE.

Table 30. 1000BASE-T Status Register (1KSTSR) address 0x0A (10'd)

Bit	Bit Name	Default	Description
13	Local Receiver Status	0, RO	**Local Receiver Status:** 1 = OK. 0 = Not OK.
12	Remote Receiver Status	0, RO	**Remote Receiver Status:** 1 = OK. 0 = Not OK.
11	LP_1000T_FD	0, RO	**Link Partner 1000T Full Duplex:** 1 = Link Partner capable of 1000BASE-T Full Duplex. 0 = Link Partner not capable of 1000BASE-T Full Duplex.
10	LP_1000T_HD	0, RO	**Link Partner 1000T Half Duplex:** 1 = Link Partner capable of 1000BASE-T Half Duplex. 0 = Link Partner not capable of 1000BASE-T Half Duplex.
9	LP_ASM_DIR	0, RO	**Link Partner ASM_DIR Capable:** 1 = Link Partner **Asymmetric Pause Direction** capable. 0 = Link Partner not **Asymmetric Pause Direction** capable.
8	Reserved	0, RO	**Reserved by IEEE:** Write ignored, read as 0.
7:0	IDLE Error Count (MSB)	0, RO	**IDLE Error Count**

Note: Registers 0x0B - 0x0E are Reserved by IEEE.

Table 31. 1000BASE-T Extended Status Register (1KSCR) address 0x0F (15'd)

Bit	Bit Name	Default	Description
15	1000BASE-X_FD	0, RO	**1000BASE-X Full Duplex Support:** 1 = 1000BASE-X is supported by the local device. 0 = 1000BASE-X is not supported. DP83861 does not support 1000BASE-X and bit should always be read back as "0".
14	1000BASE-X _DH	0, RO	**1000BASE-X Half Duplex Support:** 1 = 1000BASE-X is supported by the local device. 0 =1000BASE-X is not supported. DP83861 does not support 1000BASE-X and bit should always be read back as "0".
13	1000BASE-T_FD	1, RO	**1000BASE-T Full Duplex Support:** 1 = 1000BASE-T is supported by the local device. 0 =1000BASE-T is not supported.
12	1000BASE-T_HD	1, RO	**1000BASE-T Half Duplex Support:** 1 = 1000BASE-T is supported by the local device. 0 =1000BASE-T is not supported.
11:0	Reserved	0, RO	**Reserved by IEEE:** Write ignored, read as 0.

The register below summarizes all the strap options.

Table 32. Strap Option Register (Strap_reg) address 0x10 (16'd)

Bit	Bit Name	Default	Description
15:11	PHY_Address 4:0	00001, RO	**PHY Address:** Strap option pins 200, 201, 204, 205, 207. Changeable only through restrapping and resetting the device.
10	NC_MODE value	Strap Pin 196 0, RW	**NON-COMPLIANT Mode:** Strap option NC_MODE (pin 196). 1 = Will Auto-Negotiate to BCM5400 with revision revs prior to rev. C5 and with IEEE 802.3ab compliant PHY's. 0 = Will Auto-Negotiate with IEEE 802.3ab compliant PHY's
9	Manual M/S Enable	Strap Pin 195 0, RO	**Manual Master/Slave Configuration Enable:** Strap option MANUAL_M/S_CFG (pin 195). This value could be overwritten by changing bit 12 of register 0x09.
8	AN enable	Strap Pin 192 1, RO	**Auto-negotiation Enable:** Strap option AN_EN (pin 192). This value could be overwritten by changing bit 12 of register 0x00. However this bit will retain the original strapped value, regardless of changes to bit 12 of register 0x00.
7	Master/Slave value	Strap Pin 191 0, RO	**Master/Slave Value:** Strap option MAS_SLAVE (pin 191). This value could be overwritten by changing bit 11 of register 0x09.
6	Reserved	0, O	**Reserved**
5	Reserved	1, O	**Reserved**
4	1000HDX_ADV value	Strap Pin 185 1, RO	**1000 HDX Advertisement:** Strap option 1000_HDX_ADV (pin 185).
3	1000FDX_ADV value	Strap Pin 184 1, RO	**1000 FDX Advertisement:** Strap option 1000_FDX_ADV (pin 184).
2	100FDX/HDX_ADV	Strap Pin 181 1, RO	**100 FDX and HDX Advertisement:** Strap option 100_ADV (pin 181).
1:0	Sel_Speed 1:0	Strap Pin 180, Strap Pin 208 [00], RO	**Speed Select:** Strap option pins 180 and 208 respectively. This value could be overwritten by changing bits 6 and 13 of register 0x00.

Table 33. PHY Support Register (PHY_Sup) address 0x11 (17'd)

Bit	Bit Name	Default	Description
15:5	Reserved		**Reserved:**
4:3	Speed_Status 1:0	Strap or AN determined value, RW	**Speed Resolved:** These two bits indicate the speed of operation as determined by Auto-negotiation or as set by manual configuration. Speed[1] / Speed[0] / Speed of operation 1 / 0 = 1000 Mb/s 0 / 1 = 100 Mb/s 0 / 0 = 10 Mb/s
2	Link-up_Status	0, RW	**Link status:** '1' indicates that a good link is established '0' indicates no link.
1	Duplex_Status	0, RW	**Duplex status:** '1' indicates that the current mode of operation is Full Duplex. '0' indicates that the current mode of operation is Half Duplex.
0	10BASE-T Resolved	0, RW	**10BASE-T Resolved:** '1' indicates that the current mode of operation is 10BASE-T '0' indicates that the current mode of operation is not 10BASE-T

Table 34. MDIX_sel address 0x15 (21'd)

Bit	Bit Name	Default	Description
15:1	Reserved	0, RW	**Reserved**
0	MDIX_sel	0, RW	**MDIX_sel:** If Auto-MDIX selection is disabled, then this bit can be used to set for either cross-over or straight cable operation when in 1000BASE-T, 100BASE-TX and 10BASE-T mode: 1 = Cross-over channels A and B. (i.e. the cable is straight) 0 = Don't cross-over channels A and B. (i.e. the cable is cross-over)

Table 35. Expand_mem address 0x16 (22'd)

Bit	Bit Name	Default	Description
15:4	Reserved	0, RW	**Expanded Memory Modes:** Allows access to expanded memory and sets the mode of access. Also see registers 0x1D and 0x1E and the FAQ section.
3	Re-Time Management Data	1, RW	**Re-time Management Data:** 1 = Re-time management data to MDC clock domain 0 = Do not re-time management data to MDC clock domain
2	Expanded Memory Access	0, RW	**Expanded Memory Access:** 1 = Enable Expanded Memory Access 0 = Disable Expanded Memory Access
1:0	Address Control	[11], RW	**Address Control:** 00 = Reserve 01 = 8-bit access 10 = 16-bit access 11 = Reserve

Table 36. Exp_mem_data address 0x1D (29'd)

Bit	Bit Name	Default	Description
15:0	Expanded Memory Data	0, RW	**Expanded Memory Data:** Data to be written to or read from expanded memory. Note that in 8-bit mode, the data resides at the LSB octet of this register. See an example in the FAQ section.

Table 37. Exp_mem_add address 0x1E (30'd)

Bit	Bit Name	Default	Description
15:0	Expanded Memory Address	0, RW	**Expanded Memory Address:** Pointer to the address in expanded memory. The pointer is 16-bit wide. See an example in the FAQ section.

The following are expanded memory locations that contains extended register sets to access interrupt status and control functions. These registers are 8-bit wide and accessed through Exp_mem_mode, Exp_mem_data and Exp_mem_addr registers

Table 38. Interrupt_Status ISR0 address 0x810D

Bit	Bit Name	Default, Type	Description
7	isr_an_comp_thresh	0, RO	**AN Counter Reached Threshold:** The Auto-negotiation Counter counts the number of time AN occurs. This bit determines if the counter has reached a preset threshold value. 1 = When COUNTER_AUTONEG > AN_COMP_THRESH 0 = Cleared when corresponding ICLR0 bit 7 is set
6	isr_an_comp	0, RO	1 = When BMSR 0x01 bit 5 an_complete changes 0 = Cleared when corresponding ICLR0 bit 6 is set
5	isr_an_remote_fault	0, RO	1 = When BMSR 0x01 bit 4 an_remote_fault changes 0 =Cleared when corresponding ICLR0 bit 5 is set
4	isr_speed	0, RO	1 = When PHY_Sup 0x11 bit 3 and 4 resolved_speed change state qualified by link up 0 = Cleared when corresponding ICLR0 bit 4 is set
3	isr_link_thresh	0, RO	**Link Counter Reached Threshold:** The Link Counter counts the number of link session. This bit determines if the Link Counter has reached a preset threshold value. 1 = When (COUNTER_LINK_10 + COUNTER_LINK_100 + COUNTER_LINK_1000) > LINK_THRESH 0 = Cleared when corresponding ICLR0 bit 3 is set
2	isr_link	0, RO	1 = When PHY_Sup 0x11 bit 2 resolved_link changes state 0 = Cleared when corresponding ICLR0 bit 2 is set
1	isr_duplex	0, RO	1 = When PHY_Sup 0x11 bit 1 resolved_duplex changes state qualified by link up 0 = Cleared when corresponding ICLR0 bit 1 is set
0	isr_jabber	0, RO	1 = When BMSR 0x01 bit 1 jabber changes state 0 = Cleared when corresponding ICLR0 bit 0 is set

Table 39. Interrupt_Status ISR1 address 0x810E

Bit	Bit Name	Default, Type	Description
7	isr_config_fault	0, RO	1 = When 1KSTSR 0x0A bit 15 config_fault changes state 0 = Cleared when corresponding ICR1 bit is set
6	isr_config	0, RO	1 = When 1KSTSR 0x0A bit 14 config_resolved_to_master changes state qualified by link up 0 = When corresponding ICR1 bit 6 is set
5	isr_loc_rcvr_status	0, RO	1 = When 1KSTSR 0x0A bit 13 1000BT loc_rcvr_status changes state 0 = When corresponding ICR1 bit 5 is set
4	isr_rem_rcvr_status	0, RO	1 = When 1KSTSR 0x0A bit 12 1000BT rem_rcvr_status changes state 0 = When corresponding ICR1 bit 4 is set
3	isr_iec_thresh	0, RO	**Idle Error Counter Reached Threshold:** The Idle Error Counter counts the number of idle error. This bit determines if the IEC has reached a preset threshold value 1 = When 1KSTSR 0x0A bits 0 to 7 idle_error_count > IEC_THRESH 0 = When corresponding ICR1 bit 3 is set
2	isr_fw_ROM	0, RO	1 = Firmware is detected to be running from ROM 0 = Firmware is detected to be running from RAM

Table 39. Interrupt_Status ISR1 address 0x810E

Bit	Bit Name	Default, Type	Description
1	isr_fw_RAM	0, RO	1 = Firmware is detected to be running from RAM 0 = Firmware is detected to be running from ROM
0	isr_reset	1, RO	1= Firmware cycles through the reset sequence 0 = Corresponding bit in ICR1 bit 0 is set

Table 40. Interrupt_Reason IRR0 address 0x810F

Bit	Bit Name	Default, Type	Description
7	Reserved	0, RO, LH	Reserved
6	irr_an_comp	0, RO, LH	Copy of BMSR 0x01 bit 5 an_complete at the time interrupt is asserted
5	irr_an_remote_fault	0, RO, LH	Copy of BMSR 0x01 bit 4 an_remote_fault at the time interrupt is asserted
4:3	irr_speed[1:0]	0, RO, LH	Copy of PHY_Sup 0x11 bits 3 and 4 speed_res at the time interrupt is asserted if link is up
2	irr_link	0, RO, LH	Copy of PHY_Sup 0x11 bit 2 link_res at the time interrupt is asserted
1	irr_duplex	0, RO, LH	Copy of PHY_Sup 0x11 bit 1 duplex_res at the time interrupt is asserted if link is up
0	irr_jabber	0, RO, LH	Copy of BMSR 0x01 bit 1 jabber at the time interrupt is asserted

Table 41. Interrupt_Reason IRR1 address 0x8110

Bit	Bit Name	Default, Type	Description
7	irr_config_fault	0, RO, LH	Copy of 1KSTSR 0x0A bit 15 config_fault at the time interrupt is asserted
6	irr_config	0, RO, LH	Copy of 1KSTSR 0x0A bit 14 an_remote_fault at the time interrupt is asserted if link is up
5	irr_loc_rcvr_status	0, RO, LH	Copy of 1KSTSR 0x0A bit 13 loc_rcvr_status at the time interrupt is asserted
4	irr_rem_rcvr_status	0, RO, LH	Copy of 1KSTSR 0x0A bit 12 rem_rcvr_status at the time interrupt is asserted
3	Reserved	0, RO, LH	Reserved
2	Reserved	0, RO, LH	Reserved
1	Reserved	0, RO, LH	Reserved
0	Reserved	0, RO, LH	Reserved

Table 42. Interrupt_Raw_Reason RRR0 address 0x8111

Bit	Bit Name	Default, Type	Description
7	Reserved	0, RO	Reserved
6	irw_an_comp	0, RO	Current value of BMSR 0x01 bit 5 an_complete
5	irw_an_remote_fault	0, RO	Current value of BMSR 0x01 bit 4 an_remote_fault
4:3	irw_speed[1:0]	0, RO	Current value of PHY_Sup 0x11 bits 3 and 4 speed_res when link is up, else last value of bits 3 and 4 when link was up
2	irw_link	0, RO	Current value of PHY_Sup 0x11 bit 2 link_res
1	irw_duplex	0, RO	Current value of PHY_Sup 0x11 bit 1 duplex_res if link is up, else last value of duplex last time link was up
0	irw_jabber	0, RO	Current value of BMSR 0x01 bit 1 jabber

Table 43. Interrupt_Raw_Reason RRR1 address 0x8112

Bit	Bit Name	Default, Type	Description
7	irw_config_fault	0, RO	Current value of 1KSTSR 0x0A bit 15 config_fault at the time interrupt is asserted
6	irw_config	0, RO	Current value of 1KSTSR 0x0A bit 14 an_remote_fault at the time interrupt is asserted if link is up
5	irw_loc_rcvr_status	0, RO	Current value of 1KSTSR 0x0A bit 13 loc_rcvr_status at the time interrupt is asserted
4	irw_rem_rcvr_status	0, RO	Current value of 1KSTSR 0x0A bit 12 rem_rcvr_status at the time interrupt is asserted
3	Reserved	0, RO	Reserved
2	Reserved	0, RO	Reserved
1	Reserved	0, RO	Reserved
0	Reserved	0, RO	Reserved

Table 44. Interrupt_Enable IER0 address 0x8113

Bit	Bit Name	Default, Type	Description
7	ier_an_comp_thresh	0, RW	1 = Enable isr_an_comp_thresh interrupt 0 = Disable isr_an_comp_thresh interrupt
6	ier_an_comp	0, RW	1 = Enable isr_an_comp interrupt 0 = Disable isr_an_comp interrupt
5	ier_an_remote_fault	0, RW	1 = Enable isr_an_rem_fault interrupt 0 = Disable isr_an_rem_fault interrupt
4	ier_speed	0, RW	1 = Enable isr_speed interrupt 0 = Disable isr_speed interrupt
3	ier_link_thresh	0, RW	1 = Enable isr_link_thresh interrupt 0 = Disable isr_link_thresh interrupt
2	ier_link	0, RW	1 = Enable isr_link interrupt 0 = Disable isr_link interrupt
1	ier_duplex	0, RW	1 = Enable isr_duplex interrupt 0 = Disable isr_duplex interrupt
0	ier_jabber	0, RW	1 = Enable isr_jabber interrupt 0 = Disable isr_jabber interrupt

Table 45. Interrupt_Enable IER1 address 0x8114

Bit	Bit Name	Default, Type	Description
7	Reserved	0, RO	Reserved
6	ier_config	0, RW	1 = Enable isr_config interrupt 0 = Disable isr_config interrupt
5	ier_loc_rcvr_status	0, RW	1 = Enable isr_loc_rcvr_status interrupt 0 = Disable isr_loc_rcvr_status interrupt
4	ier_rem_revr_status	0, RW	1 = Enable isr_rem_revr_status interrupt 0 = Disable isr_rem_revr_status interrupt
3	ier_iec_thresh	0, RW	1 = Enable isr_iec_thresh interrupt 0 = Disable isr_iec_thresh interrupt
2	ier_fw_ROM	0, RW	1 = Enable isr_fw_ROM interrupt 0 = Disable isr_fw_ROM interrupt

Table 45. Interrupt_Enable IER1 address 0x8114

Bit	Bit Name	Default, Type	Description
1	ier_fw_RAM	0, RW	1 = Enable isr_fw_RAM interrupt 0 = Disable isr_fw_RAM interrupt
0	ier_reset	0, RW	1 = Enable isr_reset interrupt 0 = Disable isr_reset interrupt

Table 46. Interrupt_Clear ICLR0 address 0x8115

Bit	Bit Name	Default, Type	Description
7	icr_an_comp_thresh	0, RW, SC	1 = Clear isr_an_comp_thresh interrupt and clear COUNTER_AUTONEG 0 = No action
6	icr_an_comp	0, RW, SC	1 = Clear isr_an_comp interrupt 0 = No action
5	icr_an_remote_fault	0, RW, SC	1 = Clear isr_an_remote_fault interrupt 0 = No action
4	icr_speed	0, RW, SC	1 = Clear isr_speed interrupt 0 = No action
3	icr_link_thresh	0, RW, SC	1 = Clear isr_link_thresh interrupt, clear COUNTER_LINK_10, clear COUNTER_LINK_100, and clear COUNTER_LINK_1000. 0 = No action
2	icr_link	0, RW, SC	1 = Clear isr_link interrupt 0 = No action
1	icr_duplex	0, RW, SC	1 = Clear isr_duplex interrupt 0 = No action
0	icr_jabber	0, RW, SC	1 = Clear isr_jabber interrupt 0 = No action

Table 47. Interrupt_Clear ICLR1 address 0x8116

Bit	Bit Name	Default, Type	Description
7	Reserved	0, RW, SC	Reserved
6	icr_config	0, RW, SC	1 = Clear isr_config interrupt 0 = No action
5	icr_loc_rcvr_status	0, RW, SC	1 = Clear isr_loc_rcvr_status interrupt 0 = No action
4	icr_rem_rcvr_status	0, RW, SC	1 = Clear isr_rem_rcvr_status interrupt 0 = No action
3	icr_iec_thresh	0, RW, SC	1 = Clear isr_iec_thresh interrupt 0 = No action
2	Reserved	0	Reserved
1	Reserved	0	Reserved
0	icr_reset	0, RW, SC	1 = Clear isr_reset interrupt 0 = No action

Table 48. Interrupt_Control ICTR address 0x8117

Bit	Bit Name	Default, Type	Description
7:3	Reserved	0, RW	Reserved
2	ict_mode	0, RW	**Interrupt mode** 1 = Enable interrupt (when LED's are enabled) 0 = Disable interrupt
1	Reserved	0, RW	Reserved
0	ict_polarity	0 RW	**Interrupt polarity** 1 = Active high 0 = Active low

Table 49. AN_THRESH address 0x8118

Bit	Bit Name	Default, Type	Description
7:0	an_comp_thresh[7:0]	0xff, RW	Threshold value used to generate isr_an_comp_thresh

Table 50. LINK_THRESH address 0x8119

Bit	Bit Name	Default, Type	Description
7:0	link_thresh[7:0]	0xff, RW	Threshold value used to generate isr_link_thresh

Table 51. IEC_THRESH address 0x811A

Bit	Bit Name	Default, Type	Description
7:0	iec_thresh[7:0]	0xff, RW	Threshold value used to generate isr_iec_thresh

5.0 Electrical Specifications

Absolute Maximum Ratings

Supply Voltage (V_{DD})	-0.5V to 4.2V
Input Voltage (DC_{IN})	-0.5V to V_{DD} + 0.5V
Output Voltage (DC_{OUT})	-0.5V to V_{DD} + 0.5V
Storage Temperature	-65°C to 150°C
ESD Protection	6000V

Note: *Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.*

Recommended Operating Condition

	Min	Typ	Max	Units
Supply Voltage I/O, Analog	3.135	3.3	3.465	V
Supply Voltage Digital Core	1.71	1.8	1.89	
Ambient Temperature (T_A)	0		70	°C
REF_CLK Input Freq. Stability (over temperature)	-50		+50	ppm
REF_CLK Input Jitter pk-pk			200	ps
REF_CLK Input Duty Cycle	35		65	%
Center Frequency (f_c)		125		MHz

Thermal Characteristics

	Max	Units
Maximum Case Temperature @ 4.0 W	110	°C
Theta Junction to Case (T_{jc})	2.13	°C
Theta Junction to Ambient (T_{ja}) degrees Celsius/Watt - No Airflow @ 4.0 W	11.7	°C / W
Theta Junction to Ambient (T_{ja}) degrees Celsius/Watt - 225 LFPM Airflow @ 4.0 W	8.0	°C / W

5.1 DC Electrical Specification

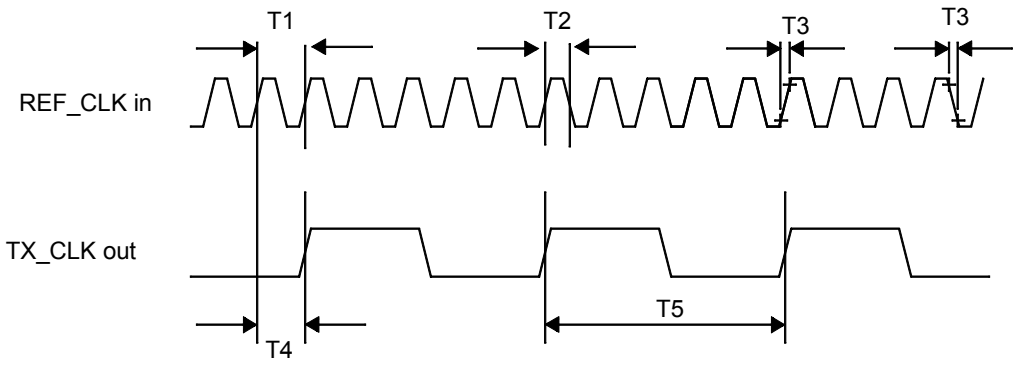
Symbol	Pin Types	Parameter	Conditions	Min	Typ	Max	Units
V_{IH} GMII inputs	I I/O I/O_Z	Input High Voltage	V_{DD} = 3.3 V	1.7			V
V_{IL} GMII inputs	I I/O I/O_Z	Input Low Voltage	V_{DD} = 3.3 V			0.9	V
V_{IH} non-GMII inputs	I I/O I/O_Z	Input High Voltage	V_{DD} = 3.3 V	2.0			V
V_{IL} non-GMII inputs	I I/O I/O_Z	Input Low Voltage	V_{DD} = 3.3 V			0.8	V
I_{IH}	I I/O I/O_Z	Input High Current	V_{IN} = V_{DD} V_{DD} = $V_{DD(max)}$			10	µA
I_{IL}	I I/O I/O_Z	Input Low Current	V_{IN} = 0 V V_{DD} = $V_{DD(max)}$			10	µA
R strap	Strap	PU/PD internal resistor value.		35-6	5		kΩ
R strap	JTAG	PU/PD internal resistor value.		20-4	0		kΩ

Symbol	Pin Types	Parameter	Conditions	Min	Typ	Max	Units
V_{OL} GMII outputs	O, I/O I/O_Z	Output Low Voltage	I_{OL} = 1.0 mA $V_{DD} = V_{DD(min)}$	Gnd		0.5	V
V_{OH} GMII outputs	O, I/O I/O_Z	Output High Voltage	I_{OH} = -1 mA $V_{DD} = V_{DD(min)}$	2.1		3.6	V
V_{OL} non-GMII outputs	O, I/O I/O_Z	Output Low Voltage	I_{OL} = 4 mA $V_{DD} = V_{DD(min)}$	Gnd		0.4	V
V_{OH} non-GMII outputs	O, I/O I/O_Z	Output High Voltage	I_{OH} = -4 mA $V_{DD} = V_{DD(min)}$	2.4			V
V_{OL}	LED	Output Low Voltage	I_{OL} = 2.5 mA			0.4	V
V_{OH}	LED	Output High Voltage	I_{OH} = -2.5 mA	2.4			V
I_{OZ1}	I/O _Z	TRI-STATE Leakage	$V_{OUT} = V_{DD}$			10	µA
I_{OZ2}	I/O_Z T	RI-STATE Leakage	V_{OUT} = GND			-10	µA
R_{INdiff}	RXD_B±	Differential Input Resistance	see Test Conditions section	2.4			kΩ
V_{TXD_100}	TXD_A±	100 M Transmit V_{DIFF}	see Test Conditions section	0.950	1.0	1.05	V peak differential
V_{TXDsym}	TXD_A±	100 M Transmit Voltage Symmetry	see Test Conditions section		±2		%
V_{TXD_1000-2}	TXD#±	1000 M Transmit V_{DIFF} (Note 2)	see Test Conditions section	0.7	5		V peak differential
V_{TXD_1000-1}	TXD#±	1000 M Transmit V_{DIFF} (Note 3)	see Test Conditions section	0.37	5		V peak differential
C_{IN1}	I	CMOS Input Capacitance			8		pF
C_{OUT1}	O, I/O I/O_Z	CMOS Output Capacitance			8		pF
3.3V I_{dd1000}	3.3V Supply	1000BASE-T (Full Duplex)	see Test Conditions section		680		mA
1.8V I_{dd1000}	1.8V Supply	1000BASE-T (Full Duplex)	see Test Conditions section		900		mA

Note 1: IEEE test mode 1, points A and B as described in Clause 40, section 40.6.1.2.1

Note 2: IEEE test mode 1, points C and D as described in Clause 40, section 40.6.1.2.1

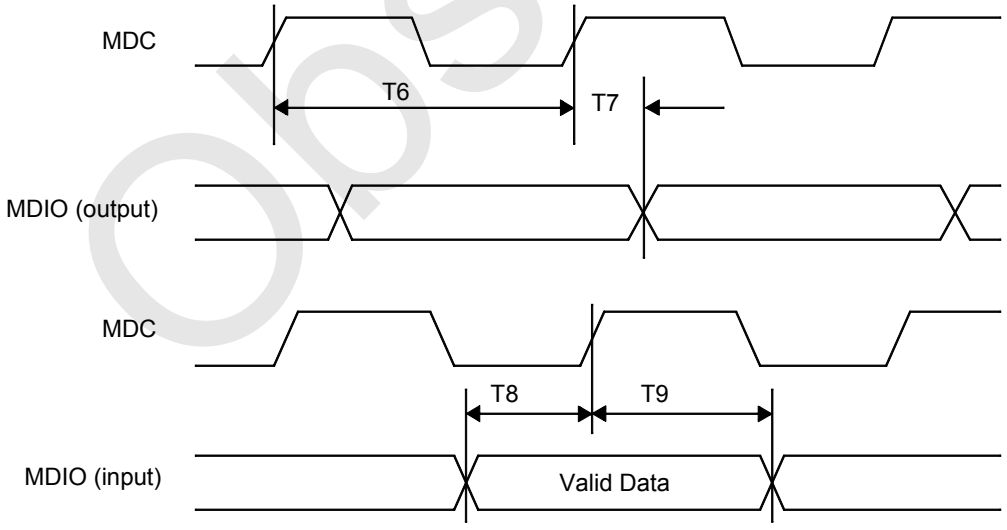
5.2 PGM Clock Timing



Parameter	Description	Notes	Min	Typ	Max	Units
T1	REF_CLK frequency		-50		+50	125 MHz+/- ppm
T2	REF_CLK Duty Cycle		40		60	%
T3	REF_CLK t_R/t_F	10% to 90%		200-500		ps
T4	REF_CLK to TX_CLK Delay		-3 (Note 1)		+3	ns
T5	TX_CLK Duty Cycle		40		60	%

Note 1: Guaranteed by design. Not tested.

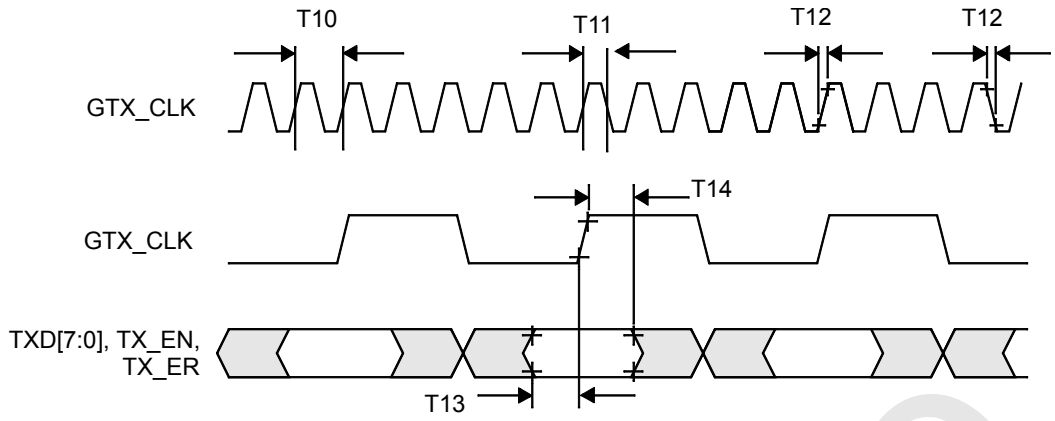
5.3 Serial Management Interface Timing



Parameter	Description	Notes	Min	Typ	Max	Units
T6	MDC Frequency				2.5	MHz
T7	MDC to MDIO (Output) Delay Time		0		300	ns
T8	MDIO (Input) to MDC Setup Time		10			ns
T9	MDIO (Input) to MDC Hold Time		10			ns

5.4 1000 Mb/s Timing

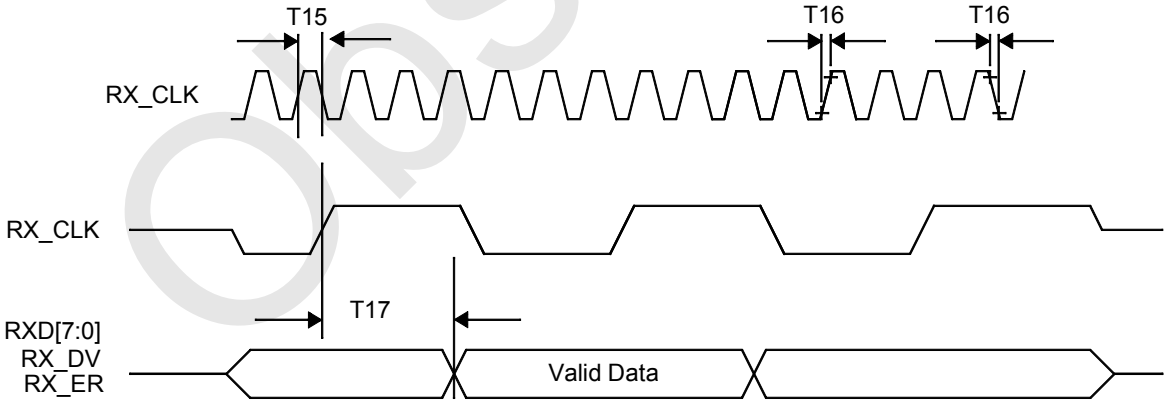
5.4.1 GMII Transmit Interface Timing



Parameter	Description	Notes	Min	Typ	Max	Units
T10	GTX_CLK Stability (Note 5)		-100		+100	ppm
T11	GTX_CLK Duty Cycle		40		60	%
T12	GTX_CLK t_R/t_F (Note 5)	Note 1,4			1	ns
T13	Setup from valid TXD, TX_EN and TXER to ↑ GTX_CLK	Note 2,4	2.0			ns
T14	Hold from ↑ GTX_CLK to invalid TXD, TX_EN and TXER	Note 3,4	0.0			ns

Note 1: t_r and t_f are measured from $V_{IL\_AC(MAX)}$ = 0.7V to $V_{IH\_AC(MIN)}$ = 1.9V.
Note 2: t_{setup} is measured from data level of 1.9V to clock level of 0.7V for data = '1'; and data level = 0.7V to.clock level 0.7V for data = '0'.
Note 3: t_{hold} is measured from clock level of 1.9V to data level of 1.9V for data = '1'; and clock level = 1.9V to.data level 0.7V for data = '0'.
Note 4: GMII Receiver input template measured with "GMII point-to-point test circuit", see Test Conditions Section
Note 5: Guaranteed by design. Not tested.

5.4.2 GMII Receive Timing

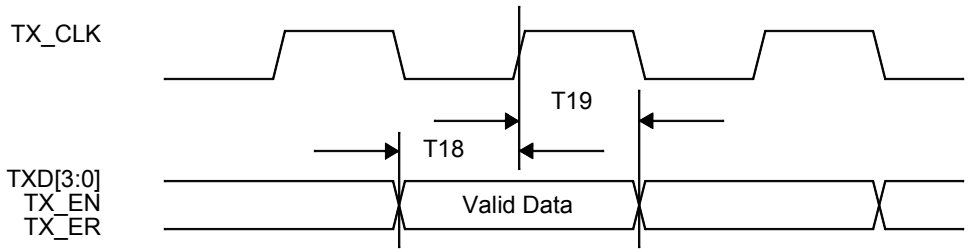


Parameter	Description	Notes	Min	Typ	Max	Units
T15	RX_CLK Duty Cycle		40		60	%
T16	RX_CLK t_R/t_F (Note 5)	Note 1, 4			1	ns
T17	↑ RX_CLK to RXD, RX_DV and RX_ER delay	Note 2, 3, 4	0.5		5.5	ns

Note 1: t_r and t_f are measured from $V_{IL\_AC(MAX)}$ = 0.7V to $V_{IH\_AC(MIN)}$ = 1.9V.
Note 2: $t_{delay\ max}$ is measured from clock level of 0.7V to data level of 1.9V for data = '1'; and clock level = 0.7V to.data level 0.7V for data = '0'.
Note 3: $t_{delay\ min}$ is measured from clock level of 1.9V to data level of 1.9V for data = '1'; and clock level = 1.9V to.data level 0.7V for data = '0'.
Note 4: GMII Receiver input template measured with "GMII point-to-point test circuit", see Test Conditions Section.
Note 5: Guaranteed by design. Not tested.

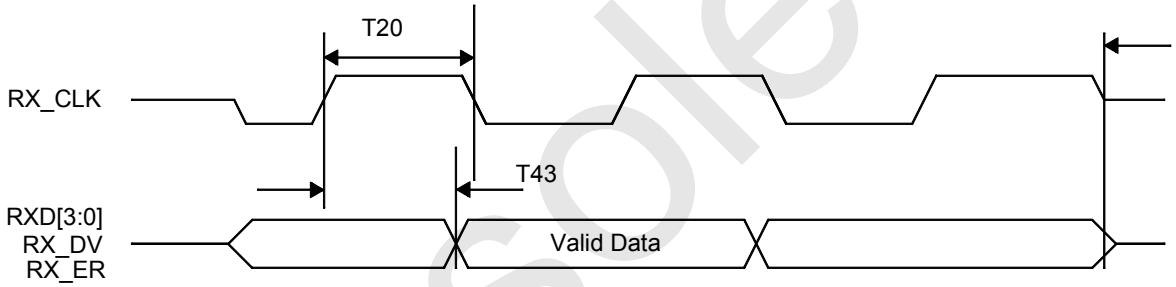
5.5 100 Mb/s Timing

5.5.1 100 Mb/s MII Transmit Timing



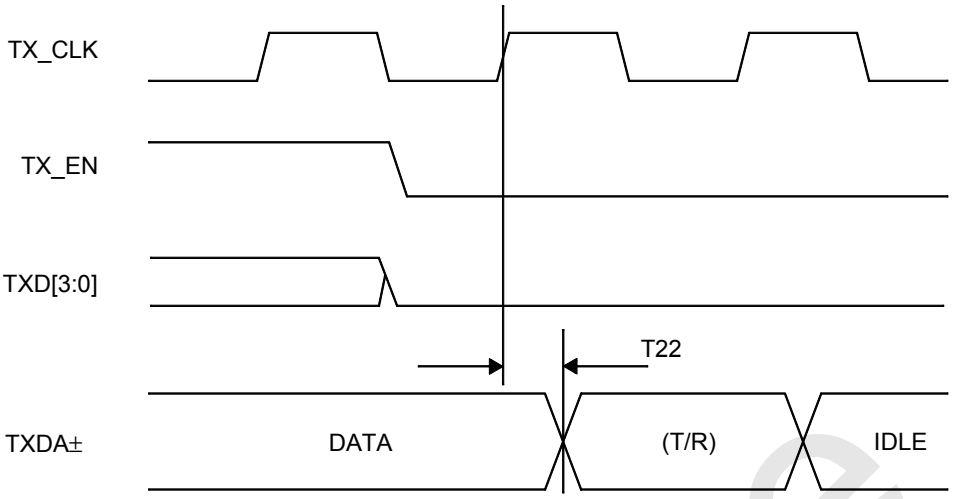
Parameter	Description	Notes	Min	Typ	Max	Units
T18	TXD[3:0], TX_EN, TX_ER Setup to ↑ TX_CLK		10			ns
T19	TXD[3:0], TX_EN, TX_ER Hold from ↑ TX_CLK		-1			ns

5.5.2 100 Mb/s MII Receive Timing



Parameter	Description	Notes	Min	Typ	Max	Units
T43	↑ RX_CLK to RXD[3:0], RX_DV, RX_ER Delay		10		30	ns
T20	RX_CLK Duty Cycle		35		65	%

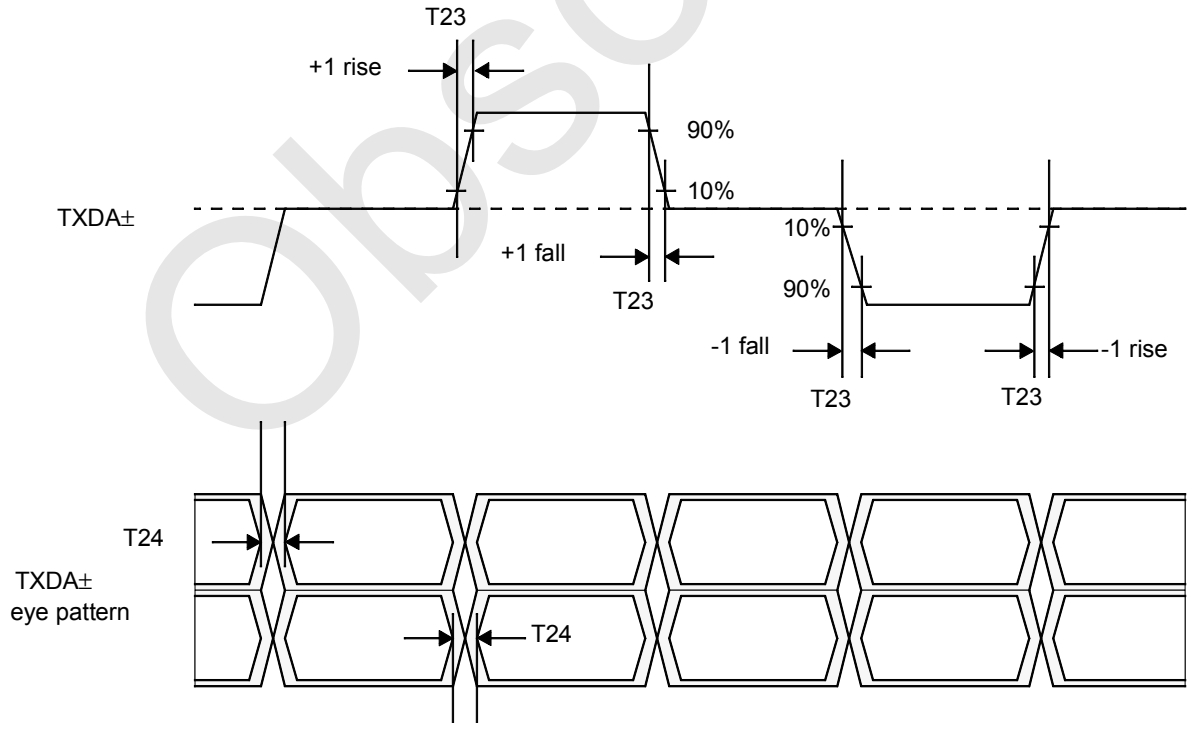
5.5.3 100BASE-TX Transmit Packet Deassertion Timing



Parameter	Description	Notes	Min	Typ	Max	Units
T22	TX_CLK to TXDA± Idling				6.0	bits

Note: Deassertion is determined by measuring the time from the first rising edge of TX_CLK occurring after the deassertion of TX_EN to the first bit of the "T" code group as output from the TXDA± pins. For Symbol mode, because TX_EN has no meaning, Deassertion is measured from the first rising edge of TX_CLK occurring after the deassertion of a data nibble on the Transmit MII to the last bit (LSB) of that nibble when it deasserts on the wire. 1 bit time = 10 ns in 100 Mb/s mode.

5.5.4 100BASE-TX Transmit Timing ($t_{R/F}$ & Jitter)

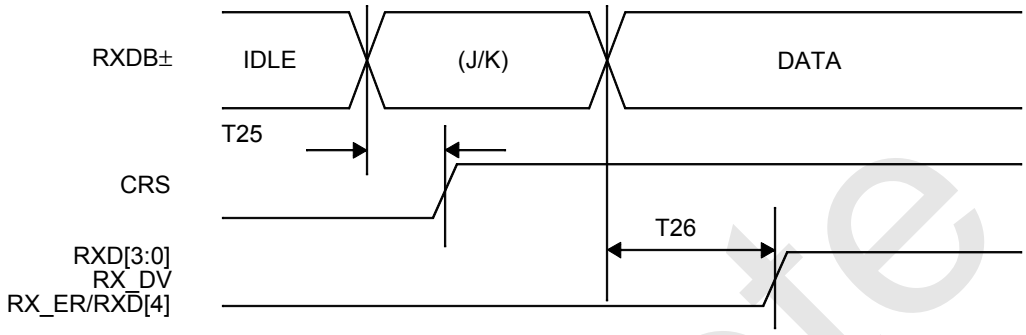


Parameter	Description	Notes	Min	Typ	Max	Units
T23	100 Mb/s TXDA± t_R and t_F	see Test Conditions section	3	4	5	ns
	100 Mb/s t_R and t_F Mismatch			500		ps
T24	100 Mb/s TXDA± Transmit Jitter				1.4	ns

Note: Normal mismatch is the difference between the maximum and minimum of all rise and fall times.

Note: Rise and fall times taken at 10% and 90% of the +1 or -1 amplitude.

5.5.5 100BASE-TX Receive Packet Latency Timing



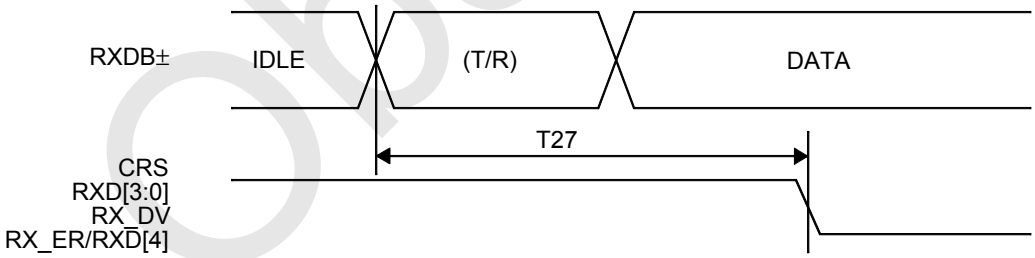
Parameter	Description	Notes	Min	Typ	Max	Units
T25	Carrier Sense ON Delay				17.5	bits
T26	Receive Data Latency				21	bits

Note: Carrier Sense On Delay is determined by measuring the time from the first bit of the “J” code group to the assertion of Carrier Sense.

Note: 1 bit time = 10 ns in 100 Mb/s mode.

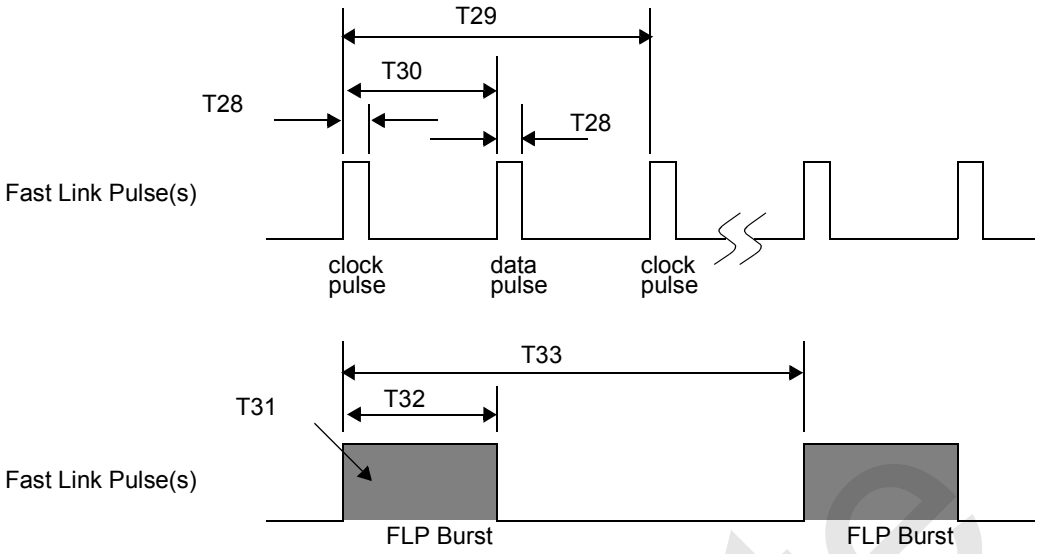
Note: RXDB± voltage amplitude is greater than the Signal Detect Turn-On Threshold Value.

5.5.6 100BASE-TX Receive Packet Deassertion Timing



Parameter	Description	Notes	Min	Typ	Max	Units
T27	Carrier Sense OFF Delay				21.5	bits

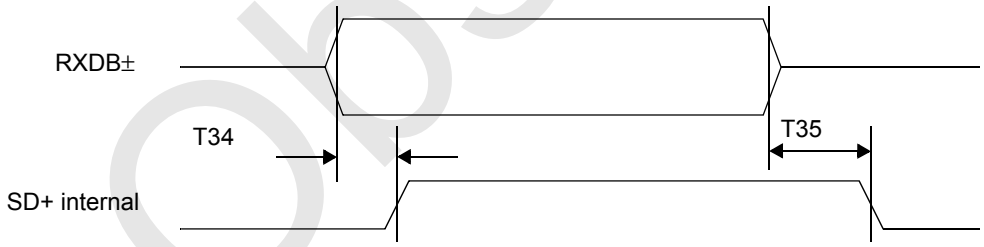
5.6 Auto-Negotiation Fast Link Pulse (FLP) Timing



Parameter	Description	Notes	Min	Typ	Max	Units
T28	Clock/Data Pulse Width			100		ns
T29	Clock Pulse to Clock Pulse Period		111	125	139	µs
T30	Clock Pulse to Data Pulse Period	Data = 1	55.5	62.5	69.5	µs
T31	Number of Pulses in a Burst		17		33	#
T32	Burst Width			2		ms
T33	FLP Burst to FLP Burst Period		8		24	ms

Note: These specifications represent both transmit and receive timings.

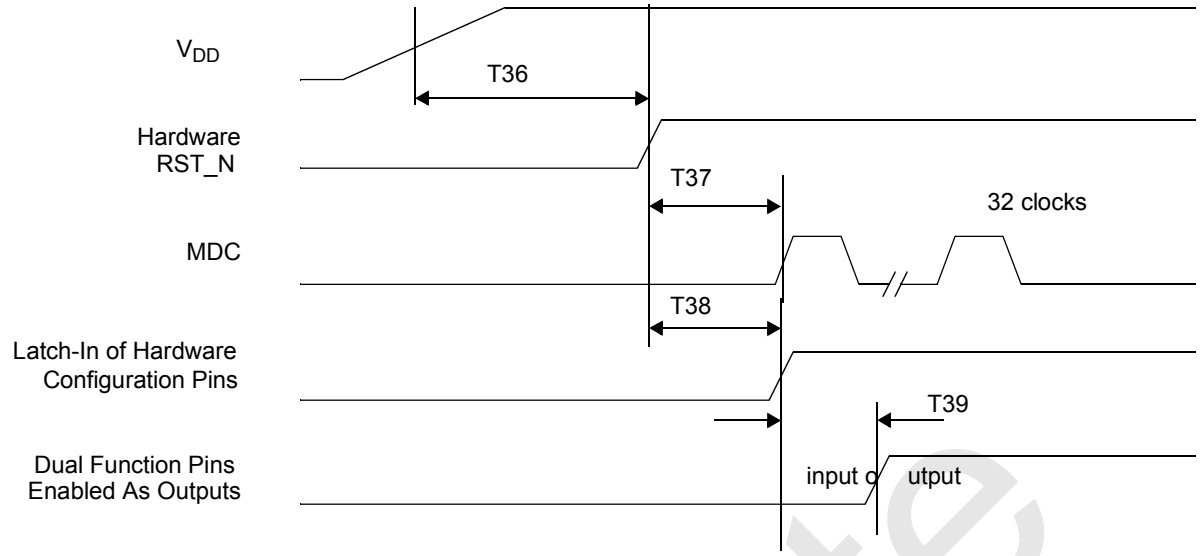
5.6.1 100BASE-TX Signal Detect Timing



Parameter	Description	Notes	Min	Typ	Max	Units
T34	SD Internal Turn-on Time				1	ms
T35	SD Internal Turn-off Time				300	µs

Note: The signal amplitude at RXDB± is TP-PMD compliant.

5.7 Reset Timing

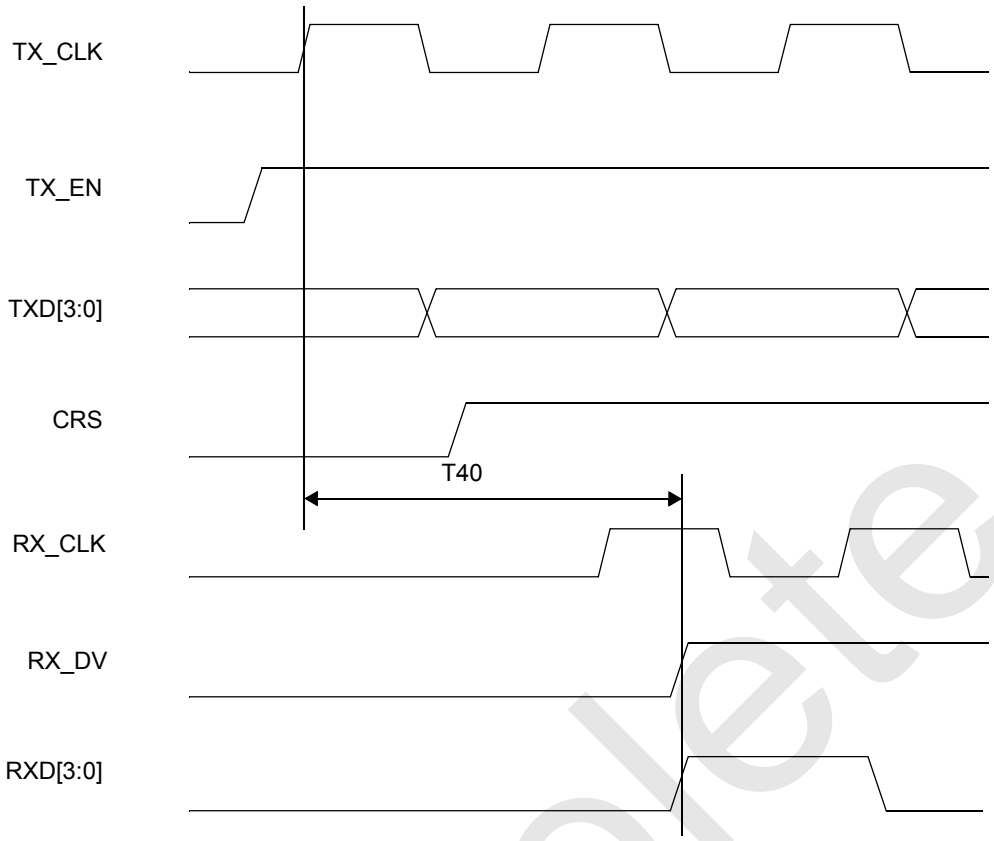


Parameter	Description	Notes	Min	Typ	Max	Units
T36	Hardware RESET Pulse Width		140			µs
T37	Post RESET Stabilization time prior to MDC preamble for register accesses	MDIO is pulled high for 32-bit serial management initialization		3		µs
T38	Hardware Configuration Latch-in Time from the Deassertion of RESET (either soft or hard)	Hardware Configuration Pins are described in the Pin Description section		3		µs
T39	Hardware Configuration pins transition to output drivers	It is important to choose pull-up and/or pull-down resistors for each of the hardware configuration pins that provide fast RC time constants in order to latch-in the proper value prior to the pin transitioning to an output driver		50		ns

Note: Software Reset should be initiated no sooner then 500 µs after power-up or the deassertion of hardware reset.

Note: It is important to choose pull-up and/or pull-down resistors for each of the hardware configuration pins that provide fast RC time constants in order to latch-in the proper value prior to the pin transitioning to an output driver.

5.8 Loopback Timing



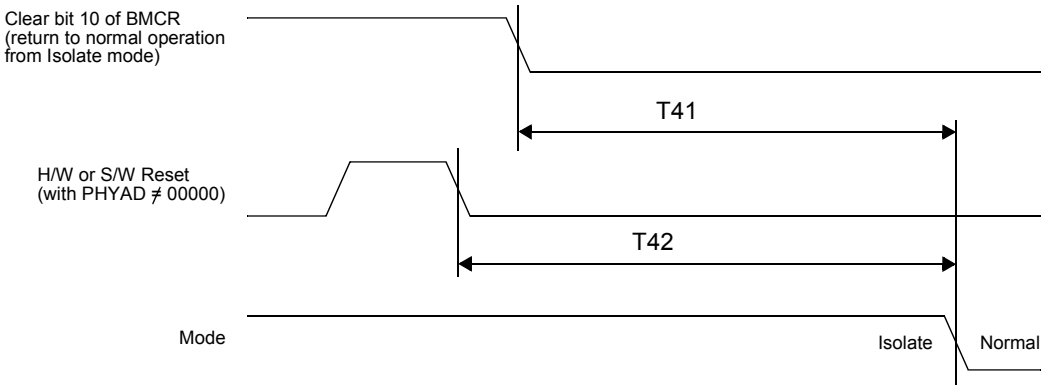
Parameter	Description	Notes	Min	Typ	Max	Units
T40	TX_EN to RX_DV Loopback	100 Mb/s			240	ns

Note: Due to the nature of the descrambler function, all 100BASE-X Loopback modes will cause an initial “dead-time” of up to 550 μs during which time no data will be present at the receive MII outputs. The 100BASE-X timing specified is based on device delays after the initial 550 μs “dead-time”.

Note: During loopback (all modes) both the TD± outputs remain inactive by default.

Note: The TD± outputs of the DP83861 can be enabled or disabled during loopback operation via the LBK_XMT_EN bit (bit 0 of the LBR register).

5.9 Isolation Timing



Parameter	Description	Notes	Min	Typ	Max	Units
T41	From software clear of bit 10 in the BMCR register to the transition from Isolate to Normal Mode				100	µs
T42	From Deassertion of S/W or H/W Reset to transition from Isolate to Normal mode				500	µs

6.0 Test Conditions

This section contains information relating to the specific test environments, (including stimulus and loading parameters), used for the DP83861. These test conditions are categorized by pin/interface type in the following subsections:

— CMOS Outputs i.e., GMII/MII and LEDs

— TXD± Outputs sourcing 100BASE-TX

— TXD± Outputs sourcing 1000BASE-T

Additionally, testing conditions for Idd measurements are included.

6.1 CMOS Outputs (GMII/MII and LED)

Each of the GMII/MII and LED outputs are loaded with a controlled current source to either ground or V_{DD} for testing V_{OH}, V_{OL}, and AC parametrics. The associated capacitance of this load is 50 pF. The diagram in Figure 17 illustrates the test configuration.

It should be noted that the current source and sink limits are set to 4.0 mA when testing/loading the GMII/MII output pins. The current source and sink limits are set to 2.5 mA when testing/loading the LED output pins.

6.2 TXD± Outputs (sourcing 100BASE-TX)

When configured for 100BASE-TX operation, these differential outputs source scrambled 125 Mb/s data at MLT-3 logic levels. These outputs are loaded as illustrated in Figure 18. Note that the transmit amplitude and rise/fall time measurements are made across the secondary of the transmit transformer as specified by the IEEE 802.3u Standard. This test is done at nominal Vcc's.

6.3 TXD± Outputs (sourcing 1000BASE-T)

When configured for 1000BASE-T operation, the differential outputs (4-pairs) source Pattern-1 (see below) at 125 Mb/s using PAM-17 levels. The outputs are loaded as illustrated in Figure 19. Note that the transmit amplitude and rise/fall time measurements are made across the secondary of the transmit transformer as specified by the IEEE 802.3ab/D5.1 Specification.

Pattern 1:

{{+2 followed by 127 0 symbols}, {-2 followed by 127 0 symbols}, {+1 followed by 127 0 symbols}, {-1 followed by 127 0 symbols}, (128 +2 symbols, 128 -2 symbols}, {1024 0 symbols}}

6.4 Idd Measurement Conditions

The DP83861 EN Gig PHYTER is currently tested for total device Idd under three operational modes:

— 100BASE-TX Full Duplex (max packet length / min IPG)

— 1000BASE-T Full Duplex (max packet length / min IPG)

The device loading described in each of the preceding sections is present during Idd test execution.

6.5 GMII Point-to-Point Test Conditions

In order to meet the requirements to support point-to-point links RX_CLK must comply with the potential template shown in Figure 20 using the test circuit in Figure 21.

6.6 GMII Setup and Hold Test Conditions

In order to meet the requirements to support point-to-point links GMII drivers (RXD[7:0], RX_DV, RX_ER) must comply with the potential template shown in Figure 20 using the test circuit in Figure 22 and meet the setup and hold times specified in Section 5.4.2 GMII Receive Timing.

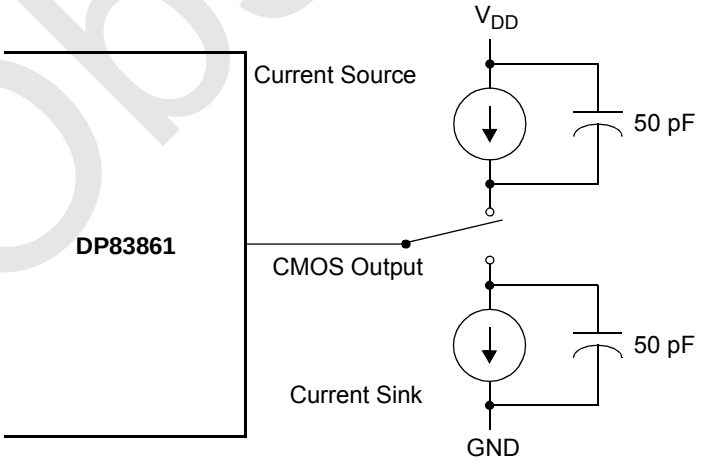


Figure 17. CMOS Output Test Load

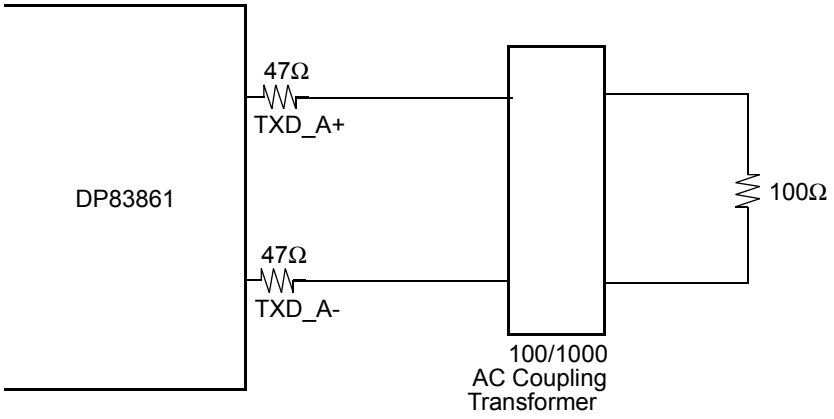


Figure 18. 100 Mb/s Twisted Pair Load (zero meters)

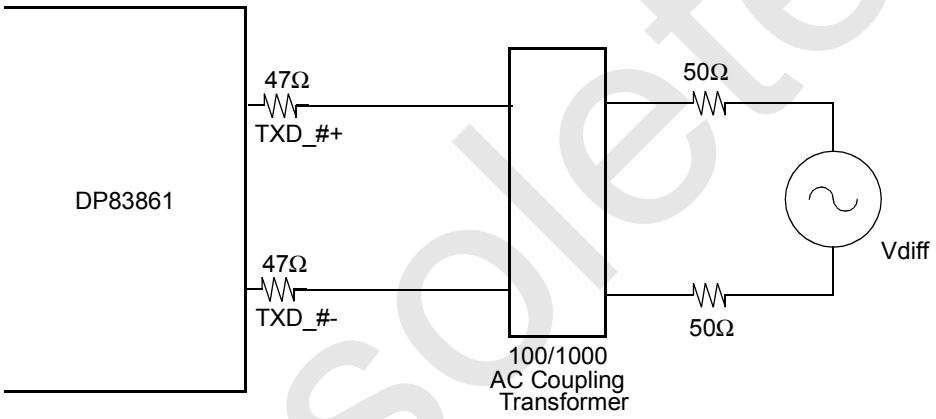


Figure 19. 1000 Mb/s Twisted Pair Load (zero meters)

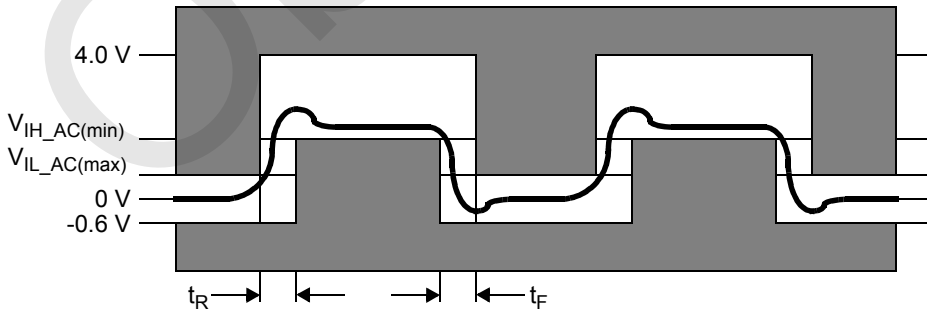


Figure 20. GMII Receiver Input Potential Template

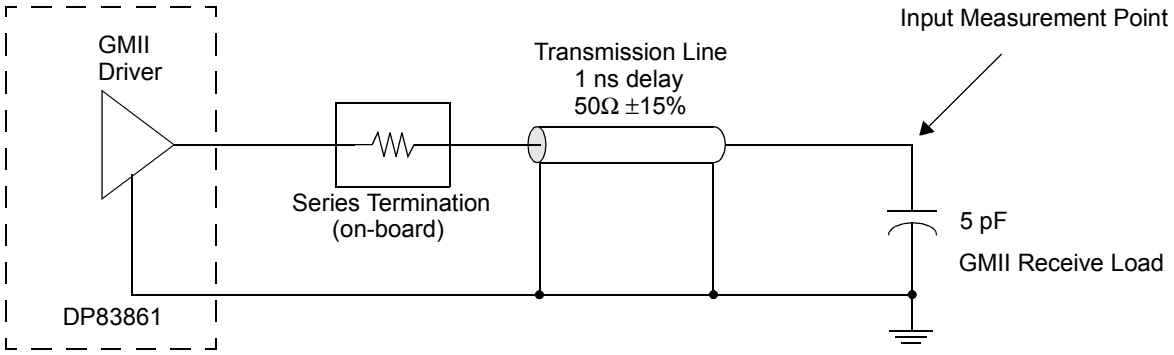


Figure 21. GMII Point-to-Point Test Circuit

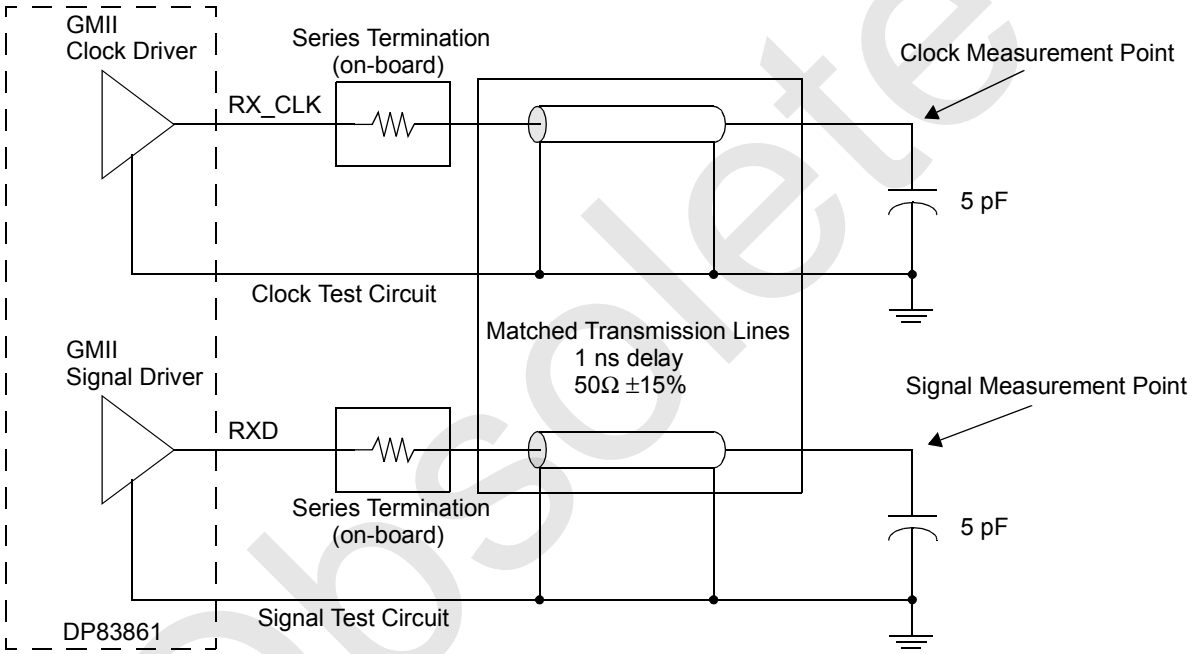


Figure 22. GMII Setup and Hold Time Test Circuit

7.0 User Information:

7.1 10Mb/s VOD

IEEE 802.3 specification, Clause 14, requires that the 10 Mb/s output levels be within the following limits:

VOD = 2.2 to 2.8 V peak-differential, when terminated by a 100Ω resistor directly at the RJ-45 outputs. The DP83861's 10 Mb/s output level is typically 1.58 V peak-differential.

IEEE 802.3 specification, Clause 14, requires that a 10 Mb/s PHY should be able to correctly receive signal levels on Vin = 585 mV peak-differential. It also requires that any signal which is less than 300 mV peak-differential should be rejected by the PHY. The DP83861 VOD level of 1.58 V peak-differential is received at the link partner with magnitudes exceeding Vin = 585 mV peak-differential for cables up to 150 meters of CAT3 or CAT5 cables.

In 10 Mb/s operation the DP83861 can receive and transmit up to 187 meters using CAT5 cable and over 100 meters using CAT3 cable. There is no system level impact on the receive ability of the link partner due to the reduced levels of VOD transmitted by the DP83861.

There are no plans to change the 10 Mb/s VOD levels.

7.2 Asymmetrical Pause

IEEE 802.3ab has assigned bit 11 in register 0x04 to indicate Asymmetrical PAUSE capability. In the DP83861 this bit is a read only bit with a default value of zero.

Asymmetrical PAUSE capability can be advertised by doing the following software register writes through the MDIO interface:

Write to Register 0x16 the value 0x0D
Write to Register 0x1E the value 0x8084
Write to Register 0x1D the value 0x0001

The order of the writes are important. Register 0x1E is a pointer to the internal expanded addresses. Register 0x1D contains the data to be written to or read from the internal address pointed by register 0x1E.The contents of register 0x1E automatically increments after each read or write to register 0x1D. Therefore, if one wants to confirm that the data write was successful, one should re-write register 0x1E with the original address and then read register 0x1D.

There are no plans to change the Asymmetrical Pause register.

7.3 Next Page

The Next Page operation is not IEEE 802/3ab compliant. When the DP83861 sends it's last Next Page (register 0x04, bit 15 = 0), the DP83861 will stop the Next Page exchange with its' Link Partner prematurely, without going through the final page. this will cause the Link Partner to time-out and a link will not be established. This only occurs when the Link Partner has more Next Pages to send than the DP83861. If the Link Partner has the same or less Next Pages to send than the DP83861. If the Link Partner has the same or less number of Next Pages then the DP83861 will complete Auto-Negotiation.

This problem only impacts systems that need to exchange Next page information. This does not affect the normal 1000 Mb/s Auto-Negotiation process. Below are software work-arounds for 10/100 Mb/s and 1 000 Mb/s modes if Next Pages need to be exchanged.

10/100 Mb/s Next Page Work-around:

— 1. Write to Register 0x00, bit 12 = 0 (Disables Auto-Negotiation)

— 2. Write to Register 0x04, bit 15 =1 (Advertises additional Next Page exchanges)

— 3. Write to Register 0x07, all 16 bits with Next Page information including:

Bit 15 [NP] = 0, if this is the final Next Page to be exchanged

Bit 15 [NP] = 1, if additional Next Pages are to follow

— 4. Write to Register 0x16 the value 0x0D (Enables expanded memory access)

— 5. Write to Register 0x1E the value 0x80DD (Accesses the expanded memory location)

— 6. Write to Register 0x1D the value 0x40 (Writes to the expanded memory location and alerts firmware that an additional Next Page is loaded)

— 7. Write to Register 0x08 the value 0x0000 (Clears the Auto-Negotiation Next page Receive Register)

— 8. Write Register 0x00, bits 9 and 12 = 1 (Enable and restart Auto-Negotiation)

— 9. Wait approximately 2 seconds for Auto-Negotiate to transfer the normal base page required for link.

— 10. Read Register 0x08 until a non-zero value is read (i.e. we receive the link partner's additional Next Page)

— 11. Store the contents of Register 0x08 locally (Somewhere in the Station Manager)

— 12. Read Register 0x08 bit 15 [NP].
If bit 15 = 0, then no more Next Pages to exchange
If bit 15 = 1, then go to 3.

1000 Mb/s Next Page Work-around

— 1. Write to Register 0x00, bit 12 = 0 (Disables Auto-Negotiation)

— 2. Write to Register 0x04, bit 15 =1 (Advertises additional Next Page exchanges)

— 3. Write to Register 0x07, all 16 bits with Next Page information including:

Bit 15 [NP] = 0, if this is the final Next Page to be exchanged

Bit 15 [NP] = 1, if additional Next Pages are to follow

— 4. Write to Register 0x16 the value 0x0D (Enables expanded memory access)

— 5. Write to Register 0x1E the value 0x80DD (Accesses the expanded memory location)

— 6. Write to Register 0x1D the value 0x40 (Writes to the expanded memory location and alerts firmware that an additional Next Page is loaded)

— 7. Write to Register 0x08 the value 0x0000 (Clears the Auto-Negotiation Next page Receive Register)

— 8. Write Register 0x00, bits 9 and 12 = 1 (Enable and restart Auto-Negotiation)

— 9. Wait approximately 4 to 5 seconds for Auto-Negotiate to transfer the normal base page, Message Page, and two unformated Message pages required for link.

— 10. Read Register 0x08 until a non-zero value is read (i.e. we receive the link partner's additional Next Page)

— 11. Store the contents of Register 0x08 locally (Somewhere in the Station Manager)

— 12. Read Register 0x08 bit 15 [NP].
If bit 15 = 0, then no more Next Pages to exchange
If bit 15 = 1, then go to 3.

There are no plans to change the Next Page operation.

7.4 125 MHz Oscillator Operation with Ref_Sel Floating

The Ref_Sel (pin 154) has an internal pull-up that when left floating will select the 125 MHz oscillator mode of operation for Ref_CLK (pin 153). Depending on board layout, noise on the Ref_Sel pin can corrupt internal clocks causing packet errors or intermittent loss of Link.

To guarantee robust operation across a variety of board layouts pin 154 must be connected either directly or through a 2 KΩ resistor to a 3.3 V supply (See Figure 3).

7.5 MDI/MDIX Operation when in Forced 10 Mb/s and 100MB/s

When the DP83861 is forced to 10Mb/s or 100Mb/s mode the Transmit Output and Receive Input will come up in either MDI mode (Transmit Outputs on RJ45 pins 1 and 2, Receive Outputs on RJ45 pins 3 and 6) or in MDIX mode (Transmit Outputs on RJ45 pins 3 and 6, Receive Outputs on RJ45 pins 1 and 2). This can cause the DP83861 not to establish Link depending on the configuration of the CAT5 cable (Crossover or Straight Cable) or the configuration of the link partner (MDI or MDIX mode).

The recommendation is to use Auto-Negotiation mode where the DP83861 will automatically detect the configuration of the cable and link partner.

There are no plans on fixing this.

7.6 Receive LED in 10 Mb/s Half Duplex mode

When the DP83861 is in 10 Mb/s Half Duplex mode the Receive LED will be active when the DP83861 transmits data.

There are no plans on fixing this.

8.0 EN Gig PHYTER Frequently Asked Questions:

8.1 Q1: What is the difference between TX_CLK, TX_TCLK, and GTX_CLK?

A1: All the 3 clocks above are related to transmitting data. However, their functions are completely different:

TX_CLK: This is used for 10/100 Mb/s transmit activity. It has two separate functions:

— It's used to synchronize the data sent by the MAC and to latch this data into the PHY.

— It's used to clock transmit data on the twisted pair.

The TX_CLK is an output of the PHY and is part of the MII interface as described in IEEE 802.3u specification, Clause 28.

GTX_CLK: This is used for 1000 Mb/s transmit activity. It has only one function:

— It's used to synchronize the data sent by the MAC and to latch this data into the PHY.

The GTX_CLK is NOT used to transmit data on the twisted pair wire. For 1000 Mb/s operation, the Master PHY uses the X1 clock to transmit data on the wire, while the Slave PHY uses the clock recovered from the channel A receiver, as the transmit clock for all four pairs.

The GTX_CLK is an output of the MAC and is part of the GMII interface as described in IEEE 802.3z specification, Clause 35.

TX_TCLK: This is used for 1000 Mb/s transmit activity. It has only one function:

— It's used in "Test Modes 2 & 3" to measure jitter in the data transmitted on the wire.

As explained above during the discussion of GTX_CLK, either the X1 clock or the clock recovered from received data is used for transmitting data; depending on whether the PHY is a MASTER or a SLAVE. TX_TCLK represents the actual clock being used to transmit data.

The TX_TCLK is an output of the PHY and can be enabled to come out on pin 192 (during Test Mode 2 and 3 it is automatically enabled). This is a requirement from the IEEE 802.3ab specification, Clause 40.6.1.2.5. (This clock is only available in the next generation Enhanced Gig-PHYTER DP83861).

8.2 Q2: What happens to the TX_CLK during 1000 Mb/s operation? Similarly what happens to RXD[4:7] during 10/100 Mb/s operation?

A2: As mentioned in **A1** above, TX_CLK is not used during the 1000 Mb/s operation, and the RXD[4:7] lines are not used for the 10/100 operation. These signals are outputs of the EN Gig PHYTER. To simplify the MII/GMII interface, these signals are driven actively to a zero volt level. This eliminates the need for pull-down resistors which would have been needed if these pins were left floating during no use.

8.3 Q3: What happens to the TX_CLK and RX_CLK during Auto-Negotiation and during idles?

A3: During Auto-Negotiation the EN Gig PHYTER drives a 25 MHz clock on the TX_CLK and RX_CLK lines. In 10 Mb/s mode, these lines are driven by a 2.5 MHz clock during idles. In 100 Mb/s mode they are driven by a 25 MHz clock during idles. In 1000 Mb/s mode they are driven by a 125 MHz clock during idles.

8.4 Q4: Why doesn't the EN Gig PHYTER complete Auto-Negotiation if the link partner is a forced 1000 Mb/s PHY?

A4: IEEE specifications only define "parallel detection" for 10/100 Mb/s operation. Parallel detection is the name given to the Auto-Negotiation process where one of the link partners is Auto-Negotiating while the other is in forced 10 or 100 Mb/s mode. In this case, it's expected that the Auto-Negotiating PHY establishes half-duplex link, at the forced speed of the link partner.

However, for 1000 Mb/s operation this parallel detection mechanism is not defined. Instead, any 1000BASE-T PHY can establish 1000 Mb/s operation with a link partner for the following two cases:

— When both PHYs are Auto-Negotiating,

— When both PHYs are forced 1000 Mb/s and when one of the PHYs is manually configured for MASTER and the other is manually configured for SLAVE.

8.5 Q5: My two EN Gig PHYTERs won't talk to each other, but they talk to another vendor's PHY.

A5: Avoid using Manual Master/Slave Configuration. If all PHYs on a switch box are configured for the same Master/Slave value, then they can't talk to each other, because one of the link partners has to be a slave while the other has to be a Master.

8.6 Q6: You advise not to use Manual Master/Slave configuration. How come it's an option?

A6: Manual Master/Slave configuration is similar to manual forcing of 10 or 100 Mb/s operation. The only way it can work is if both link partners are forced to compatible speed of operation, or if at least one of them is Auto-Negotiating. Since there is no way of knowing ahead of time, if the link partner will also use hardwired manual Master/Slave setting, there is no way to guarantee that there won't be a conflict (i.e both PHYs are assigned Master, or both PHYs are assigned Slave value.)

Some applications automatically hardwire a switch for Master and a Node card for a Slave status. However, this is wrong, since most of the early use for 1000BASE-T is for switch to switch backplane uplink ports, and hence this will result in the both link partners assigned to Master status. This will cause a conflict and prevent establishment of link.

8.7 Q7: How can I write to EN Gig PHYTER expanded address or RAM locations? Why do I need to write to these locations?

A7: The following functions require access to expanded address:

— Asymmetric Pause Advertise

— Next Page

— Programmable Interrupt

— Read Latest Firmware Revision

— Read ROM Revision

EN Gig PHYTER requires reads and writes to RAM to accomplish these tasks. As a sample procedure, we show how to advertise Asymmetrical PAUSE:

The following software register writes will be required if Asymmetrical PAUSE needs to be advertised:

— 1)Power down the DP83861 (i.e. set bit 11, register 0x00. This is to make sure that during RAM writes, the standard operation of the part doesn't interfere with what we are writing to the RAM.)

— 2) Write to register 0x16 the value 0x000D (This allows access to expanded access for 8 bit read/write.)

— 3) Write to register 0x1E the value 0x8084.

— 4) Write to register 0x1D the value 0x0001.

— 5) Take the EN Gig PHYTER out of power down mode (i.e. reset bit 11 of register 0x00.)

Note that the order of the writes is important. Register 0x1E is a pointer to the internal expanded addresses. Register 0x1D contains the data to be written to or read from the internal address pointed by register 0x1E. The contents of register 0x1E automatically increments after each read or write to register 0x1D. Therefore, if one wants to confirm that the data write was successful, one should re-write register 0X1E with the original address and then read register 0X1D.

All register writes are 16 bits. However the RAM data is 8 bits wide. In the 8 bit read/write mode as described above in step 2, the lowest 8 bits of the register will be written to the RAM location pointed by register 0x1E.

For each one of the desired functions listed above (e.g. disable jabber), steps 1,2, and 5 have to be followed. Depending on the exact functionality required a different register location and different data value have to be entered at steps 3) and 4).

8.8 Q8: What specific addresses and values do I have to use for each of the functions mentioned in Q7 above?

A8:

— **Advertise Asymmetrical Pause:** address 0x8084, value 0x01

— **Read Latest Firmware Revision:** addresses 0x8402 and 0x8403 contain a two character revision number. These are ASCII coded characters: The latest version of EN Gig PHYTER DP83861 will have rev code = "09" which corresponds to "0" =0x30 and "9" = 0x39.

— **Read Latest Hardware (ROM) Revision:** addresses 0xD002 and 0xD003 contain a two character revision number. These are ASCII coded characters: Production version of EN Gig PHYTER DP83861 will have rev code = "3B" which corresponds to "3" = 0x33 and "B" = 0x42.

— **E^2PROM checksum:** RAM location 0x83FE contains the value of the computed checksum, and RAM location 0x83FF contains the checksum indicated by the firmware which was loaded.

8.9 Q9: How can I do firmware updates? What are some of the benefits of the firmware updates?

A9: Firmware updates have many uses. Some of these uses are:

— If future bugs are discovered, they could be fixed (or work arounds implemented) using firmware updates. Typically for hardwired PHYs without the firmware update option, the customer has to "live with the bug", or try to implement a software work around.

— Enhancements and additional functionality can be added to the EN Gig PHYTER. For example, the EN Gig PHYTER might be able to detect cable length and indicate this length in a register. These functions are not implemented in hardware at this time, and they will be added as enhancements using firmware updates.

To update firmware there are two options:

1) Use E^2PROM. This is described in the Application Note "DP83861 EN Gig PHYTER E^2PROM Usage Guide." (Available soon.) National will supply the.HEX files needed to program the serial E^2PROM devices.

2) Using the driver and/or management interface (MDC/MDIO). An application note on this method "DP83861: Firmware Download Using the MDIO/MDC Interface" is available now. Basically the procedure will be similar to what is described in answer 7. The main difference is that 16 bit read/write mode will be used. As discussed earlier in answer 7, all register writes are 16 bits. However the RAM data is 8 bits wide. In the 8 bit read/write mode as described earlier, the lowest 8 bits of register 0x1D will be written to the RAM location pointed by register 0x1E. This is sufficient for single register writes and this mode was used to make the necessary RAM write in answer 7. However for loading the entire 14 KB of RAM, this method is not efficient. Since each MDC/MDIO read/write accesses a 16 bit register, it is more efficient to use one MII register write, and let the internal software break this into two 8 bit RAM writes. To achieve this, we will program a 16 bit read/write mode into register 0x16, instead of the earlier 8 bit mode as described in answer 7. In this mode each 16 bit write into register 0x1D, is broken into 2 internal 8 bit RAM writes. The internal hardware will automatically, increment the RAM address pointer register 0x1E after each 8 bit write. It will first use the lowest 8 bits of register 0x1D to write to the RAM location pointed by register 0x1E. Then it will increment the address pointed by 0x1E by one, and write the most significant 8 bits of 0x1D into the next RAM location. This is all transparent to the user, who only has to set the 16 bit read/write mode as described in step 2 below and then do regular 16 bit MDC/MDIO writes.

— 1)Power down the DP83861 (i.e. set bit 11, register 0x00. This is to make sure that during RAM writes, the standard operation of the part doesn't interfere with what we are writing to the RAM.)

— 2) Write to register 0x16 the value 0x0006 (This allows access to expanded access for 16 bit read/write.)

— 3) Write to register 0x1E the value 0x8400. (The starting address of RAM)

— 4) Write to register 0x1D the desired value. The higher 8 bits of this register will be written into location pointed by register 0x1E above. Then the location pointed to by register 0x1E will incremented by one automatically to point to the next location. Next, the 8 least significant bits of register 0x1D will be written to the RAM location pointed by register 0x1E. (The values to be written to all the RAM locations will be supplied by National in a HEX file.)

— 5) Write to register 0x1D the next desired value.

— 6) Continue repeating step 5 for all data to be written as shown in the.HEX file to be supplied by National.

— 7) Write 0x8400 to register 0x1F. This starts execution of down loaded code at address 0x8400.

— 8)Wait for 1.024 ms. (i.e. no MDC/MDIO access for 1.024 ms)

— 9) Read register 0x00 (This read is needed to clear an interrupt problem.)

— 10) Take the EN Gig PHYTER out of power down mode (i.e. reset bit 11 of register 0x00.)

8.10 Q10: How long does Auto-Negotiation take?

A10: Two EN Gig PHYTERs typically complete Auto-Negotiation and establish 1000 Mb/s operation within 5 seconds. 1000BASE-T Auto-Negotiation process takes longer than the 10/100 Mb/s. One of the reasons for this is the use of Next Page exchanges during 1000 Mb/s negotiation.

8.11 Q11: I know I have good link, but register 0x01, bit 2 "Link Status" doesn't contain value = '1' indicating good link.

A11: This bit is defined by IEEE 802.3u Clause 22. It indicates if the link was lost since the last time this register was read. Its name (given by IEEE) is perhaps misleading. A more accurate name would have been the "Link lost" bit. If the actual present link status is desired, then either this register should be read twice, or register 0x11 bit 2 should be read. Register 0x11 shows the actual status of link, speed, and duplex regardless of what was advertised or what has happened in the interim.

8.12 Q12: I have forced 100 Mb/s operation but the 100 Mb/s speed LED doesn't come on.

A12: Speed LEDs are actually an AND function of the speed and link status. Regardless of whether the speed is forced or Auto-Negotiated, there has to be a good link, before the speed LEDs will come on.

8.13 Q13: Your reference design shows pull-up or pull-down resistors attached to certain pins, which conflict with the pull-up or pull-down information specified in the datasheet?

A13: The pull-up or pull-down information specified in the pin description section of the datasheet, indicate if there is an internal pull-up or pull-down resistor at the IO buffer used for that specific pin. These internal resistors are between 25 - 65 kΩ. They will determine the default strap value if the pin is floated. If the default value is desired to be overwritten, then an external 2 KΩ pull-up or pull-down resistor can be used.

8.14 Q14: What are some other applicable documents?

A14:

— DP83861 Reference Design (Schematics, BOM, Gerber files.)

— IEEE 802.3z "MAC Parameters, Physical Layer, Repeater and Management Parameters for 1000 Mb/s Operation."

— IEEE 802.3ab "Physical layer specification for 1000 Mb/s operation on four pairs of category 5 or better balanced twisted pair cable (1000BASE-T)".

— IEEE 802.3 and 802.3u (For 10/100 Mb/s operation.)

8.15 Q15: How is the maximum junction temperature calculated?

A15: The maximum die temperature is calculated using the following equations:

$T_J = T_A + P_d(\Theta_{JA})$

$T_J = T_C + P_d(\Theta_{JC})$

$T_C = T_J - P_d(\Theta_{JC})$

Where:

T_J = Junction temperature of the die in ^oC
T_C = Case temperature of the package in ^oC
P_d = Power dissipated in the die in Watts
Θ_{JA} = 11.7 ^oC/watt
Θ_{JC} = 2.13 ^oC/watt

For reliability purposes the maximum junction should be kept below 120 ^oC. If the Ambient temperature is 70 ^oC and the power dissipation is 4.0 watts then the Maximum Case Temperature will be:

$T_{C\ max} = 120\ ^oC - 4.0\ watts(2.13\ ^oC/watt)$

$T_{C\ max} = 111.48\ ^oC$

8.16 Q16: How do I measure FLP's?

A16: In order measure FLP's you must first disable Auto MDIX function. When in Auto MDIX mode the DP83861 will put out link pulses every 150 µs. The MDIX pulse could be confused with the FLP pulses which occur every 125 µs +/- 14 µs.

To disable MDIX the following register writes need to be done

Register	Write	Comments
0x00	bit 11 = 1	This puts the DP83861 into power down mode.
0x16	000D	This allows access to expanded memory mode.
0x1E	808B	This allows access to expanded memory 808B.
0x1D	0001	This disables MDIX mode.
0x00	bit 11 = 0	This takes the DP83861 out of power down mode.

Once MDIX is disabled the DP83861 will randomly come up in cross over mode or straight cable mode output FLP's on either pins 1 and 2 or 3 and 6 on the RJ45.

8.17 Q17: The DP83861 will establish Link in 10 Mb/s and 100Mb/s mode with a Broadcom part, but it will not establish link in 1000 Mb/s mode. When this happens the DP83861's Link led will blink on and off.

A17: We have received a number of questions regarding inter-operability of National's DP83861 with Broadcom's BCM5400. National's DP83861 is compliant to IEEE 802.3ab and it is also inter-operable with the BCM5400 as

well as other Gigabit Physical Layer products. However, there are certain situations that might require extra attention when inter-operating with the BCM5400.

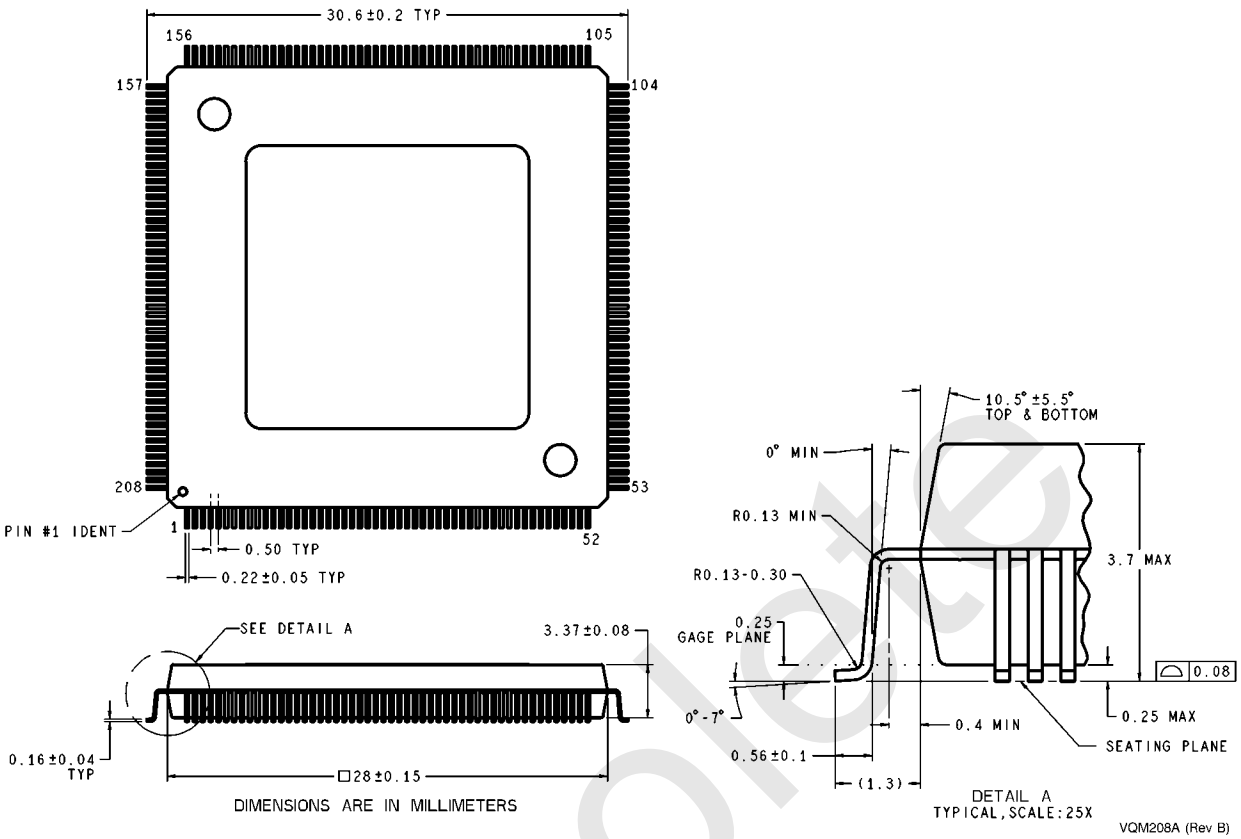
There are mainly two types of BCM5400's, those with silicon revisions earlier than C5 and those with silicon revisions of C5 and older. There is a fundamental problem with earlier silicon revisions of the BCM 5400, whereby the part was designed with faulty start-up conditions (wrong polynomials were used) which prevented the Broadcom BCM5400 from ever linking to an IEEE 802.3ab compliant part.

This problem was observed in early inter-operability testing. A solution was put together that allows the DP83861 to inter-operate with any IEEE 802.3ab compliant Gigabit PHY as well as with earlier revisions of the BCM5400 that are non compliant. To enter into this mode of operation you can either pull pin 196 (NC MODE) high through a 2 k Ω resistor or write to register 0x10h bit 10 (10.10 = 1).

8.18 Q18: Why isn't the Interrupt Pin (Pin 208) an Open Drain Output?

A18: The Interrupt feature was added by changing the internal firmware of the device and the only output pins that were available were standard Active High and Active Low outputs. This pin can not be bussed to other pins. External logic gates must be used to connect multiple Interrupt pins together.

9.0 Physical Dimensions inches (millimeters) unless otherwise noted



208 Lead Plastic Quad Flat Pack
Order Number DP83861VQM
NS Package VQM-208A

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