

DS90CF581 LVDS Transmitter 24-Bit Color Flat Panel Display (FPD) Link

Check for Samples: [DS90CF581](#)

FEATURES

- Up to 140 Megabyte/sec Bandwidth
- Narrow Bus Reduces Cable Size and Cost
- 290 mV Swing LVDS Devices for Low EMI
- Low Power CMOS Design
- Power-down Mode
- PLL Requires No External Components
- Low Profile 56-Lead TSSOP Package
- Falling Edge Data Strobe
- Compatible with TIA/EIA-644 LVDS Standard

DESCRIPTION

The DS90CF581 transmitter converts 28 bits of CMOS/TTL data into four LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. At a transmit clock frequency of 40 MHz, 24 bits of RGB data and 4 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY, CNTL) are transmitted at a rate of 280 Mbps per LVDS data channel. Using a 40 MHz clock, the data throughput is 140 Megabytes per second. This transmitter is intended to interface to any of the FPD Link receivers.

The chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

Block Diagram

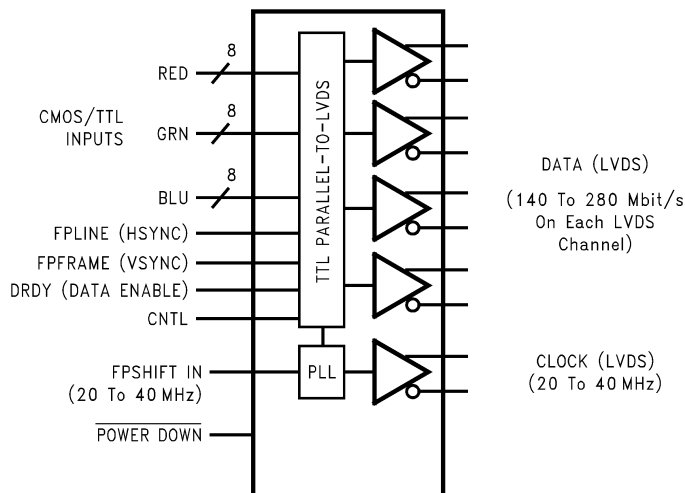


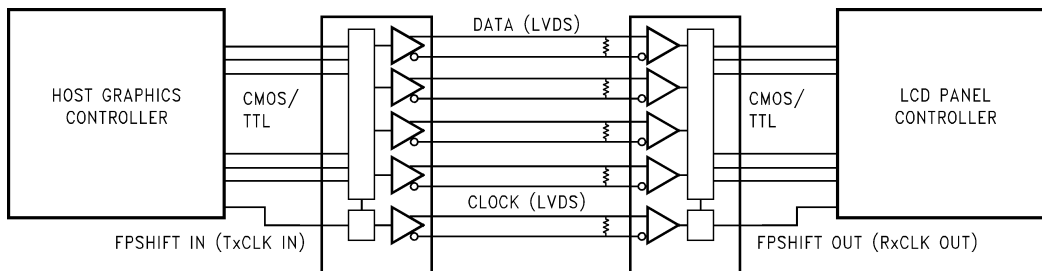
Figure 1. DS90CF581
See Package Number DGG0056A



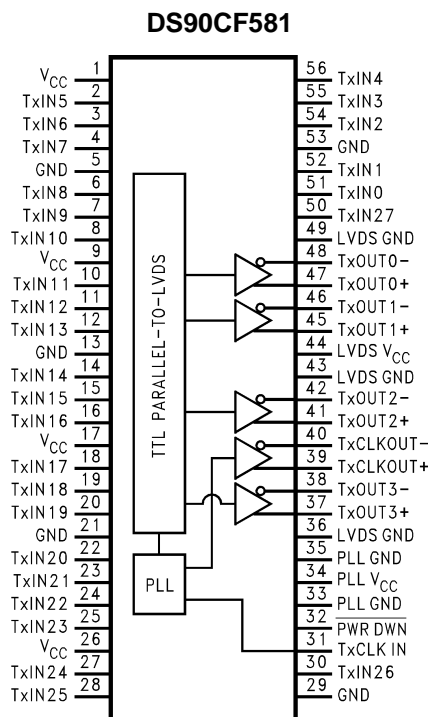
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Application



Connection Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

		Value	Unit
Supply Voltage (V_{CC})		-0.3 to +6	V
CMOS/TTL Input Voltage		-0.3 to ($V_{CC} + 0.3$)	V
LVDS Driver Output Voltage		-0.3 to ($V_{CC} + 0.3$)	V
LVDS Output Short Circuit Duration		continuous	
Junction Temperature		+150	°C
Storage Temperature Range		-65 to +150	°C
Lead Temperature (Soldering, 4 sec.)		+260	°C
Maximum Package Power Dissipation @ +25°C	DGG0056A (TSSOP) Package:	DS90CF581	1.63
	Derate Package:	DS90CF581	12.5 mW/°C above +25
This device does not meet 2000V ESD rating. ⁽³⁾			

- (1) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
 (2) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits. "Electrical Characteristics" specify conditions for device operation.
 (3) ESD Rating: HBM (1.5 kΩ, 100 pF) PLL $V_{CC} \geq 1000V$ All other pins $\geq 2000V$ EIAJ (0Ω, 200 pF) $\geq 150V$

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Operating Free Air Temperature (T_A)	-10	+25	+70	°C
Receiver Input Range	0		2.4	V
Supply Noise Voltage (V_{CC})			100	mV _{P-P}

Electrical Characteristics⁽¹⁾

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ ⁽²⁾	Max	Units
CMOS/TTL DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
V_{CL}	Input Clamp Voltage	$I_{CL} = -18$ mA		-0.79	-1.5	V
I_{IN}	Input Current	$V_{IN} = V_{CC}, GND, 2.5V$ or 0.4V		±5.1	±10	μA
LVDS DRIVER DC SPECIFICATIONS						
V_{OD}	Differential Output Voltage	$R_L = 100\Omega$	250	290	450	mV
ΔV_{OD}	Change in V_{OD} between Complimentary Output States				35	mV
V_{OS}	Offset Voltage ⁽³⁾		1.1	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between Complimentary Output States				35	mV
V_{OH}	High Level Output Voltage			1.3	1.6	V
V_{OL}	Low Level Output Voltage		0.9	1.01		V
I_{OS}	Output Short Circuit Current	$V_{OUT} = 0V, R_L = 100\Omega$		-2.9	-5	mA
I_{OZ}	Output TRI-STATE Current	Power Down = 0V, $V_{OUT} = 0V$ or V_{CC}		±1	±10	μA
TRANSMITTER SUPPLY CURRENT						
I_{CCTW}	Transmitter Supply Current, Worst Case	$R_L = 100\Omega, C_L = 5$ pF, Worst Case Pattern (Figure 2, Figure 4)	f = 32.5 MHz	34	51	mA
			f = 37.5 MHz	36	53	mA

- (1) Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).
 (2) Typical values are given for $V_{CC} = 5.0V$ and $T_A = +25^\circ C$.
 (3) V_{OS} previously referred as V_{CM} .

Electrical Characteristics⁽¹⁾ (continued)

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ ⁽²⁾	Max	Units
I _{CCTG}	Transmitter Supply Current, 16 Grayscale	R _L = 100Ω, C _L = 5 pF, Grayscale Pattern (Figure 3, Figure 4)	f = 32.5 MHz	27	47	mA
			f = 37.5 MHz	28	48	mA
I _{CCTZ}	Transmitter Supply Current, Power Down	Power Down = Low		1	25	μA

Transmitter Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units	
LLHT	LVDS Low-to-High Transition Time (Figure 4)		0.75	1.5	ns	
LHLT	LVDS High-to-Low Transition Time (Figure 4)		0.75	1.5	ns	
TCIT	TxCLK IN Transition Time (Figure 5)			8	ns	
TCCS	TxOUT Channel-to-Channel Skew ⁽¹⁾ (Figure 6)			350	ps	
TPPos0	Transmitter Output Pulse Position for Bit 0 (Figure 12)	f = 20 MHz	-200	150	350	ps
TPPos1	Transmitter Output Pulse Position for Bit 1		6.3	7.2	7.5	ns
TPPos2	Transmitter Output Pulse Position for Bit 2		12.8	13.6	14.6	ns
TPPos3	Transmitter Output Pulse Position for Bit 3		20	20.8	21.5	ns
TPPos4	Transmitter Output Pulse Position for Bit 4		27.2	28	28.5	ns
TPPos5	Transmitter Output Pulse Position for Bit 5		34.5	35.2	35.6	ns
TPPos6	Transmitter Output Pulse Position for Bit 6		42.2	42.6	42.9	ns
TPPos0	Transmitter Output Pulse Position for Bit 0 (Figure 12)	f = 40 MHz	-100	100	300	ps
TPPos1	Transmitter Output Pulse Position for Bit 1		2.9	3.3	3.9	ns
TPPos2	Transmitter Output Pulse Position for Bit 2		6.1	6.6	7.1	ns
TPPos3	Transmitter Output Pulse Position for Bit 3		9.7	10.2	10.7	ns
TPPos4	Transmitter Output Pulse Position for Bit 4		13	13.5	14.1	ns
TPPos5	Transmitter Output Pulse Position for Bit 5		17	17.4	17.8	ns
TPPos6	Transmitter Output Pulse Position for Bit 6		20.3	20.8	21.4	ns
TCIP	TxCLK IN Period (Figure 7)	25	T	50	ns	
TCIH	TxCLK IN High Time (Figure 7)	0.35T	0.5T	0.65T	ns	
TCIL	TxCLK IN Low Time (Figure 7)	0.35T	0.5T	0.65T	ns	
TSTC	TxIN Setup to TxCLK IN (Figure 7)	f = 20 MHz	14			ns
		f = 40 MHz	8			ns
THTC	TxIN Hold to TxCLK IN (Figure 7)	2.5	2		ns	
TCCD	TxCLK IN to TxCLK OUT Delay @ 25°C, V _{CC} = 5.0V (Figure 8)	5		9.7	ns	
TPLLS	Transmitter Phase Lock Loop Set (Figure 9)			10	ms	
TPDD	Transmitter Powerdown Delay (Figure 11)			100	ns	

(1) This limit based on bench characterization.

AC Timing Diagrams

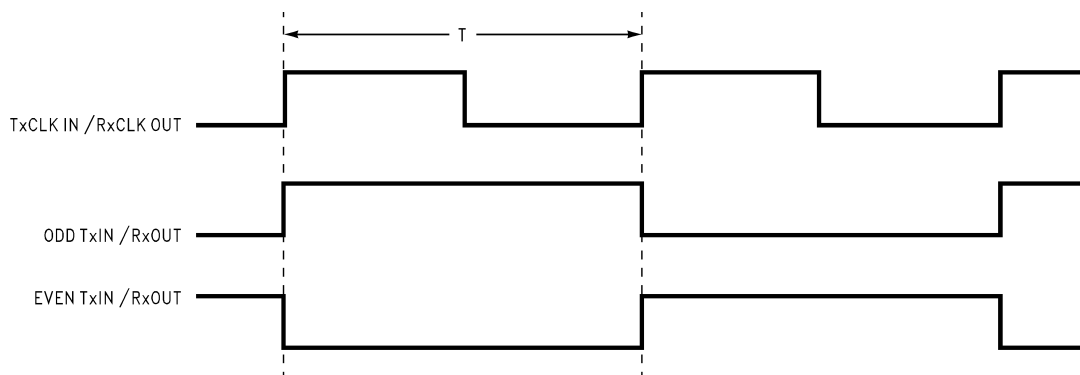


Figure 2. "WORST CASE" Test Pattern

Device Pin Name	Signal	Signal Pattern	Signal Frequency
TxCLK IN / RxCLK OUT	Dot Clk		f
TxIN0 / RxOUT0	R0		f/16
TxIN1 / RxOUT1	R1		f/8
TxIN2 / RxOUT2	R2		f/4
TxIN3 / RxOUT3	R3		f/2
TxIN4 / RxOUT4	R4		Steady State, Low
TxIN5 / RxOUT5	R7		Steady State, Low
TxIN6 / RxOUT6	R5		Steady State, Low
TxIN7 / RxOUT7	G0		Steady State, Low
TxIN8 / RxOUT8	G1		f/16
TxIN9 / RxOUT9	G2		f/8
TxIN10 / RxOUT10	G6		f/4
TxIN11 / RxOUT11	G7		f/2
TxIN12 / RxOUT12	G3		Steady State, Low
TxIN13 / RxOUT13	G4		Steady State, Low
TxIN14 / RxOUT14	G5		Steady State, Low
TxIN15 / RxOUT15	B0		Steady State, Low
TxIN16 / RxOUT16	B6		f/16
TxIN17 / RxOUT17	B7		f/8
TxIN18 / RxOUT18	B1		f/4
TxIN19 / RxOUT19	B2		f/2
TxIN20 / RxOUT20	B3		Steady State, Low
TxIN21 / RxOUT21	B4		Steady State, Low
TxIN22 / RxOUT22	B5		Steady State, Low
TxIN23 / RxOUT23	RES		Steady State, Low
TxIN24 / RxOUT24	HSYNC		Steady State, High
TxIN25 / RxOUT25	VSYNC		Steady State, High
TxIN26 / RxOUT26	EN		Steady State, High
TxIN27 / RxOUT27	R6		Steady State, High

- (1) The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.
- (2) The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.
- (3) Figure 2 and Figure 3 show a falling edge data strobe (TxCLK IN/RxCLK OUT).
- (4) Recommended pin to signal mapping. Customer may choose to define differently.

Figure 3. "16 GRAYSCALE" Test Pattern

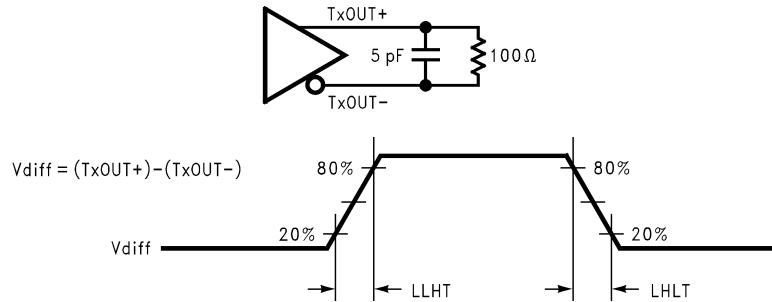


Figure 4. DS90CF581 (Transmitter) LVDS Output Load and Transition Timing

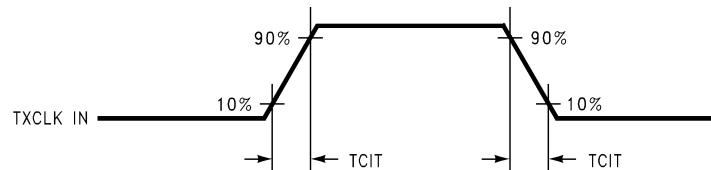
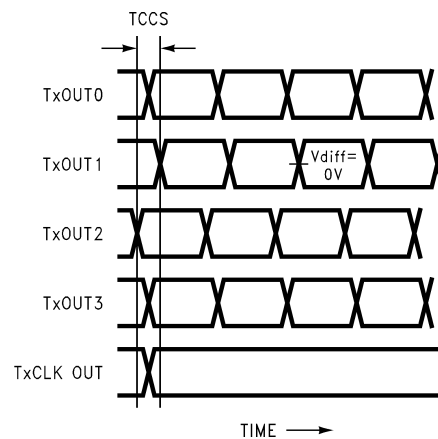


Figure 5. DS90CF581 (Transmitter) Input Clock Transition Time



- (1) Measurements at $V_{diff} = 0V$
- (2) TCCS measured between earliest and latest initial LVDS edges.
- (3) TxCLK OUT Differential High→Low Edge for DS90CF581
TxCLK OUT Differential Low→High Edge for DS90CR581

Figure 6. DS90CF581 (Transmitter) Channel-to-Channel Skew

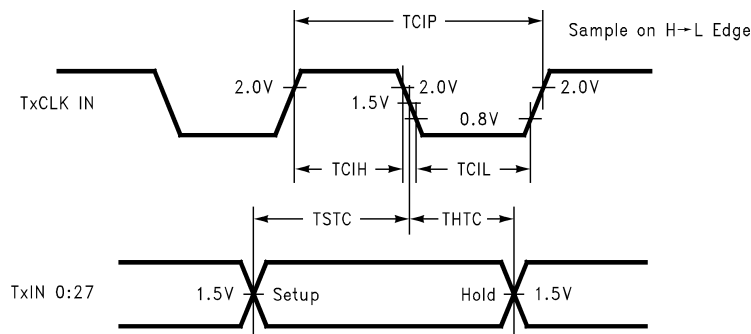


Figure 7. DS90CF581 (Transmitter) Setup/Hold and High/Low Times

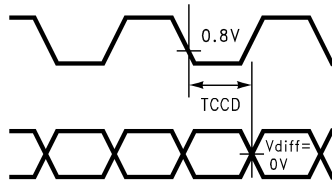


Figure 8. DS90CF581 (Transmitter) Clock In to Clock Out Delay

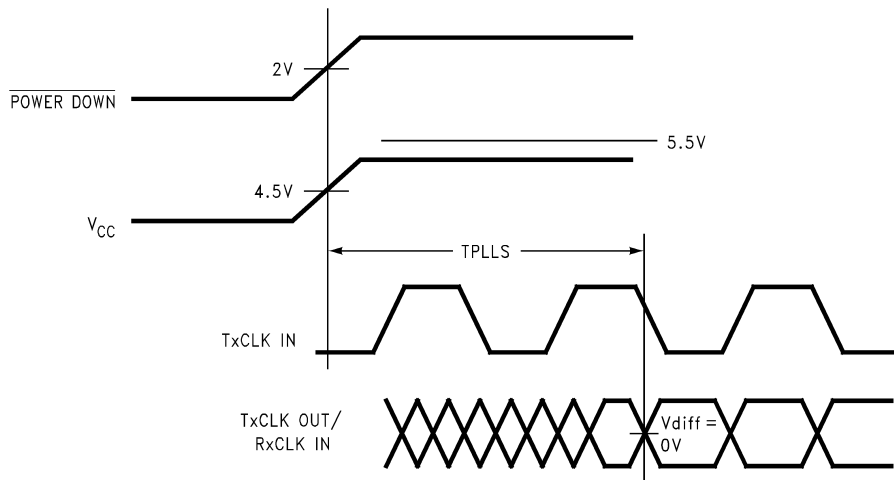


Figure 9. DS90CF581 (Transmitter) Phase Lock Loop Set Time

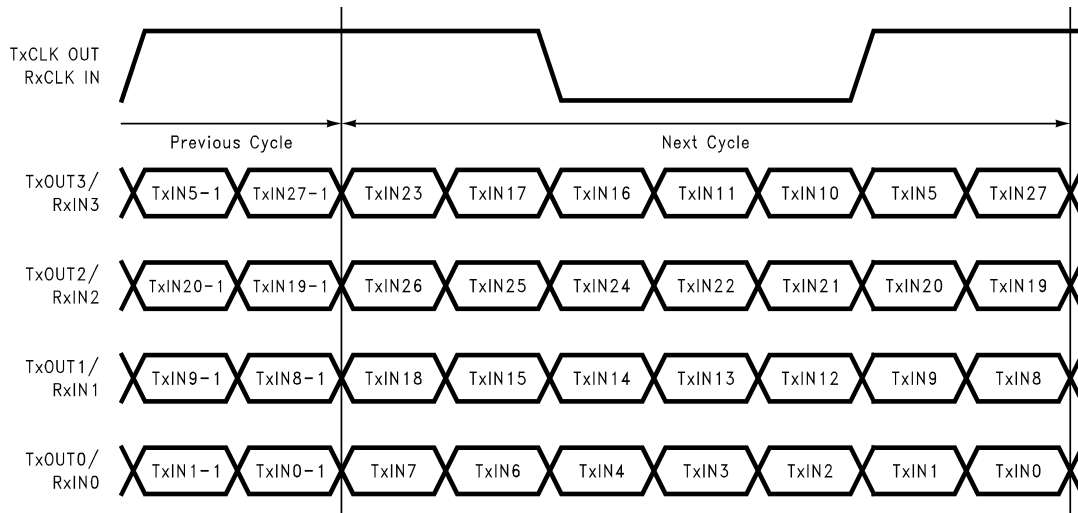


Figure 10. 28 Parallel TTL Data Inputs Mapped to LVDS Outputs (DS90CF581)

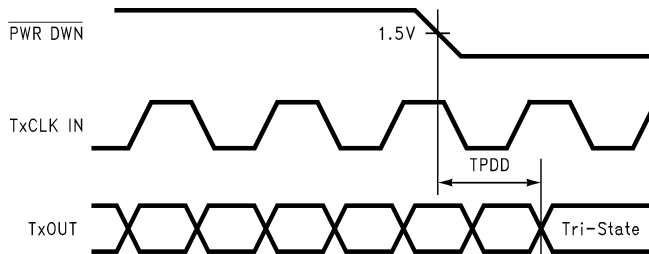


Figure 11. Transmitter Powerdown Delay

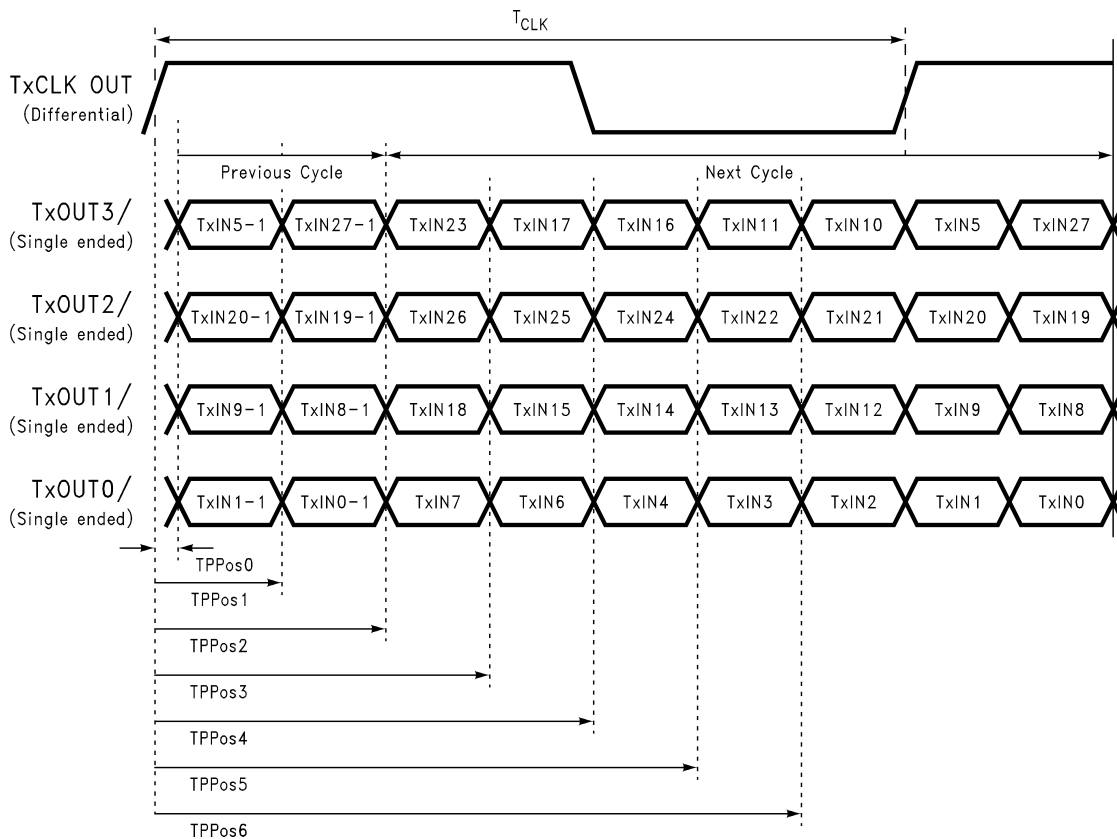


Figure 12. Transmitter LVDS Output Pulse Position Measurement

DS90CF581 Pin Descriptions — FPD Link Transmitter

Pin Name	I/O	No.	Description
TxIN	I	28	TTL level input. This includes: 8 Red, 8 Green, 8 Blue, and 4 control lines (FPLINE, FPFRAME, DRDY, CNTL). (Also referred to as HSYNC, VSYNC and DATA ENABLE)
TxOUT+	O	4	Positive LVDS differential data output
TxOUT-	O	4	Negative LVDS differential data output
FPSHIFT IN	I	1	TTL level clock input. The falling edge acts as data strobe.
TxCLK OUT+	O	1	Positive LVDS differential clock output
TxCLK OUT-	O	1	Negative LVDS differential clock output
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) TRI-STATE the outputs, ensuring low current at power down.
V_{CC}	I	4	Power supply pins for TTL inputs
GND	I	5	Ground pins for TTL inputs
PLL V_{CC}	I	1	Power supply pin for PLL
PLL GND	I	2	Ground pins for PLL
LVDS V_{CC}	I	1	Power supply pin for LVDS outputs
LVDS GND	I	3	Ground pins for LVDS outputs

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	9

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