DS90CR581 LVDS Transmitter 24-Bit Color Flat Panel Display (FPD) Link

Check for Samples: DS90CR581

FEATURES

- **Up to 140 Megabyte/sec Bandwidth**
- **Narrow Bus Reduces Cable Size and Cost**
- **290 mV Swing LVDS Devices for Low EMI**
- **Low Power CMOS Design**
- **Power Down Mode**
- **PLL Requires no External Components**
- **Low Profile 56-lead TSSOP Package**
- **Rising Edge Data Strobe**
- **Compatible with TIA/EIA-644 LVDS Standard**

DESCRIPTION

The DS90CR581 transmitter converts 28 bits of CMOS/TTL data into four LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. At a transmit clock frequency of 40 MHz, 24 bits of RGB data and 4 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY, CNTL) are transmitted at a rate of 280 Mbps per LVDS data channel. Using a 40 MHz clock, the data throughput is 140 Megabytes per second. This transmitter is intended to interface to any of the FPD Link receivers.

The chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

BLOCK DIAGRAM

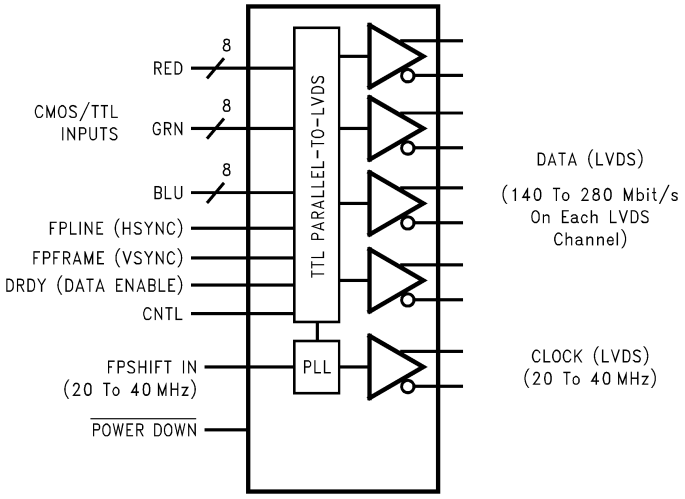
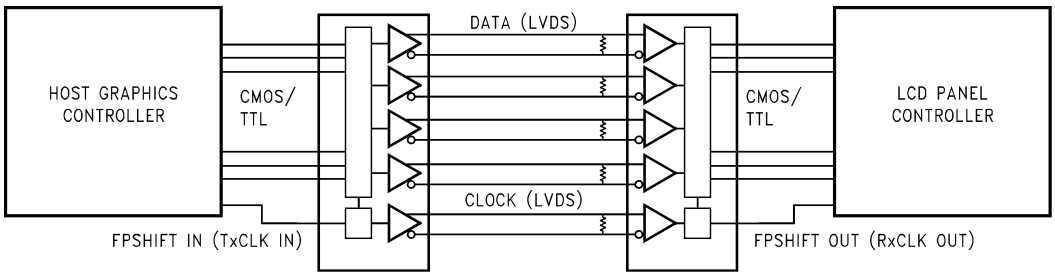


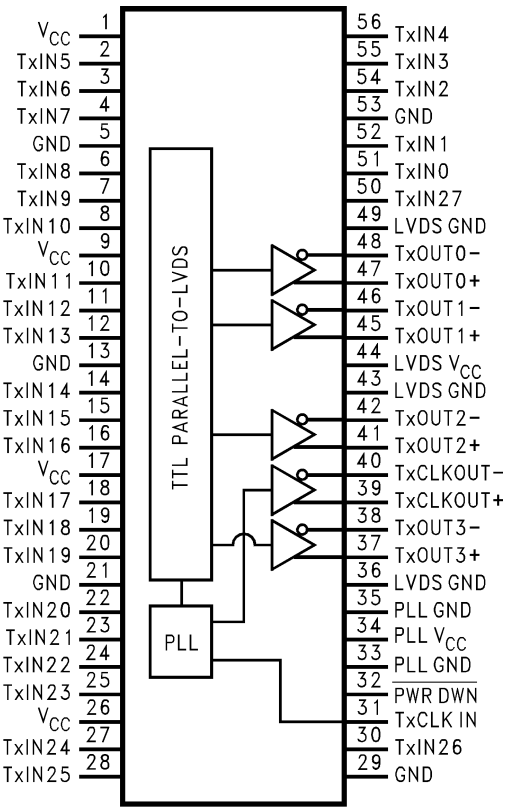
Figure 1. DS90CR581
See Package Number DGG

Application



Connection Diagram

DS90CR581



DS90CR581
TSSOP Package
See Package Number DGG

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Supply Voltage (V_{CC})			−0.3 to +6V
CMOS/TTL Input Voltage			−0.3 to (V_{CC} + 0.3V)
LVDS Driver Output Voltage			−0.3 to (V_{CC} + 0.3V)
LVDS Output Short Circuit Duration			continuous
Junction Temperature			+150°C
Storage Temperature Range			−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)			+260°C
Maximum Package Power Dissipation @ +25°C	DGG (TSSOP) Package:	DS90CR581	1.63W
	Package Derating:	DS90CR581	12.5 mW/°C above +25°C
This device does not meet 2000V ESD rating.[3]			

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits. "Electrical Characteristics" specify conditions for device operation.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) ESD Rating: HBM (1.5 kΩ, 100 pF) PLL V_{CC} ≥ 1000V All other pins ≥ 2000V EIAJ (0Ω, 200 pF) ≥ 150V

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Operating Free Air Temperature (T_A)	−10	+25	+70	°C
Receiver Input Range	0		2.4	V
Supply Noise Voltage (V_{CC})			100	mV_{P-P}

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
CMOS/TTL DC SPECIFICATIONS							
V_{IH}	High Level Input Voltage			2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = V_{CC}, GND, 2.5V or 0.4V			±5.1	±10	µA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V				−120	mA
LVDS DRIVER DC SPECIFICATIONS							
V_{OD}	Differential Output Voltage	R_L = 100Ω		250	290	450	mV
ΔV_{OD}	Change in V_{OD} between					35	mV
	Complimentary Output States						
V_{OS}	Offset Voltage[1]			1.1	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between					35	mV
	Complimentary Output States						
V_{OH}	High Level Output Voltage				1.3	1.6	V
V_{OL}	Low Level Output Voltage			0.9	1.01		V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω			−2.9	−5	mA
I_{OZ}	Output TRI-STATE® Current	$\overline{\text{Power Down}}$ = 0V, V_{OUT} = 0V or V_{CC}			±1	±10	µA
TRANSMITTER SUPPLY CURRENT							
I_{CCTW}	Transmitter Supply Current,	R_L = 100Ω, C_L = 5 pF,	f = 32.5 MHz		34	51	mA
	Worst Case	Worst Case Pattern (Figure 2, Figure 3)	f = 37.5 MHz		36	53	mA

(1) V_{OS} previously referred as V_{CM}

Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{CCTG}	Transmitter Supply Current, 16 Grayscale	R_L = 100Ω, C_L = 5 pF, Grayscale Pattern (Figure 3, Figure 4)	f = 32.5 MHz		27	47	mA
			f = 37.5 MHz		28	48	mA
I_{CCTZ}	Transmitter Supply Current, Power Down	$\overline{\text{Power Down}}$ = Low			1	25	µA

Transmitter Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
LLHT	LVDS Low-to-High Transition Time (Figure 4)			0.75	1.5	ns
LHLT	LVDS High-to-Low Transition Time (Figure 4)			0.75	1.5	ns
TCIT	TxCLK IN Transition Time (Figure 5)				8	ns
TCCS	TxOUT Channel-to-Channel Skew (1) (Figure 6)				350	ps
TPPos0	Transmitter Output Pulse Position for Bit 0 (Figure 12)	f = 20 MHz	−200	150	350	ps
TPPos1	Transmitter Output Pulse Position for Bit 1		6.3	7.2	7.5	ns
TPPos2	Transmitter Output Pulse Position for Bit 2		12.8	13.6	14.6	ns
TPPos3	Transmitter Output Pulse Position for Bit 3		20	20.8	21.5	ns
TPPos4	Transmitter Output Pulse Position for Bit 4		27.2	28	28.5	ns
TPPos5	Transmitter Output Pulse Position for Bit 5		34.5	35.2	35.6	ns
TPPos6	Transmitter Output Pulse Position for Bit 6		42.2	42.6	42.9	ns
TPPos0	Transmitter Output Pulse Position for Bit 0 (Figure 12)	f = 40 MHz	−100	100	300	ps
TPPos1	Transmitter Output Pulse Position for Bit 1		2.9	3.3	3.9	ns
TPPos2	Transmitter Output Pulse Position for Bit 2		6.1	6.6	7.1	ns
TPPos3	Transmitter Output Pulse Position for Bit 3		9.7	10.2	10.7	ns
TPPos4	Transmitter Output Pulse Position for Bit 4		13	13.5	14.1	ns
TPPos5	Transmitter Output Pulse Position for Bit 5		17	17.4	17.8	ns
TPPos6	Transmitter Output Pulse Position for Bit 6		20.3	20.8	21.4	ns
TCIP	TxCLK IN Period (Figure 7)		25	T	50	ns
TCIH	TxCLK IN High Time(Figure 7)		0.35T	0.5T	0.65T	ns
TCIL	TxCLK IN Low Time (Figure 7)		0.35T	0.5T	0.65T	ns
TSTC	TxIN Setup to TxCLK IN (Figure 7)	f = 20 MHz	14			ns
		f = 40 MHz	8			ns
THTC	TxIN Hold to TxCLK IN (Figure 7)		2.5	2		ns
TCCD	TxCLK IN to TxCLK OUT Delay @ 25°C, V_{CC} = 5.0V (Figure 8)		5		9.7	ns
TPLLS	Transmitter Phase Lock Loop Set (Figure 9)				10	ms
TPDD	Transmitter Powerdown Delay (Figure 11)				100	ns

(1) This limit based on bench characterization.

AC Timing Diagrams

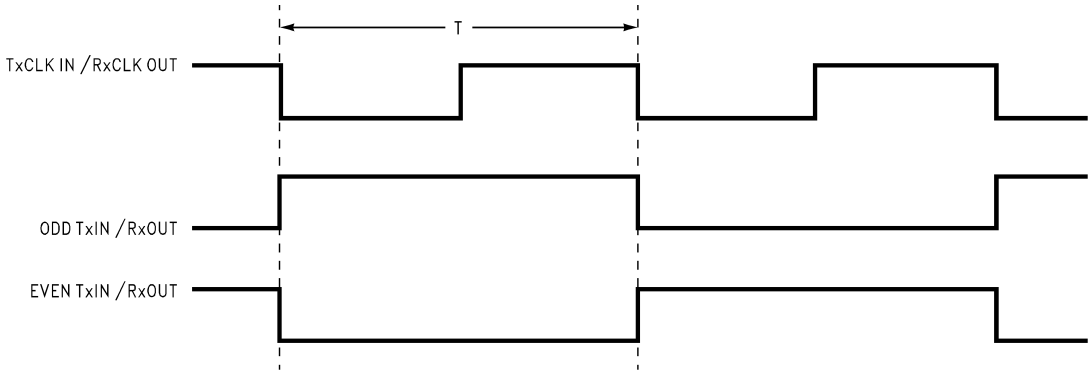
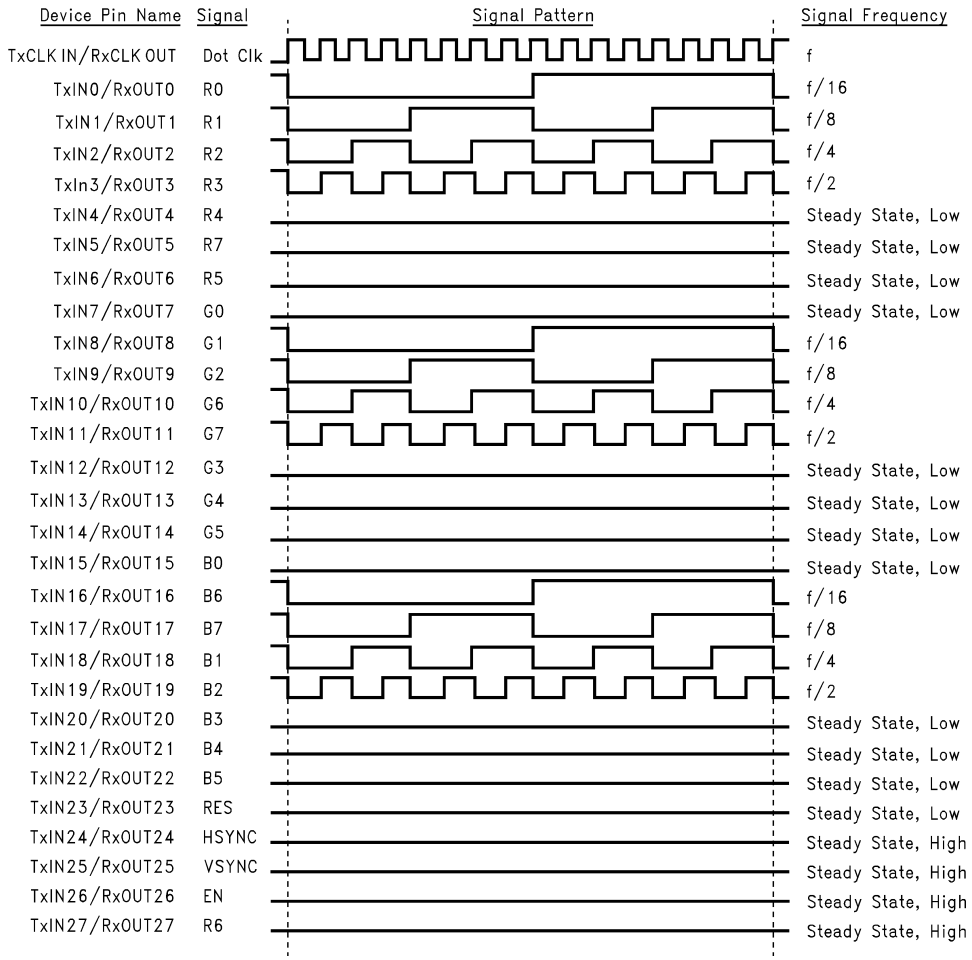


Figure 2. "Worst Case" Test Pattern



(1) The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

(2) The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

(3) Figure 2 and Figure 3 show a rising edge data strobe (TxCLK IN/RxCLK OUT).

(4) Recommended pin to signal mapping. Customer may choose to define differently.

Figure 3. "16 Grayscale" Test Pattern

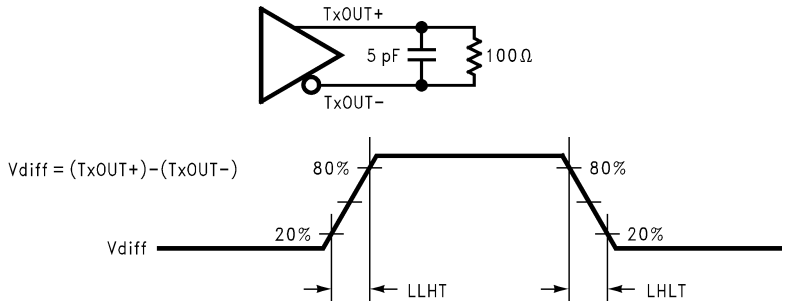


Figure 4. DS90CR581 (Transmitter) LVDS Output Load and Transition Timing

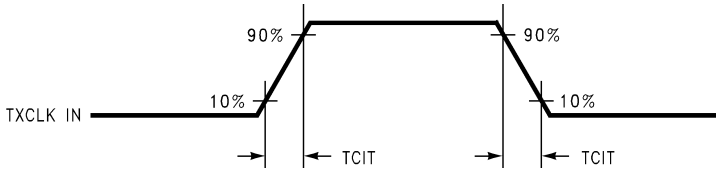
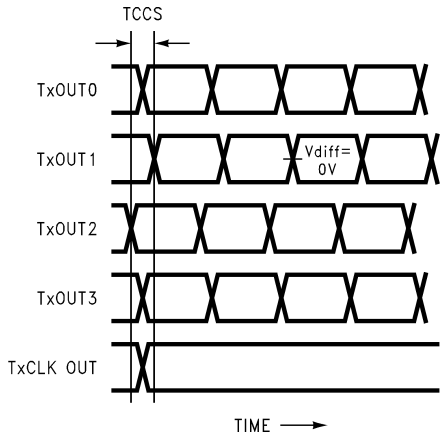


Figure 5. DS90CR581 (Transmitter) Input Clock Transition Time



(1) Measurements at V_{diff} = 0V

(2) TCCS measured between earliest and latest initial LVDS edges.

(3) TxCLK OUT Differential High→Low Edge for DS90CF581
TxCLK OUT Differential Low→High Edge for DS90CR581

Figure 6. DS90CR581 (Transmitter) Channel-to-Channel Skew

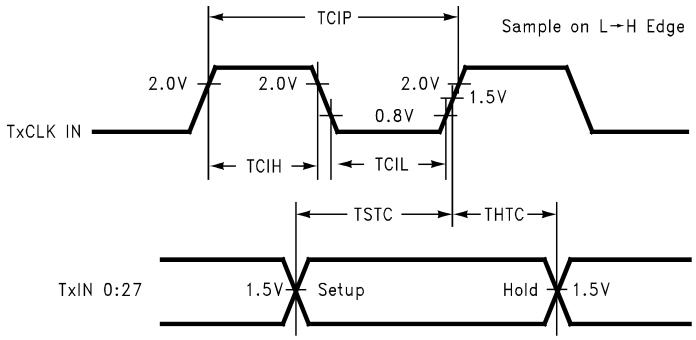


Figure 7. DS90CR581 (Transmitter) Setup/Hold and High/Low Times

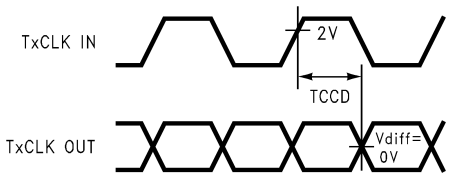


Figure 8. DS90CR581 (Transmitter) Clock In to Clock Out Delay

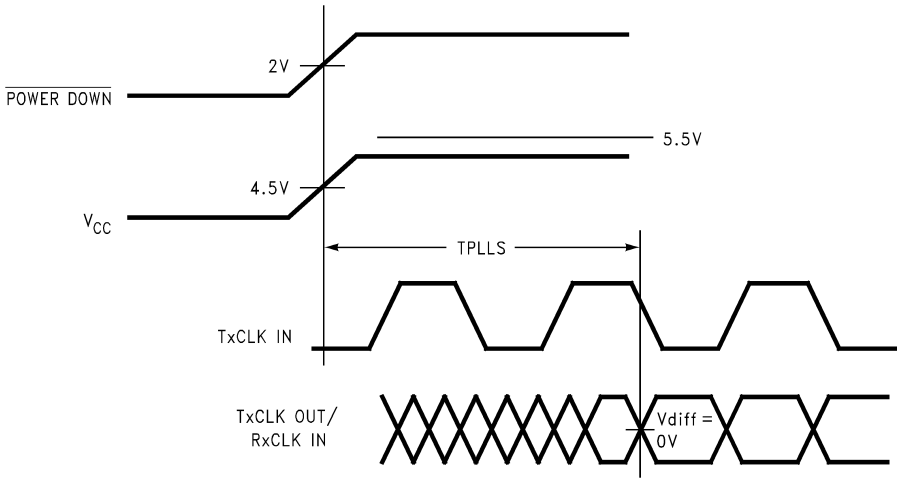


Figure 9. DS90CR581 (Transmitter) Phase Lock Loop Set Time

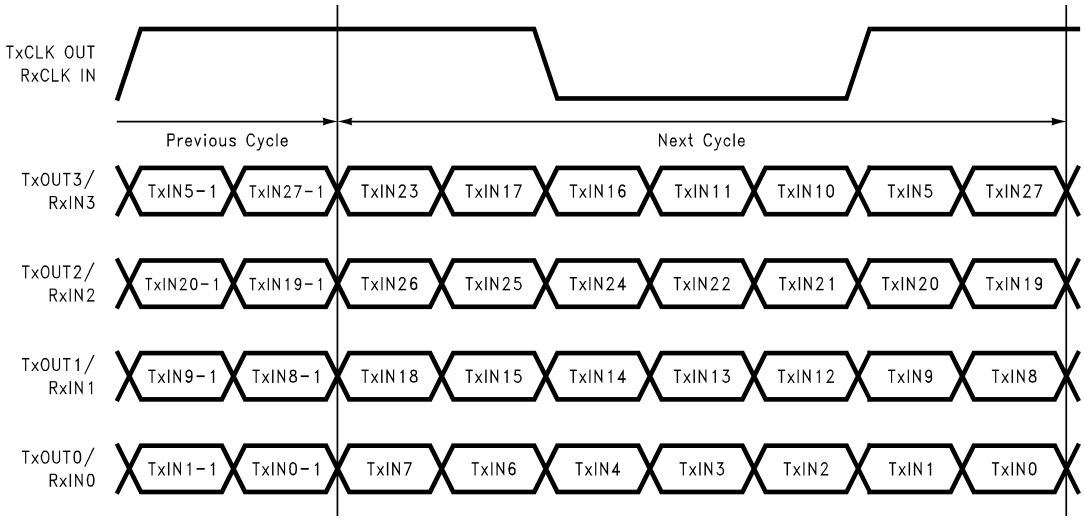


Figure 10. 28 Parallel TTL Data Inputs Mapped to LVDS Outputs (DS90CR581)

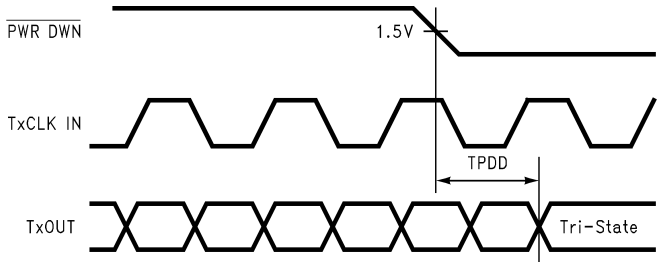


Figure 11. Transmitter Powerdown Delay

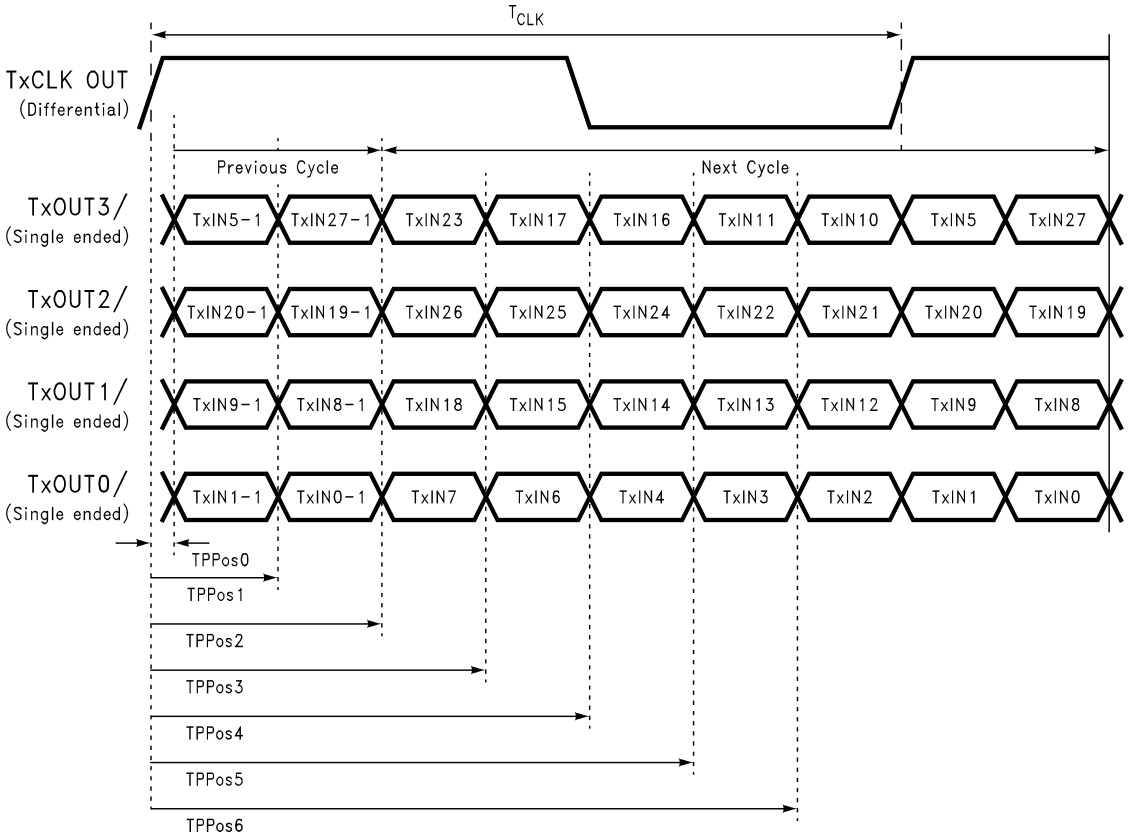


Figure 12. Transmitter LVDS Output Pulse Position Measurement

DS90CR581 Pin Description—FPD Link Transmitter

Pin Name	I/O	No.	Description
TxIN	I	28	TTL Level input. This includes: 8 Red, 8 Green, 8 Blue, and 4 control lines (FPLINE, FPFRAME, DRDY, CNTL). (Also referred to as HSYNC, VSYNC and DATA ENABLE)
TxOUT+	O	4	Positive LVDS differential data output
TxOUT−	O	4	Negative LVDS differential data output
FPSHIFT IN	I	1	TTL level clock input. The rising edge acts as data strobe.
TxCLK OUT+	O	1	Positive LVDS differential clock output
TxCLK OUT−	O	1	Negative LVDS differential clock output
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down.
V_{CC}	I	4	Power supply pins for TTL inputs
GND	I	5	Ground pins for TTL inputs
PLL V_{CC}	I	1	Power supply pin for PLL
PLL GND	I	2	Ground pins for PLL
LVDS V_{CC}	I	1	Power supply pin for LVDS outputs
LVDS GND	I	3	Ground pins for LVDS outputs

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	9

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