DS90CR583/DS90CR584 LVDS 24-Bit Color Flat Panel Display (FPD) Link— 65 MHz

Check for Samples: DS90CR583, DS90CR584

FEATURES

- **20 to 65 MHz Shift clk Support**
- **Up to 227 Mbytes/s Bandwidth**
- **Cable Size is Reduced to Save Cost**
- **290 mV Swing LVDS Devices for Low EMI**
- **Low Power CMOS Design (< 550 mW typ)**
- **Power-Down Mode Saves Power (< 0.25 mW)**
- **PLL Requires No External Components**
- **Low Profile 56-lead TSSOP Package**
- **Rising Edge Data Strobe**
- **Compatible with TIA/EIA-644 LVDS Standard**
- **Single Pixel Per Clock XGA (1024 x 768)**
- **Supports VGA, SVGA, XGA and Higher**
- **1.8 Gbps Throughput**

DESCRIPTION

The DS90CR583 transmitter converts 28 bits of CMOS/TTL data into four LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. The DS90CR584 receiver converts the LVDS data streams back into 28 bits of CMOS/TTL data. At a transmit clock frequency of 65 MHz, 24 bits of RGB data and 4 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY, CONTROL) are transmitted at a rate of 455 Mbps per LVDS data channel. Using a 65 MHz clock, the data throughput is 227 Mbytes per second. These devices are offered with rising edge data strobes for convenient interface with a variety of graphics and LCD panel controllers.

This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

BLOCK DIAGRAM

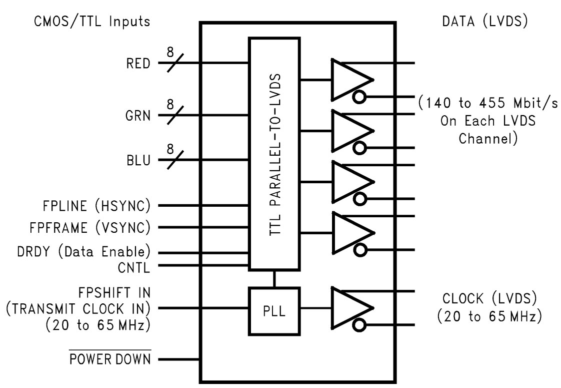


Figure 1. DS90CR583
See Package Number DGG

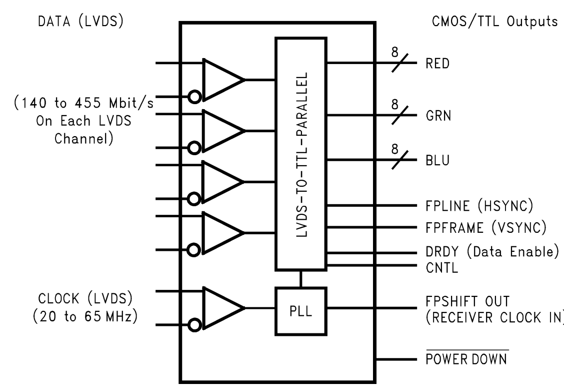
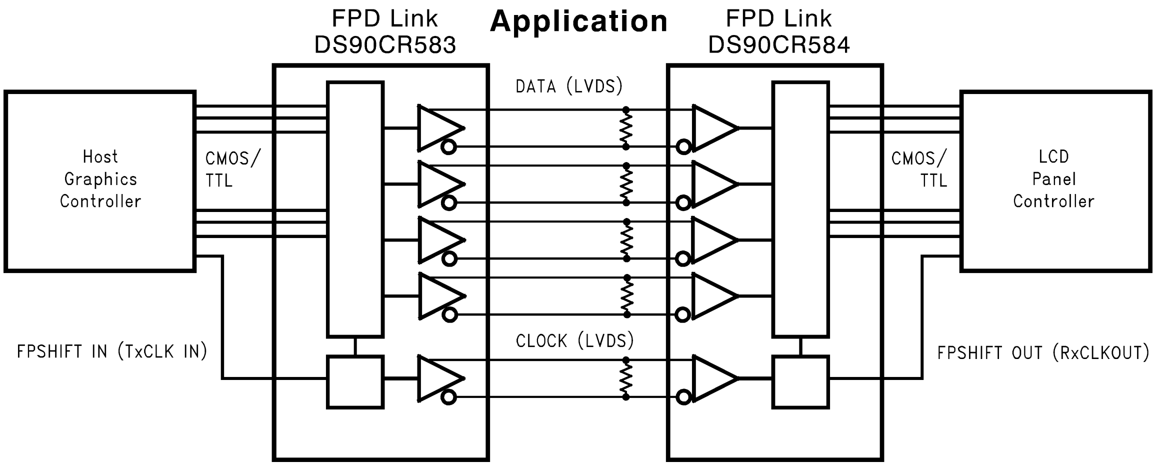


Figure 2. DS90CR584
See Package Number DGG

Application



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Supply Voltage (V_{CC})			−0.3V to +6V
CMOS/TTL Input Voltage			−0.3V to (V_{CC} + 0.3V)
CMOS/TTL Output Voltage			−0.3V to (V_{CC} + 0.3V)
LVDS Receiver Input Voltage			−0.3V to (V_{CC} + 0.3V)
LVDS Driver Output Voltage			−0.3V to (V_{CC} + 0.3V)
LVDS Output Short Circuit Duration			Continuous
Junction Temperature			+150°C
Storage Temperature			−65°C to +150°C
Lead Temperature (Soldering, 4 sec)			+260°C
Maximum Power Dissipation @ 25°C	DGG (TSSOP) Package:	DS90CR583	1.63W
		DS90CR584	1.61W
	Package Derating:	DS90CR583	12.5 mW/°C above +25°C
		DS90CR584	12.4 mW/°C above +25°C
This device does not meet 2000V ESD rating(3) .			

(1) “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits. “Electrical Characteristics” specify conditions for device operation.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) ESD Rating: HBM (1.5 kΩ, 100 pF) PLL V_{CC} ≥ 1000V All other pins ≥ 2000V EIAJ (0Ω, 200 pF) ≥ 150V

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	4.75	5.0	5.25	V
Operating Free Air Temperature (T_A)	−10	+25	+70	°C
Receiver Input Range	0		2.4	V
Supply Noise Voltage (V_{CC})			100	mV_{P-P}

ELECTRICAL CHARACTERISTICS

over opeOver recommended operating supply and temperature ranges unless otherwise specifiedrating free-air temperature range (unless otherwise noted)

Symb	Parameter	Conditions	Min	Typ	Max	Units
CMOS/TTL DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V

ELECTRICAL CHARACTERISTICS (continued)

over opeOver recommended operating supply and temperature ranges unless otherwise specifiedrating free-air temperature range (unless otherwise noted)

Symb	Parameter	Conditions		Min	Typ	Max	Units
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA		3.8	4.9		V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA			0.1	0.3	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = V_{CC}, GND, 2.5V or 0.4V			±5.1	±10	μA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V				−120	mA
LVDS DRIVER DC SPECIFICATIONS							
V_{OD}	Differential Output Voltage	R_L = 100Ω		250	290	450	mV
ΔV_{OD}	Change in V_{OD} between Complementary Output States					35	mV
ΔV_{CM}	Change in V_{CM} between Complementary Output States					35	mV
V_{OL}	Low Level Output Voltage			0.9	1.01		V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω			−2.9	−5	mA
I_{OZ}	Output TRI-STATE Current	$\overline{\text{Power Down}}$ = 0V, V_{OUT} = 0V or V_{CC}			±1	±10	μA
LVDS RECEIVER DC SPECIFICATIONS							
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V				+100	mV
V_{TL}	Differential Input Low Threshold			−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V	V_{CC} = 5.5V			±10	μA
		V_{IN} = 0V				±10	μA
TRANSMITTER SUPPLY CURENT							
I_{CCTW}	Transmitter Supply Current, Worst Case	R_L = 100Ω, C_L = 5 pF, Worst Case Pattern (Figure 3, Figure 5)	f = 32.5 MHz		49	63	mA
			f = 37.5 MHz		51	64	mA
			f = 65 MHz		70	84	mA
I_{CCTG}	Transmitter Supply Current, 16 Grayscale	R_L = 100Ω, C_L = 5 pF, 16 Grayscale Pattern (Figure 4, Figure 5)	f = 32.5 MHz		40	55	mA
			f = 37.5 MHz		41	55	mA
			f = 65 MHz		55	67	mA
I_{CCTZ}	Transmitter Supply Current, Power Down	$\overline{\text{Power Down}}$ = Low			1	10	μA
I_{CCRW}	Receiver Supply Current, Worst Case	C_L = 8 pF, Worst Case Pattern (Figure 3, Figure 6)	f = 32.5 MHz		64	77	mA
			f = 37.5 MHz		70	85	mA
			f = 65 MHz		110	140	mA
I_{CCRG}	Receiver Supply Current, 16 Grayscale	C_L = 8 pF, 16 Grayscale Pattern (Figure 4, Figure 6)	f = 32.5 MHz		35	55	mA
			f = 37.5 MHz		37	55	mA
			f = 65 MHz		55	67	mA
I_{CCRZ}	Receiver Supply Current, Power Down	$\overline{\text{Power Down}}$ = Low			1	10	μA

Transmitter Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units
LLHT	LVDS Low-to-High Transition Time (Figure 5)		0.75	1.5	ns
LHLT	LVDS High-to-Low Transition Time (Figure 5)		0.75	1.5	ns
TCIT	TxCLK IN Transition Time (Figure 7)			8	ns
TCCS	TxOUT Channel-to-Channel Skew (1) (Figure 8)			350	ps
TCCD	TxCLK IN to TxCLK OUT Delay @ 25°C, V_{CC} = 5.0V (Figure 11)	3.5		8.5	ns

(1) This limit based on bench characterization.

Transmitter Switching Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
TCIP	TxCLK IN Period (Figure 9)		15	T	50	ns
TCIH	TxCLK IN High Time (Figure 9)		0.35T	0.5T	0.65T	ns
TCIL	TxCLK IN Low Time (Figure 9)		0.35T	0.5T	0.65T	ns
TSTC	TxIN Setup to TxCLK IN (Figure 9)	f = 65 MHz	5	3.5		ns
THTC	TxIN Hold to TxCLK IN (Figure 9)		2.5	1.5		ns
TPDD	Transmitter Powerdown Delay (Figure 20)				100	ns
TPLLS	Transmitter Phase Lock Loop Set (Figure 13)				10	ms
TPPos0	Transmitter Output Pulse Position 0 (Figure 15)		−0.30	0	0.30	ns
TPPos1	Transmitter Output Pulse Position 1		1.70	1/7 T_{clk}	2.50	ns
TPPos2	Transmitter Output Pulse Position 2		3.60	2/7 T_{clk}	4.50	ns
TPPos3	Transmitter Output Pulse Position 3		5.90	3/7 T_{clk}	6.75	ns
TPPos4	Transmitter Output Pulse Position 4		8.30	4/7 T_{clk}	9.00	ns
TPPos5	Transmitter Output Pulse Position 5		10.40	5/7 T_{clk}	11.10	ns
TPPos6	Transmitter Output Pulse Position 6		12.70	6/7 T_{clk}	13.40	ns

Receiver Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter		Min	Typ	Max	Units
CLHT	CMOS/TTL Low-to-High Transition Time (Figure 6)			2.5	4.0	ns
CHLT	CMOS/TTL High-to-Low Transition Time (Figure 6)			2.0	3.5	ns
RCOP	RxCLK OUT Period		15	T	50	ns
RCOH	RxCLK OUT High Time	f = 65 MHz	3.8	5		ns
RCOL	RxCLK OUT Low Time	f = 65 MHz	7.8	9		ns
RSRC	RxOUT Setup to RxCLK OUT	f = 65 MHz	2.5	4.2		ns
RHRC	RxOUT Hold to RxCLK OUT	f = 65 MHz	4.0	5.2		ns
RCCD	RxCLK IN to RxCLK OUT Delay @ 25°C, V_{CC} = 5.0V (Figure 12)		6.4		10.7	ns
RPLLS	Receiver Phase Lock Loop Set (Figure 14)				10	ms
RSKM	RxIN Skew Margin [(1)] (Figure 16)	V_{CC} = 5V, T_A =25°C	600			ps
RPDD	Receiver Powerdown (Figure 19)				1	µs

(1) Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account transmitter output skew (TCCS) and the setup and hold time (internal data sampling window), allowing for LVDS cable skew dependent on type/length and source clock (TxCLK IN) jitter RSKM ≥ cable skew (type, length) + source clock jitter (cycle to cycle)

AC Timing Diagrams

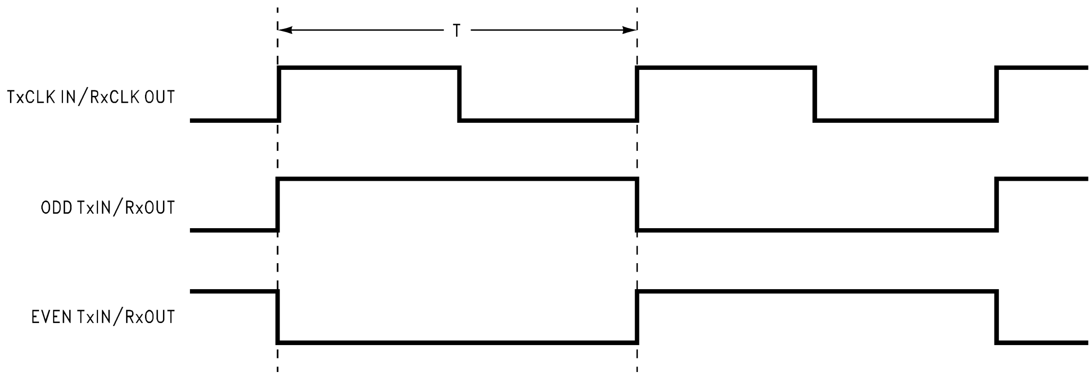
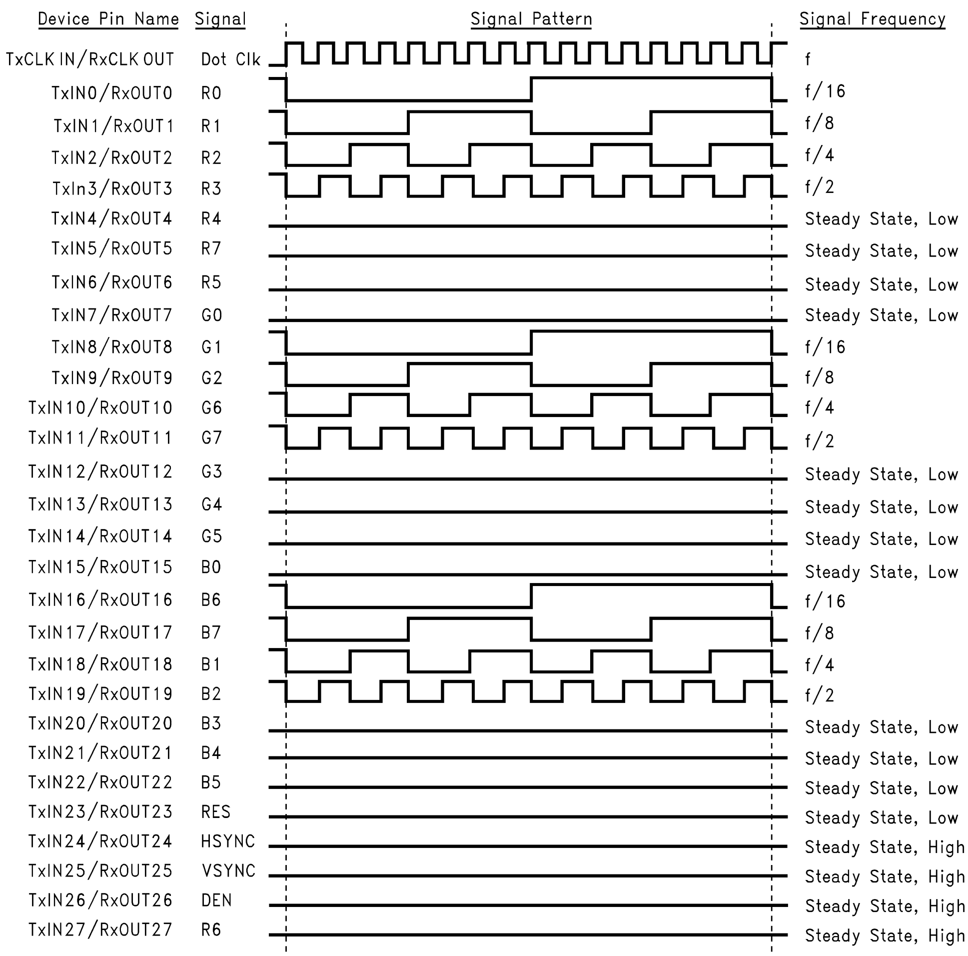


Figure 3. “Worst Case” Test Pattern



(1) The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

(2) The 16 grayscale test pattern tests device power consumption for a “typical” LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

(3) Figure 3 and Figure 4 show a falling edge data strobe (TxCLK IN/RxCLK OUT).

(4) Recommended pin to signal mapping. Customer may choose to define differently.

Figure 4. “16 Grayscale” Test Pattern

Figure 5. DS90CR583 (Transmitter) LVDS Output Load and Transition Times

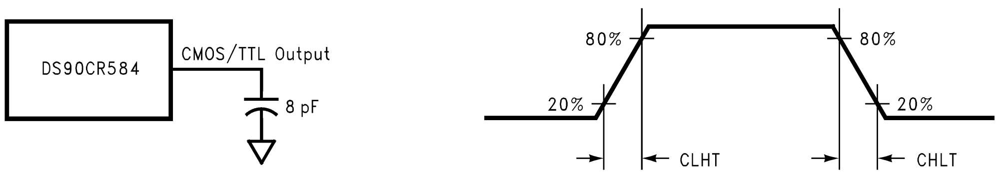


Figure 6. DS90CR584 (Receiver) CMOS/TTL Output Load and Transition Times

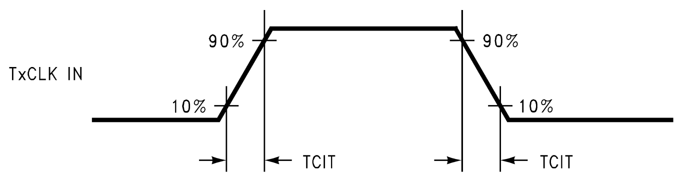
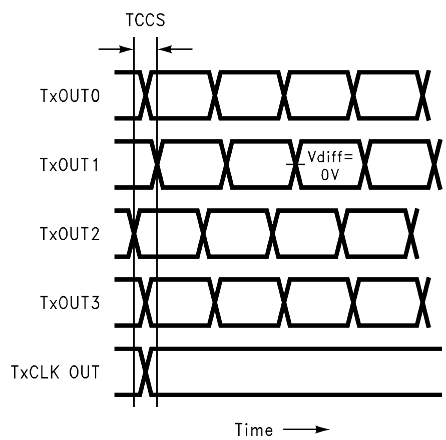


Figure 7. DS90CR583 (Transmitter) Input Clock Transition Time



Note: Measurements at Vdiff = 0V
Note: TCSS measured between earliest and latest LVDS edges.
Note: TxCLK Differential High→Low Edge

Figure 8. DS90CR583 (Transmitter) Channel-to-Channel Skew and Pulse Width

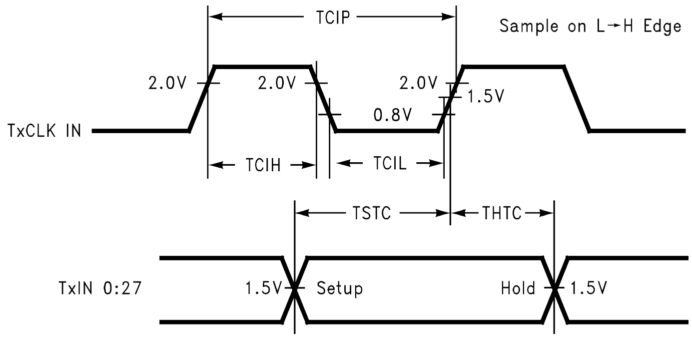


Figure 9. DS90CR583 (Transmitter) Setup/Hold and High/Low Times

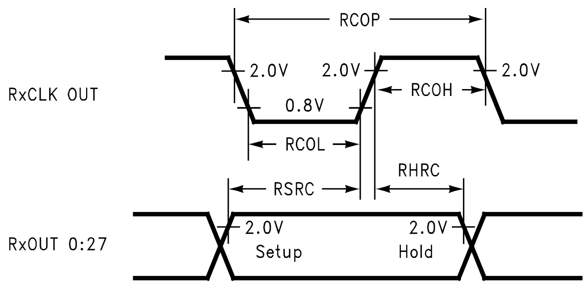


Figure 10. DS90CR584 (Receiver) Clock In to Clock Out Delay

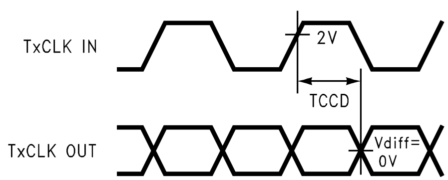


Figure 11. DS90CR583 (Transmitter) Clock In to Clock Out Delay

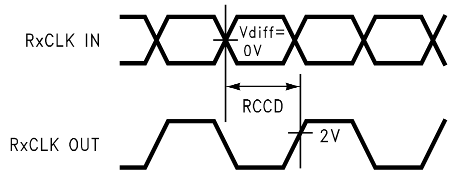


Figure 12. DS90CR584 (Receiver) Clock In to Clock Out Delay

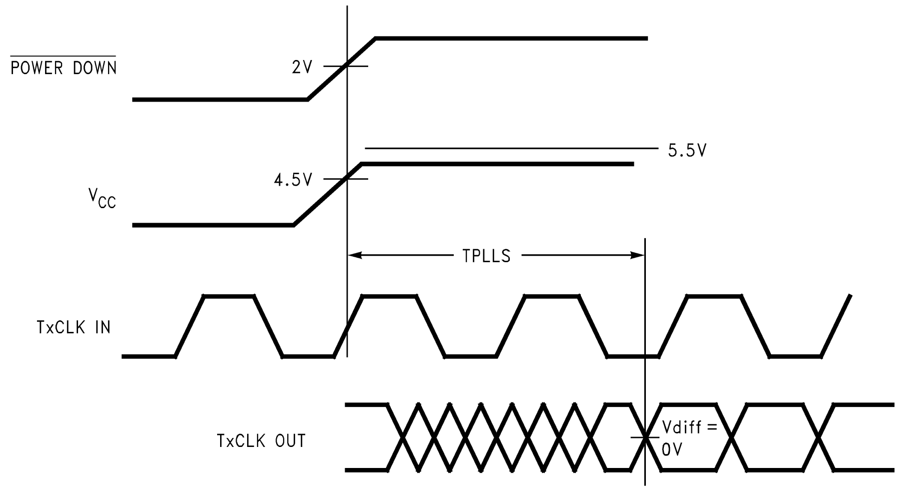


Figure 13. DS90CR583 (Transmitter) Phase Lock Loop Set Time

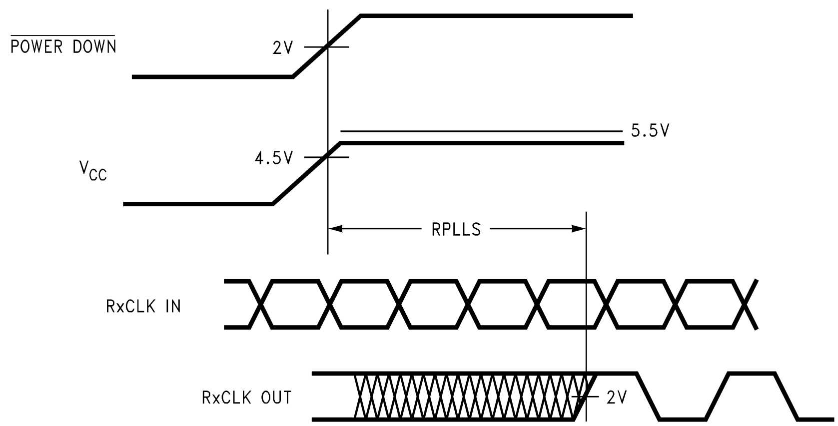


Figure 14. DS90CR584 (Receiver) Phase Lock Loop Set Time

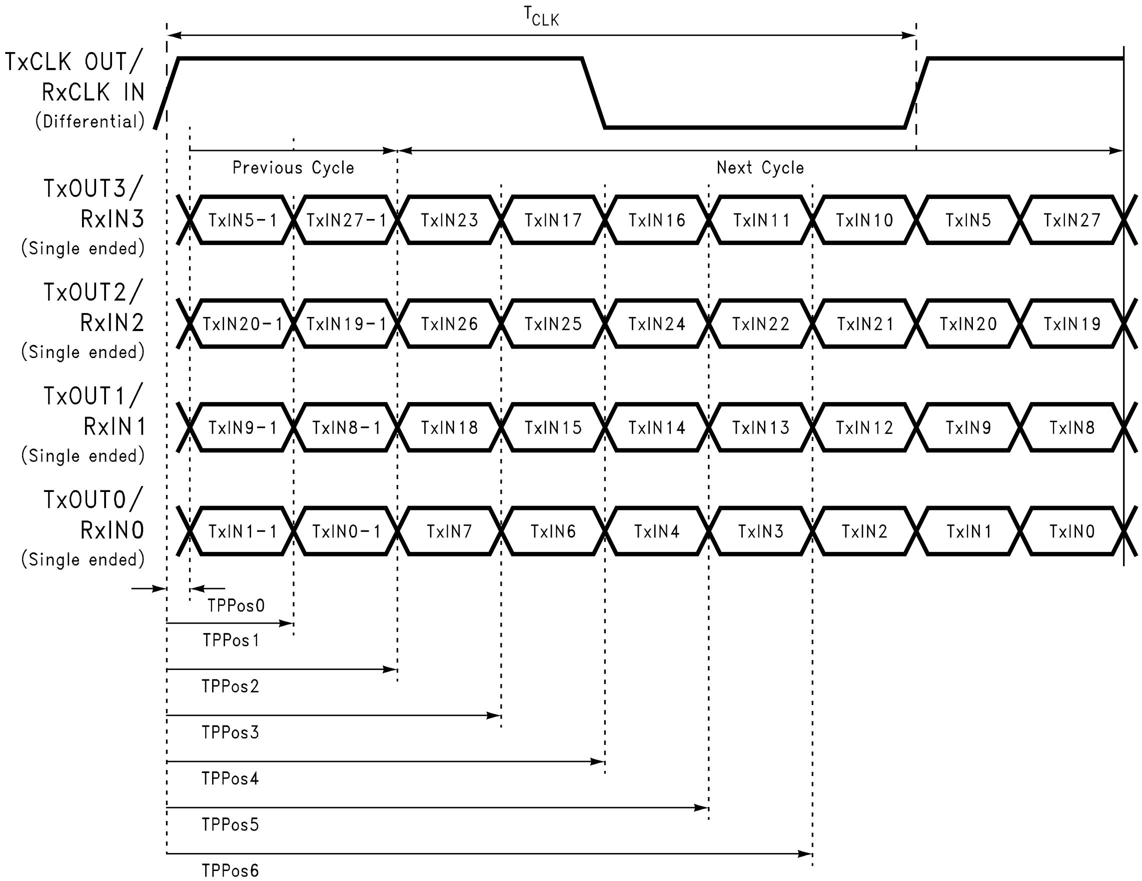
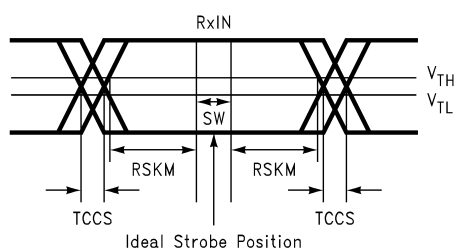


Figure 15. Transmitter LVDS Output Pulse Position Measurement



SW—Setup and Hold Time (Internal Data Sampling Window)
TCCS—Transmitter Output Skew
RSKM ≥ Cable Skew (type, length) + Source Clock Jitter (cycle to cycle)
Cable Skew—typically 10 ps–40 ps per foot

Figure 16. Receiver LVDS Input Skew Margin

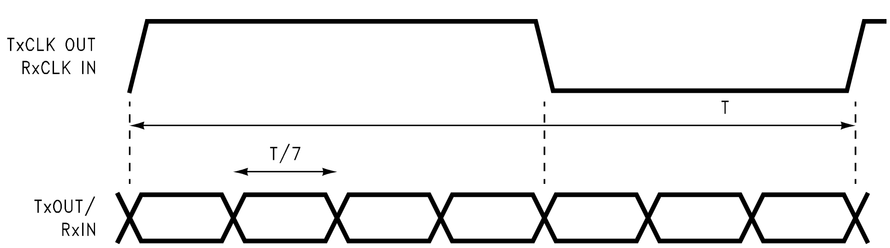


Figure 17. Seven Bits of LVDS in One Clock Cycle

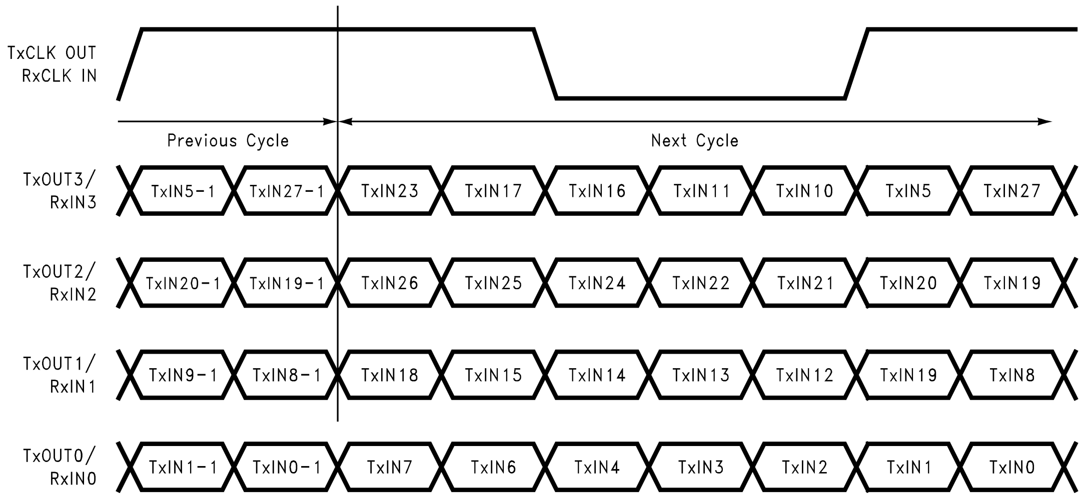


Figure 18. Parallel TTL Data Inputs Mapped to LVDS Outputs (DS90CR583)

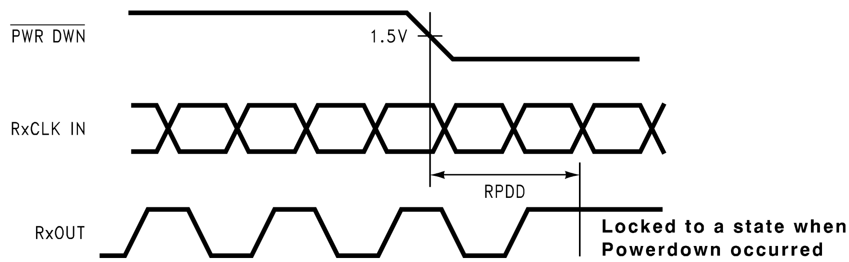


Figure 19. Receiver Powerdown Delay

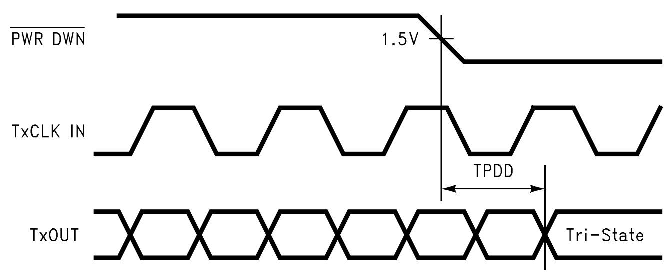


Figure 20. Transmitter Powerdown Delay

DS90CR583 Pin Descriptions—FPD Link Transmitter

Pin Name	I/O	No.	Description
TxIN	I	28	TTL level input. This includes: 8 Red, 8 Green, 8 Blue, and 4 control lines—FPLINE, FPFRAME, DRDY and CNTL (also referred to as HSYNC, VSYNC, Data Enable, CNTL)
TxOUT+	O	4	Positive LVDS differential data output
TxOUT−	O	4	Negative LVDS differential data output
FPSHIFT IN	I	1	TTL level clock input. The falling edge acts as data strobe
TxCLK OUT+	O	1	Positive LVDS differential clock output
TxCLK OUT−	O	1	Negative LVDS differential clock output
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down
V_{CC}	I	4	Power supply pins for TTL inputs
GND	I	5	Ground pins for TTL inputs

DS90CR583 Pin Descriptions—FPD Link Transmitter (continued)

Pin Name	I/O	No.	Description
PLL V_{CC}	I	1	Power supply pin for PLL
PLL GND	I	2	Ground pins for PLL
LVDS V_{CC}	I	1	Power supply pin for LVDS outputs
LVDS GND	I	3	Ground pins for LVDS outputs

DS90CR584 Pin Descriptions—FPD Link Receiver

Pin Name	I/O	No.	Description
RxIN+	I	4	Positive LVDS differential data inputs
RxIN−	I	4	Negative LVDS differential data inputs
RxOUT	O	28	TTL level data outputs. This includes: 8 Red, 8 Green, 8 Blue, and 4 control lines—FPLINE, FPFRAME, DRDY and CNTL (also referred to as HSYNC, VSYNC, Data Enable, CNTL)
RxCLK IN+	I	1	Positive LVDS differential clock input
RxCLK IN−	I	1	Negative LVDS differential clock input
FPSHIFT OUT	O	1	TTL level clock output. The falling edge acts as data strobe
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) maintains the receiver outputs in the previous state
V_{CC}	I	4	Power supply pins for TTL outputs
GND	I	5	Ground pins for TTL outputs
PLL V_{CC}	I	1	Power supply for PLL
PLL GND	I	2	Ground pin for PLL
LVDS V_{CC}	I	1	Power supply pin for LVDS inputs
LVDS GND	I	3	Ground pins for LVDS inputs

Connection Diagram

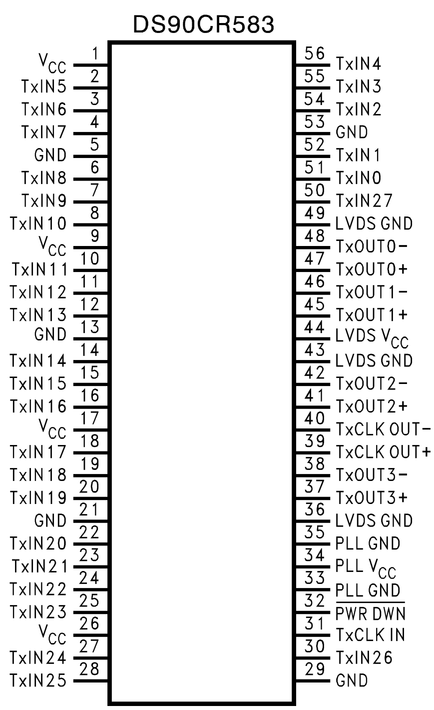


Figure 21. 56 Pin TSSOP
See Package Number DGG

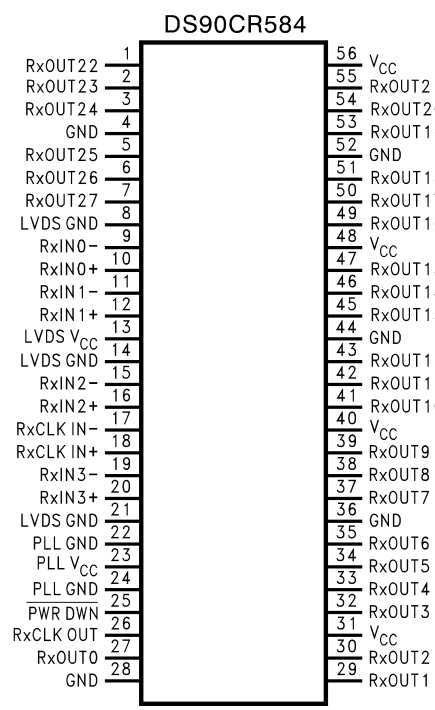


Figure 22. 56 Pin TSSOP
See Package Number DGG

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B **Page**

- Changed layout of National Data Sheet to TI format 11

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