

DS92LV1224 30-66 MHz 10 Bit Bus LVDS Deserializer

Check for Samples: [DS92LV1224](#)

FEATURES

- 30–66 MHz Single 1:10 Deserializer with 300–660 Mb/s Throughput
- Robust Bus LVDS Serial Data Transmission with Embedded Clock for Exceptional Noise Immunity and Low EMI
- Clock Recovery from PLL Lock to Random Data Patterns
- Ensured Transition Every Data Transfer Cycle
- Low Power Consumption < 300 mW (typ) at 66 MHz
- Single Differential Pair Eliminates Multi-Channel Skew
- Flow-Through Pinout for Easy PCB Layout
- Synchronization Mode and LOCK Indicator
- Programmable Edge Trigger on Clock
- High Impedance on Receiver Inputs when Power is Off
- Small 28-Lead SSOP Package

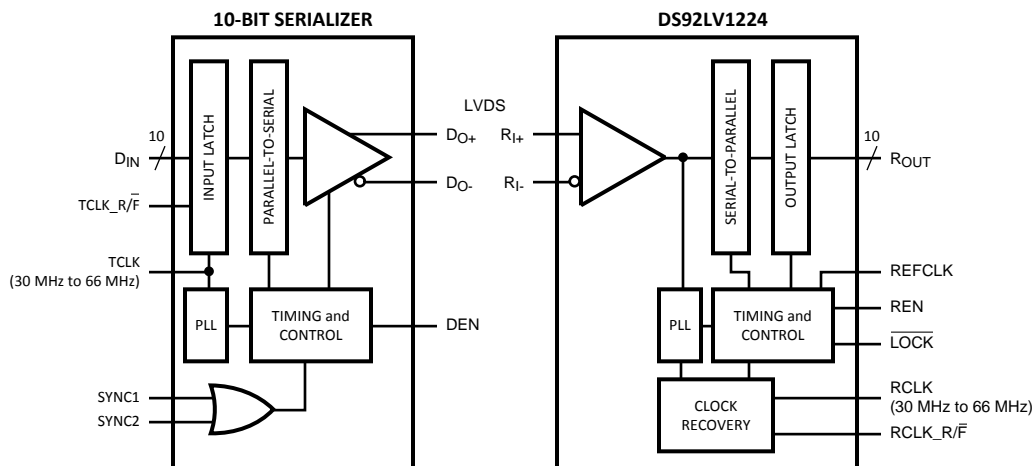
DESCRIPTION

The DS92LV1224 is a 300 to 660 Mb/s deserializer for high-speed unidirectional serial data transmission over FR-4 printed circuit board backplanes and balanced copper cables. It receives the Bus LVDS serial data stream from a compatible 10-bit serializer, transforms it back into a 10-bit wide parallel data bus and recovers parallel clock. This single serial data stream simplifies PCB design and reduces PCB cost by narrowing data paths that in turn reduce PCB size and number of layers. The single serial data stream also reduces cable size, the number of connectors, and eliminates clock-to-data and data-to-data skew.

The DS92LV1224 works well with Bus LVDS 10-bit serializers within its specified frequency operating range. It features low power consumption, and high impedance outputs in power down mode.

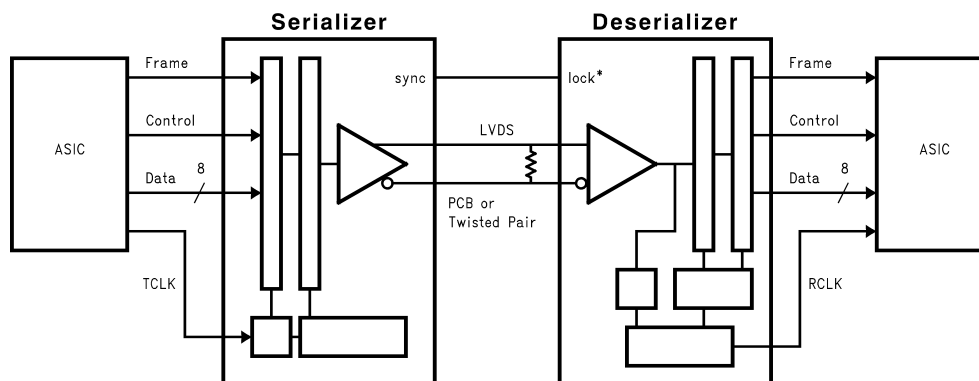
The DS92LV1224 was designed with the flow-through pinout and is available in a space saving 28-lead SSOP package.

Block Diagrams



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Functional Description

The DS92LV1224 is a 10-bit Deserializer device which together with a compatible serializer (i.e. DS92LV1023E) forms a chipset designed to transmit data over FR-4 printed circuit board backplanes and balanced copper cables at clock speeds from 30 MHz to 66 MHz.

The chipset has three active states of operation: Initialization, Data Transfer, and Resynchronization; and two passive states: Powerdown and TRI-STATE.

The following sections describe each operation and passive state.

Initialization

Initialization of both devices must occur before data transmission begins. Initialization refers to synchronization of the Serializer and Deserializer PLL's to local clocks, which may be the same or separate. Afterwards, synchronization of the Deserializer to Serializer occurs.

Step 1: When you apply V_{CC} to both Serializer and/or Deserializer, the respective outputs enter TRI-STATE, and on-chip power-on circuitry disables internal circuitry. When V_{CC} reaches V_{CCOK} (2.5V) the PLL in each device begins locking to a local clock. For the Serializer, the local clock is the transmit clock (TCLK) provided by the source ASIC or other device. For the Deserializer, you must apply a local clock to the REFCLK pin.

The Serializer outputs remain in TRI-STATE while the PLL locks to the TCLK. After locking to TCLK, the Serializer is now ready to send data or SYNC patterns, depending on the levels of the SYNC1 and SYNC2 inputs or a data stream. The SYNC pattern sent by the Serializer consists of six ones and six zeros switching at the input clock rate.

Note that the Deserializer \overline{LOCK} output will remain high while its PLL locks to the incoming data or to SYNC patterns on the input.

Step 2: The Deserializer PLL must synchronize to the Serializer to complete initialization. The Deserializer will lock to non-repetitive data patterns. However, the transmission of SYNC patterns enables the Deserializer to lock to the Serializer signal within a specified time.

The user's application determines control of the SYNC1 and SYNC 2 pins. One recommendation is a direct feedback loop from the \overline{LOCK} pin. Under all circumstances, the Serializer stops sending SYNC patterns after both SYNC inputs return low.

When the Deserializer detects edge transitions at the Bus LVDS input, it will attempt to lock to the embedded clock information. When the Deserializer locks to the Bus LVDS clock, the \overline{LOCK} output will go low. When \overline{LOCK} is low, the Deserializer outputs represent incoming Bus LVDS data.

Data Transfer

After initialization, the Serializer will accept data from inputs DIN0–DIN9. The Serializer uses the TCLK input to latch incoming Data. The TCLK_R/F pin selects which edge the Serializer uses to strobe incoming data. TCLK_R/F high selects the rising edge for clocking data and low selects the falling edge. If either of the SYNC inputs is high for $5 \cdot TCLK$ cycles, the data at DIN0–DIN9 is ignored regardless of clock edge.

After determining which clock edge to use, a start and stop bit, appended internally, frame the data bits in the register. The start bit is always high and the stop bit is always low. The start and stop bits function as the embedded clock bits in the serial stream.

The Serializer transmits serialized data and clock bits (10+2 bits) from the serial data output (DO±) at 12 times the TCLK frequency. For example, if TCLK is 66 MHz, the serial rate is $66 \times 12 = 792$ Mega-bits-per-second. Since only 10 bits are from input data, the serial “payload” rate is 10 times the TCLK frequency. For instance, if TCLK = 66 MHz, the payload data rate is $66 \times 10 = 660$ Mbps. The data source provides TCLK and must be in the range of 30 MHz to 66 MHz nominal.

The Serializer outputs (DO±) can drive a point-to-point connection or in limited multi-point or multi-drop backplanes. The outputs transmit data when the enable pin (DEN) is high, PWRDN = high, and SYNC1 and SYNC2 are low. When DEN is driven low, the Serializer output pins will enter TRI-STATE.

When the Deserializer synchronizes to the Serializer, the $\overline{\text{LOCK}}$ pin is low. The Deserializer locks to the embedded clock and uses it to recover the serialized data. ROUT data is valid when $\overline{\text{LOCK}}$ is low. Otherwise ROUT0–ROUT9 is invalid.

The ROUT0–ROUT9 pins use the RCLK pin as the reference to data. The polarity of the RCLK edge is controlled by the RCLK_R/F input. See [Figure 6](#).

ROUT(0-9), $\overline{\text{LOCK}}$ and RCLK outputs will drive a maximum of three CMOS input gates (15 pF load) with a 66 MHz clock.

Resynchronization

When the Deserializer PLL locks to the embedded clock edge, the Deserializer $\overline{\text{LOCK}}$ pin asserts a low. If the Deserializer loses lock, the $\overline{\text{LOCK}}$ pin output will go high and the outputs (including RCLK) will enter TRI-STATE.

The user's system monitors the $\overline{\text{LOCK}}$ pin to detect a loss of synchronization. Upon detection, the system can arrange to pulse the Serializer SYNC1 or SYNC2 pin to resynchronize. Multiple resynchronization approaches are possible. One recommendation is to provide a feedback loop using the $\overline{\text{LOCK}}$ pin itself to control the sync request of the Serializer (SYNC1 or SYNC2). Dual SYNC pins are provided for multiple control in a multi-drop application. Sending sync patterns for resynchronization is desirable when lock times within a specific time are critical. However, the Deserializer can lock to random data, which is discussed in the next section.

Random Lock Initialization and Resynchronization

The initialization and resynchronization methods described in their respective sections are the fastest ways to establish the link between the Serializer and Deserializer. However, the DS92LV1224 can attain lock to a data stream without requiring the Serializer to send special SYNC patterns. This allows the DS92LV1224 to operate in “open-loop” applications. Equally important is the Deserializer's ability to support hot insertion into a running backplane. In the open loop or hot insertion case, we assume the data stream is essentially random. Therefore, because lock time varies due to data stream characteristics, we cannot possibly predict exact lock time. However, please see [Table 1](#) for some general random lock times under specific conditions. The primary constraint on the “random” lock time is the initial phase relation between the incoming data and the REFCLK when the Deserializer powers up. As described in the next paragraph, the data contained in the data stream can also affect lock time.

If a specific pattern is repetitive, the Deserializer could enter “false lock” - falsely recognizing the data pattern as the clocking bits. We refer to such a pattern as a repetitive multi-transition, RMT. This occurs when more than one Low-High transition takes place in a clock cycle over multiple cycles. This occurs when any bit, except DIN 9, is held at a low state and the adjacent bit is held high, creating a 0-1 transition. In the worst case, the Deserializer could become locked to the data pattern rather than the clock. Circuitry within the DS92LV1224 can detect that the possibility of “false lock” exists. The circuitry accomplishes this by detecting more than one potential position for clocking bits. Upon detection, the circuitry will prevent the LOCK output from becoming active until the potential “false lock” pattern changes. The false lock detect circuitry expects the data will eventually change, causing the Deserializer to lose lock to the data pattern and then continue searching for clock bits in the serial data stream. Graphical representations of RMT are shown in [Figure 1](#). Please note that RMT only applies to bits DIN0–DIN8.

Powerdown

When no data transfer occurs, you can use the Powerdown state. The Serializer and Deserializer use the Powerdown state, a low power sleep mode, to reduce power consumption. The Deserializer enters Powerdown when you drive $\overline{\text{PWRDN}}$ and $\overline{\text{REN}}$ low. The Serializer enters Powerdown when you drive $\overline{\text{PWRDN}}$ low. In Powerdown, the PLL stops and the outputs enter TRI-STATE, which disables load current and reduces supply current to the milliampere range. To exit Powerdown, you must drive the $\overline{\text{PWRDN}}$ pin high.

Before valid data exchanges between the Serializer and Deserializer, you must reinitialize and resynchronize the devices to each other. Initialization of the Serializer takes 510 TCLK cycles. The Deserializer will initialize and assert LOCK high until lock to the Bus LVDS clock occurs.

TRI-STATE

The Serializer enters TRI-STATE when the DEN pin is driven low. This puts both driver output pins (DO+ and DO-) into TRI-STATE. When you drive DEN high, the Serializer returns to the previous state, as long as all other control pins remain static ($\overline{\text{SYNC1}}$, $\overline{\text{SYNC2}}$, $\overline{\text{PWRDN}}$, $\overline{\text{TCLK_R/F}}$).

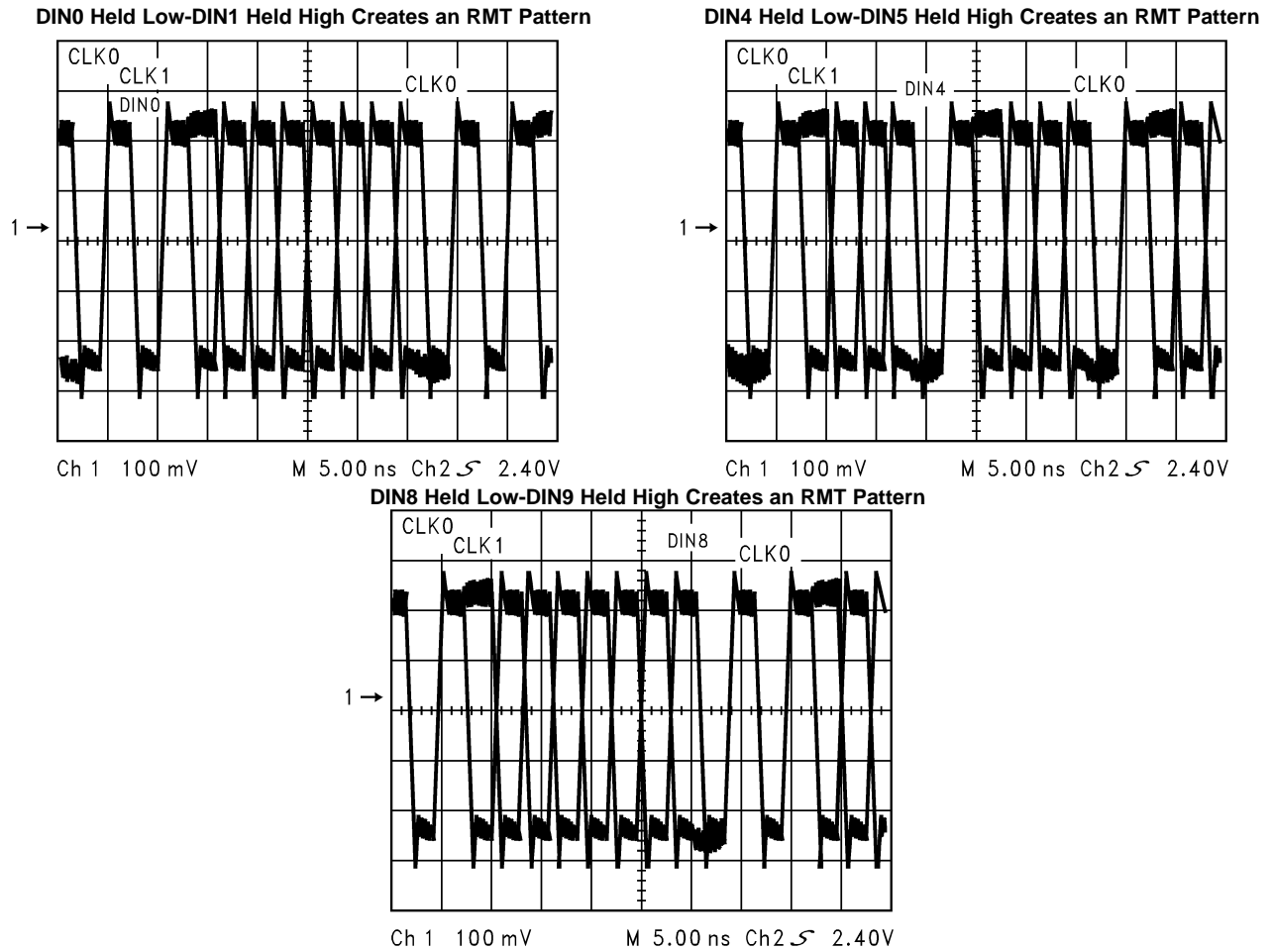
When you drive the $\overline{\text{REN}}$ pin low, the Deserializer enters TRI-STATE. Consequently, the receiver output pins (ROUT0–ROUT9) and RCLK will enter TRI-STATE. The LOCK output remains active, reflecting the state of the PLL.

Table 1. (1)

| Random Lock Times for the DS92LV1224 | | | |
|--------------------------------------|---|--------|---------------|
| | 40 MHz | 66 MHz | Units |
| Maximum | 26 | 18 | μs |
| Mean | 4.5 | 3.0 | μs |
| Minimum | 0.77 | 0.43 | μs |
| Conditions: | PRBS 2^{15} , $V_{\text{CC}} = 3.3\text{V}$ | | |

(1) Difference in lock times are due to different starting points in the data pattern with multiple parts.

Figure 1. RMT Patterns Seen on the Bus LVDS Serial Output





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

| | | |
|--|-----------------------------|------------------------------|
| Supply Voltage (V_{CC}) | | -0.3V to +4V |
| LVCMOS/LVTTL Input Voltage | | -0.3V to ($V_{CC} + 0.3V$) |
| LVCMOS/LVTTL Output Voltage | | -0.3V to ($V_{CC} + 0.3V$) |
| Bus LVDS Receiver Input Voltage | | -0.3V to +3.9V |
| Junction Temperature | | +150°C |
| Storage Temperature | | -65°C to +150°C |
| Lead Temperature (Soldering, 4 seconds) | | +260°C |
| Maximum Package Power Dissipation Capacity at 25°C Package: 28-Lead SSOP | | 1.27 W |
| Package Derating: | | 10.3 mW/°C above |
| 28-Lead SSOP | | +25°C |
| θ_{ja} | | 97°C/W |
| θ_{jc} | | 27°C/W |
| ESD Rating | HBM (1.5k Ω , 100pF) | >2kV |
| | MM | > 250V |

- (1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Recommended Operating Conditions

| | Min | Nom | Max | Units |
|--|-----|-----|-----|-----------------------|
| Supply Voltage (V_{CC}) | 3.0 | 3.3 | 3.6 | V |
| Operating Free Air Temperature (T_A) | -40 | +25 | +85 | °C |
| Receiver Input Range | 0 | | 2.4 | V |
| Supply Noise Voltage(V_{CC}) | | | | 100 mV _{P-P} |

Electrical Characteristics⁽¹⁾⁽²⁾⁽³⁾

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units | |
|--|--|--|----------------------|------------|----------|---------------|----|
| DESERIALIZER LVCMOS/LVTTL DC SPECIFICATIONS (apply to pins $\overline{\text{PWRDN}}$, $\overline{\text{RCLK_R/F}}$, $\overline{\text{REN}}$, $\overline{\text{REFCLK}}$ = inputs; apply to pins $\overline{\text{ROUT}}$, $\overline{\text{RCLK}}$, $\overline{\text{LOCK}}$ = outputs) | | | | | | | |
| V_{IH} | High Level Input Voltage | | 2.0 | | V_{CC} | V | |
| V_{IL} | Low Level Input Voltage | | GND | | 0.8 | V | |
| V_{CL} | Input Clamp Voltage | $I_{CL} = -18 \text{ mA}$ | | -0.62 | -1.5 | V | |
| I_{IN} | Input Current | $V_{IN} = 0\text{V}$ or 3.6V | -10 | ± 1 | +15 | μA | |
| V_{OH} | High Level Output Voltage | $I_{OH} = -9 \text{ mA}$ | 2.2 | 3.0 | V_{CC} | V | |
| V_{OL} | Low Level Output Voltage | $I_{OL} = 9 \text{ mA}$ | GND | 0.25 | 0.5 | V | |
| I_{OS} | Output Short Circuit Current | $V_{OUT} = 0\text{V}$ | -15 | -47 | -85 | mA | |
| I_{OZ} | TRI-STATE Output Current | $\overline{\text{PWRDN}}$ or $\overline{\text{REN}} = 0.8\text{V}$, $V_{OUT} = 0\text{V}$ or V_{CC} | -10 | ± 0.1 | +10 | μA | |
| DESERIALIZER Bus LVDS DC SPECIFICATIONS (apply to pins RI+ and RI-) | | | | | | | |
| V_{TH} | Differential Threshold High Voltage | $V_{CM} = +1.1\text{V}$ | | +6 | +50 | mV | |
| V_{TL} | Differential Threshold Low Voltage | | -50 | -12 | | mV | |
| I_{IN} | Input Current | $V_{IN} = +2.4\text{V}$, $V_{CC} = 3.6\text{V}$ or 0V | -10 | ± 1 | +15 | μA | |
| | | $V_{IN} = 0\text{V}$, $V_{CC} = 3.6\text{V}$ or 0V | -10 | ± 0.05 | +10 | μA | |
| DESERIALIZER SUPPLY CURRENT (apply to pins DVCC and AVCC) | | | | | | | |
| I_{CCR} | Deserializer Supply Current Worst Case | $C_L = 15 \text{ pF}$ See Figure 2 | $f = 30 \text{ MHz}$ | | 58 | 75 | mA |
| | | | $f = 40 \text{ MHz}$ | | 58 | 75 | mA |
| | | | $f = 66 \text{ MHz}$ | | 90 | 110 | mA |
| I_{CCXR} | Deserializer Supply Current Powerdown | $\overline{\text{PWRDN}} = 0.8\text{V}$, $\overline{\text{REN}} = 0.8\text{V}$ | | 0.36 | 1.0 | mA | |

- (1) Typical values are given for $V_{CC} = 3.3\text{V}$ and $T_A = +25^\circ\text{C}$.
- (2) Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground except V_{OD} , ΔV_{OD} , V_{TH} and V_{TL} which are differential voltages.
- (3) For the purpose of specifying deserializer PLL performance, t_{DSR1} and t_{DSR2} are specified with the $\overline{\text{REFCLK}}$ running and stable, and with specific conditions for the incoming data stream (SYNCPATs). It is recommended that the deserializer be initialized using either t_{DSR1} timing or t_{DSR2} timing. t_{DSR1} is the time required for the deserializer to indicate lock upon power-up or when leaving the power-down mode. Synchronization patterns should be sent to the device before initiating either condition. t_{DSR2} is the time required to indicate lock for the powered-up and enabled deserializer when the input (RI+ and RI-) conditions change from not receiving data to receiving synchronization patterns (SYNCPATs).

Deserializer Timing Requirements for $\overline{\text{REFCLK}}$

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|----------------------|---|------------|-------|-----|-------|-------|
| t_{RFCP} | $\overline{\text{REFCLK}}$ Period | | 15.15 | T | 33.33 | ns |
| t_{RFDC} | $\overline{\text{REFCLK}}$ Duty Cycle | | 30 | 50 | 70 | % |
| t_{RFCP} / t_{TCP} | Ratio of $\overline{\text{REFCLK}}$ to $\overline{\text{TCLK}}$ | | 95 | 1 | 105 | |
| t_{RFTT} | $\overline{\text{REFCLK}}$ Transition Time | | | 3 | 6 | ns |

Deserializer Switching Characteristics⁽¹⁾⁽²⁾

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter | Conditions | Pin/Freq. | Min | Typ | Max | Units |
|------------|---|----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|---------|
| t_{RCP} | Receiver out Clock Period | $t_{RCP} = t_{TCP}$ | RCLK | 15.15 | | 33.33 | ns |
| t_{CLH} | CMOS/TTL Low-to-High Transition Time | CL = 15 pF See Figure 3 | Rout(0-9), LOCK, RCLK | | 1.2 | 4 | ns |
| t_{CHL} | CMOS/TTL High-to-Low Transition Time | | | | 1.1 | 4 | ns |
| t_{DD} | Deserializer Delay See Figure 5 | All Temp./ All Freq. | | $1.75 \cdot t_{RCP} + 1.25$ | $1.75 \cdot t_{RCP} + 3.75$ | $1.75 \cdot t_{RCP} + 6.25$ | ns |
| | | Room Temp./ 3.3V/30MHz | | $1.75 \cdot t_{RCP} + 2.25$ | $1.75 \cdot t_{RCP} + 3.75$ | $1.75 \cdot t_{RCP} + 5.25$ | ns |
| | | Room Temp./ 3.3V/40MHz | | $1.75 \cdot t_{RCP} + 2.25$ | $1.75 \cdot t_{RCP} + 3.75$ | $1.75 \cdot t_{RCP} + 5.25$ | ns |
| | | Room Temp./ 3.3V/66MHz | | $1.75 \cdot t_{RCP} + 2.75$ | $1.75 \cdot t_{RCP} + 3.75$ | $1.75 \cdot t_{RCP} + 4.75$ | ns |
| t_{ROS} | ROUT Data Valid before RCLK | See Figure 6 | RCLK 30MHz | $0.4 \cdot t_{RCP}$ | $0.5 \cdot t_{RCP}$ | | ns |
| | | | RCLK 40MHz | $0.4 \cdot t_{RCP}$ | $0.5 \cdot t_{RCP}$ | | ns |
| | | | RCLK 66MHz | $0.38 \cdot t_{RCP}$ | $0.5 \cdot t_{RCP}$ | | ns |
| t_{ROH} | ROUT Data valid after RCLK | See Figure 6 | 30MHz | $-0.4 \cdot t_{RCP}$ | $-0.5 \cdot t_{RCP}$ | | ns |
| | | | 40MHz | $-0.4 \cdot t_{RCP}$ | $-0.5 \cdot t_{RCP}$ | | ns |
| | | | 66MHz | $-0.38 \cdot t_{RCP}$ | $-0.5 \cdot t_{RCP}$ | | ns |
| t_{RDC} | RCLK Duty Cycle | | | 45 | 50 | 55 | % |
| t_{HZR} | HIGH to TRI-STATE Delay | See Figure 7 | Rout(0-9) | | 2.8 | 10 | ns |
| t_{LZR} | LOW to TRI-STATE Delay | | | | 2.8 | 10 | ns |
| t_{ZHR} | TRI-STATE to HIGH Delay | | | | 4.2 | 10 | ns |
| t_{ZLR} | TRI-STATE to LOW Delay | | | | 4.2 | 10 | ns |
| t_{DSR1} | Deserializer PLL Lock time from PWRDWN (with SYNCPAT) | | | | 30MHz | | 1.68 |
| | | | 40MHz | | 1.31 | 3 | μ s |
| | | | 66MHz | | 0.84 | 3 | μ s |
| t_{DSR2} | Deserializer PLL Lock time from SYNCPAT | | 30MHz | | 0.62 | 1 | μ s |
| | | | 40MHz | | 0.47 | 1 | μ s |
| | | | 66MHz | | 0.29 | 0.8 | μ s |
| t_{ZHLK} | TRI-STATE to HIGH Delay (power-up) | | \overline{LOCK} | | 3.7 | 12 | ns |
| t_{RNM} | Deserializer Noise Margin | See ⁽³⁾ | 30 MHz | 650 | 950 | | ps |
| | | | 40 MHz | 450 | 730 | | ps |
| | | | 66 MHz | 250 | 400 | | ps |

(1) t_{LLHT} and t_{LHLT} specifications are Guaranteed By Design (GBD) using statistical analysis.

(2) Because the Serializer is in TRI-STATE mode, the Deserializer will lose PLL lock and have to resynchronize before data transfer.

(3) t_{RNM} is a measure of how much phase noise (jitter) the deserializer can tolerate in the incoming data stream before bit errors occur. The Deserializer Noise Margin is Guaranteed By Design (GBD) using statistical analysis.

AC Timing Diagrams and Test Circuits

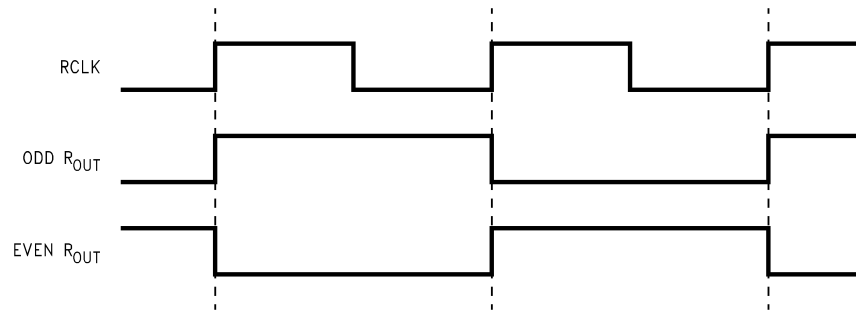


Figure 2. "Worst Case" Deserializer ICC Test Pattern

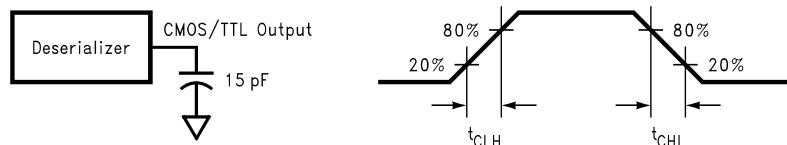


Figure 3. Deserializer CMOS/TTL Output Load and Transition Times

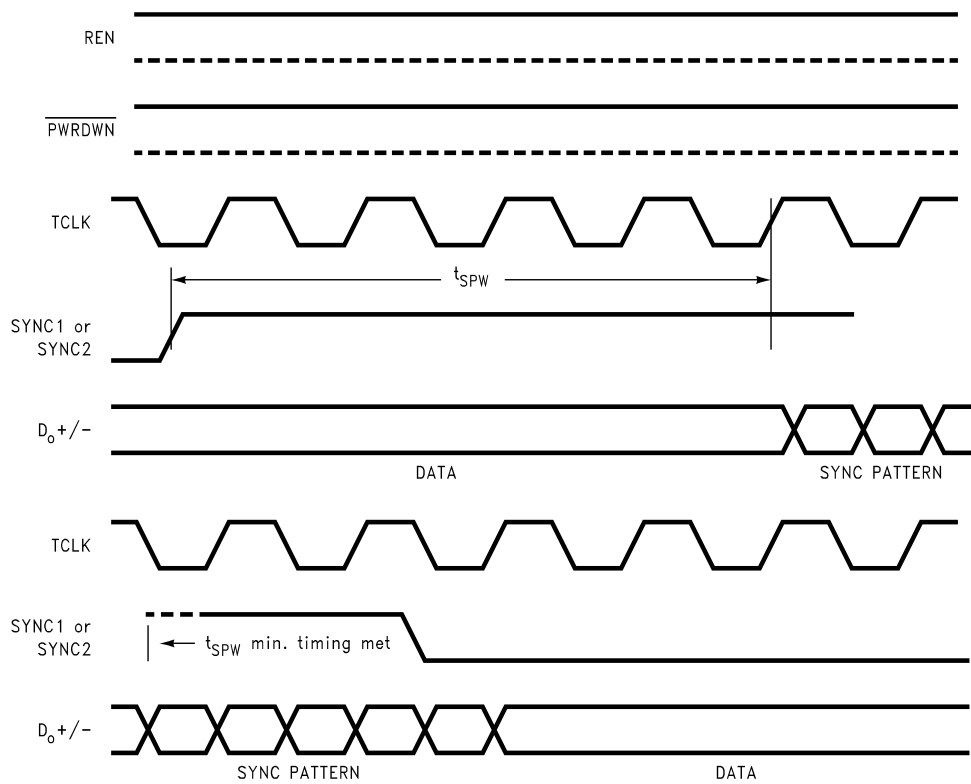


Figure 4. SYNC Timing Delays

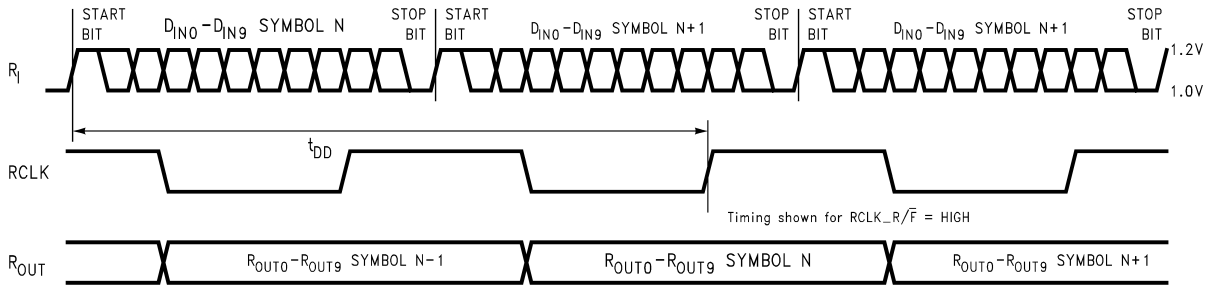
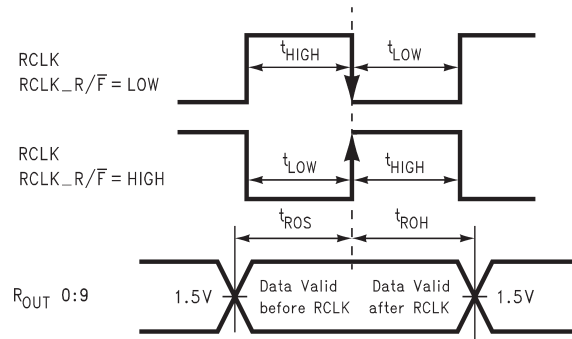


Figure 5. Deserializer Delay



Timing shown for RCLK_R/F = LOW

$$\text{Duty Cycle } (t_{RDC}) = \frac{t_{HIGH}}{t_{HIGH} + t_{LOW}}$$

Figure 6. Deserializer Data Valid Out Times

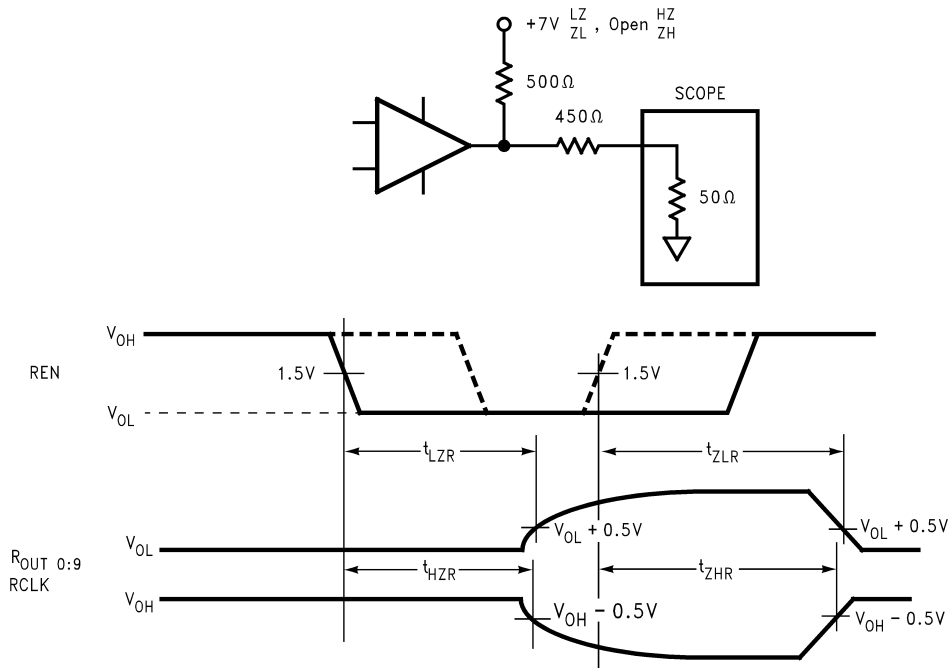


Figure 7. Deserializer TRI-STATE Test Circuit and Timing

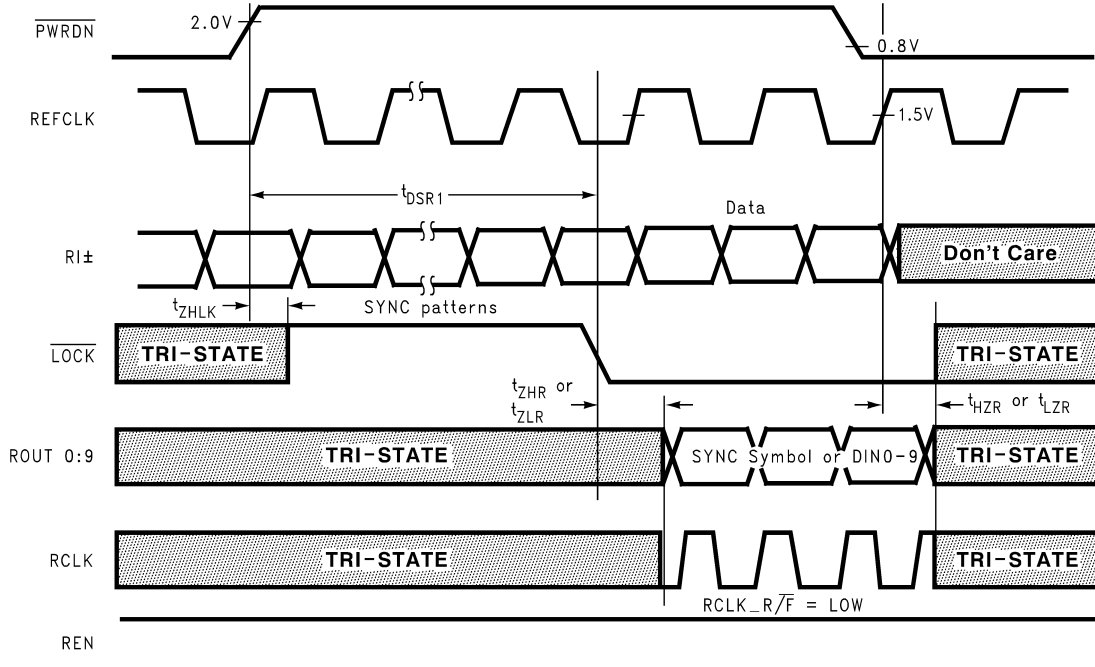


Figure 8. Deserializer PLL Lock Times and \overline{PWRDN} TRI-STATE Delays

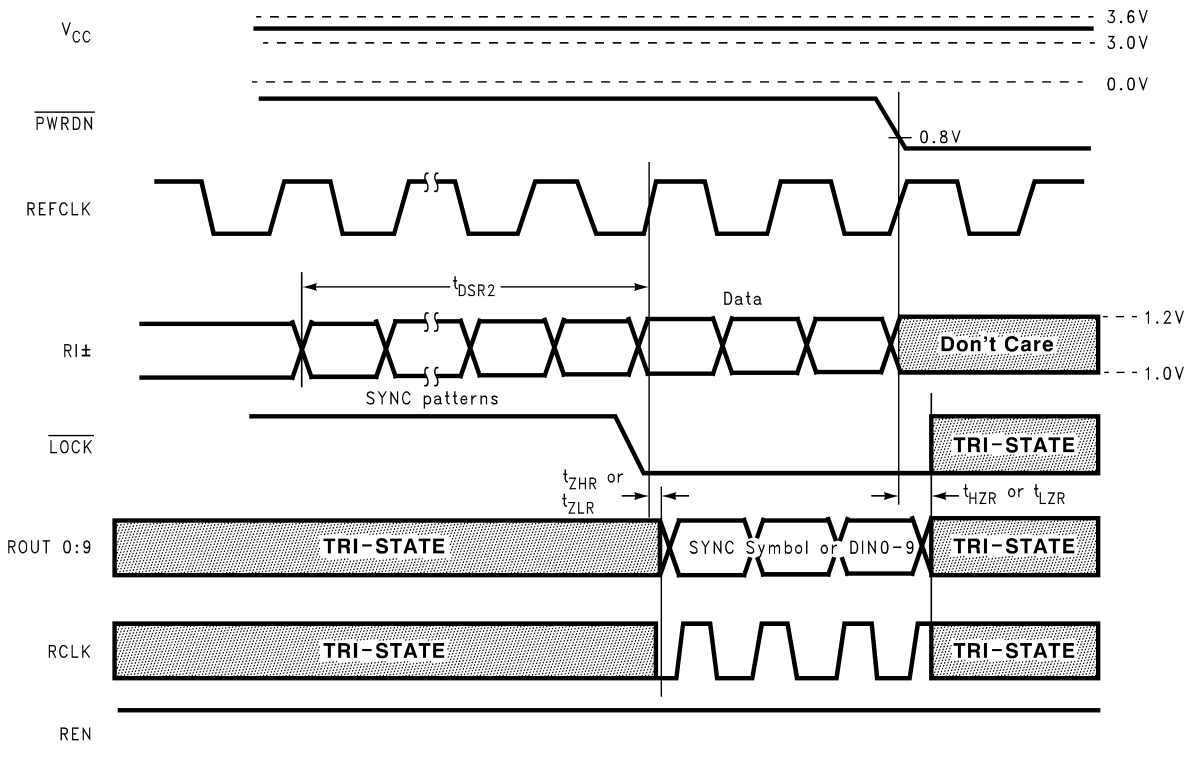
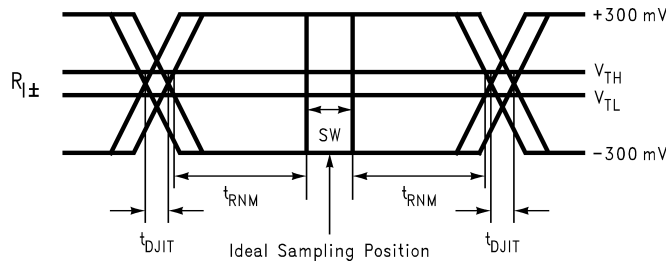


Figure 9. Deserializer PLL Lock Time from SyncPAT



SW - Setup and Hold Time (Internal Data Sampling Window)
 t_{DJIT} - Serializer Output Bit Position Jitter that results from Jitter on TCLK
 t_{RNM} = Receiver Noise Margin Time

Figure 10. Receiver Bus LVDS Input Skew Margin

Deserializer Truth Table⁽⁴⁾⁽⁵⁾⁽⁶⁾

| INPUTS | | OUTPUTS | | |
|--------------------|-----|------------|-------------------|--------|
| \overline{PWRDN} | REN | ROUT [0:9] | \overline{LOCK} | RCLK |
| H | H | Z | H | Z |
| H | H | Active | L | Active |
| L | X | Z | Z | Z |
| H | L | Z | Active | Z |

- (4) \overline{LOCK} Active indicates the \overline{LOCK} output will reflect the state of the Deserializer with regard to the selected data stream.
- (5) RCLK Active indicates the RCLK will be running if the Deserializer is locked. The Timing of RCLK with respect to ROUT is determined by RCLK_R/F
- (6) ROUT and RCLK are TRI-STATED when \overline{LOCK} is asserted High.

APPLICATION INFORMATION

USING THE SERIALIZER AND DESERIALIZER CHIPSET

The Serializer and Deserializer chipset is an easy to use transmitter and receiver pair that sends 10 bits of parallel LVTTTL data over a serial Bus LVDS link up to 660 Mbps. An on-board PLL serializes the input data and embeds two clock bits within the data stream. The Deserializer uses a separate reference clock (REFCLK) and an onboard PLL to extract the clock information from the incoming data stream and then deserialize the data. The Deserializer monitors the incoming clock information, determines lock status, and asserts the $\overline{\text{LOCK}}$ output high when loss of lock occurs.

POWER CONSIDERATIONS

An all CMOS design of the Serializer and Deserializer makes them inherently low power devices. In addition, the constant current source nature of the Bus LVDS outputs minimizes the slope of the speed vs. I_{CC} curve of conventional CMOS designs.

POWERING UP THE DESERIALIZER

The DS92LV1224 can be powered up at any time by following the proper sequence. The REFCLK input can be running before the Deserializer powers up, and it must be running in order for the Deserializer to lock to incoming data. The Deserializer outputs will remain in TRI-STATE until the Deserializer detects data transmission at its inputs and locks to the incoming data stream.

TRANSMITTING DATA

Once you power up the Serializer and Deserializer, they must be phase locked to each other to transmit data. Phase locking occurs when the Deserializer locks to incoming data or when the Serializer sends patterns. The Serializer sends SYNC patterns whenever the SYNC1 or SYNC2 inputs are high. The $\overline{\text{LOCK}}$ output of the Deserializer remains high until it has locked to the incoming data stream. Connecting the $\overline{\text{LOCK}}$ output of the Deserializer to one of the SYNC inputs of the Serializer will ensure that enough SYNC patterns are sent to achieve Deserializer lock.

The Deserializer can also lock to incoming data by simply powering up the device and allowing the “random lock” circuitry to find and lock to the data stream.

While the Deserializer $\overline{\text{LOCK}}$ output is low, data at the Deserializer outputs (ROUT0-9) is valid, except for the specific case of loss of lock during transmission which is further discussed in the “Recovering from LOCK Loss” section below.

NOISE MARGIN

The Deserializer noise margin is the amount of input jitter (phase noise) that the Deserializer can tolerate and still reliably receive data. Various environmental and systematic factors include:

Serializer: TCLK jitter, V_{CC} noise (noise bandwidth and out-of-band noise)

Media: ISI, Large V_{CM} shifts

Deserializer: V_{CC} noise

RECOVERING FROM LOCK LOSS

In the case where the Deserializer loses lock during data transmission, up to 3 cycles of data that were previously received can be invalid. This is due to the delay in the lock detection circuit. The lock detect circuit requires that invalid clock information be received 4 times in a row to indicate loss of lock. Since clock information has been lost, it is possible that data was also lost during these cycles. Therefore, after the Deserializer relocks to the incoming data stream and the Deserializer $\overline{\text{LOCK}}$ pin goes low, at least three previous data cycles should be suspect for bit errors.

The Deserializer can relock to the incoming data stream by making the Serializer resend SYNC patterns, as described above, or by random locking, which can take more time, depending on the data patterns being received.

HOT INSERTION

All the BLVDS devices are hot pluggable if you follow a few rules. When inserting, ensure the Ground pin(s) makes contact first, then the VCC pin(s), and then the I/O pins. When removing, the I/O pins should be unplugged first, then the VCC, then the Ground. Random lock hot insertion is illustrated in [Figure 13](#)

PCB CONSIDERATIONS

The Bus LVDS Serializer and Deserializer should be placed as close to the edge connector as possible. In multiple Deserializer applications, the distance from the Deserializer to the slot connector appears as a stub to the Serializer driving the backplane traces. Longer stubs lower the impedance of the bus, increase the load on the Serializer, and lower the threshold margin at the Deserializers. Deserializer devices should be placed much less than one inch from slot connectors. Because transition times are very fast on the Serializer Bus LVDS outputs, reducing stub lengths as much as possible is the best method to ensure signal integrity.

TRANSMISSION MEDIA

The Serializer and Deserializer can also be used in point-to-point configuration of a backplane, through a PCB trace, or through twisted pair cable. In point-to-point configuration, the transmission media need only be terminated at the receiver end. Please note that in point-to-point configuration, the potential of offsetting the ground levels of the Serializer vs. the Deserializer must be considered. Also, Bus LVDS provides a $\pm 1.2V$ common mode range at the receiver inputs.

Failsafe Biasing for the DS92LV1224

The DS92LV1224 has an improved input threshold sensitivity of $\pm 50mV$ versus $\pm 100mV$ for the DS92LV1210 or DS92LV1212. This allows for greater differential noise margin in the DS92LV1224. However, in cases where the receiver input is not being actively driven, the increased sensitivity of the DS92LV1224 can pickup noise as a signal and cause unintentional locking. For example, this can occur when the input cable is disconnected.

External resistors can be added to the receiver circuit board to prevent noise pick-up. Typically, the non-inverting receiver input is pulled up and the inverting receiver input is pulled down by high value resistors. The pull-up and pull-down resistors (R_1 and R_2) provide a current path through the termination resistor (R_L) which biases the receiver inputs when they are not connected to an active driver. The value of the pull-up and pull-down resistors should be chosen so that enough current is drawn to provide a $+15mV$ drop across the termination resistor. Please see [Figure 11](#) for the Failsafe Biasing Setup.

USING T_{DJIT} AND T_{RNM} TO VALIDATE SIGNAL QUALITY

The parameters t_{DJIT} and t_{RNM} can be used to generate an eye pattern mask to validate signal quality in an actual application or in simulation.

The parameter t_{DJIT} measures the transmitter's ability to place data bits in the ideal position to be sampled by the receiver. The typical t_{DJIT} parameter of -80 ps indicates that the crossing point of the Tx data is 80 ps ahead of the ideal crossing point. The $t_{DJIT(min)}$ and $t_{DJIT(max)}$ parameters specify the earliest and latest, respectively, time that a crossing will occur relative to the ideal position.

The parameter t_{RNM} is calculated by first measuring how much of the ideal bit the receiver needs to ensure correct sampling. After determining this amount, what remains of the ideal bit that is available for external sources of noise is called t_{RNM} . It is the offset from $t_{DJIT(min \text{ or } max)}$ for the test mask within the eye opening.

The vertical limits of the mask are determined by the DS92LV1224 receiver input threshold of ± 50 mV.

Please refer to the eye mask pattern of [Figure 11](#) for a graphic representation of t_{DJIT} and t_{RNM} .

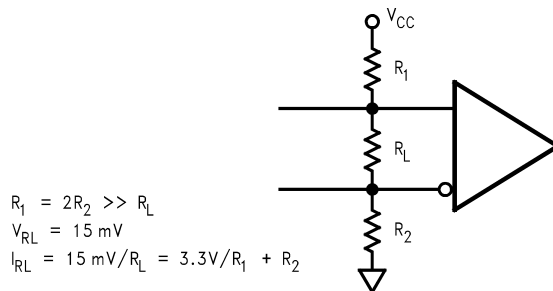


Figure 11. Failsafe Biasing Setup

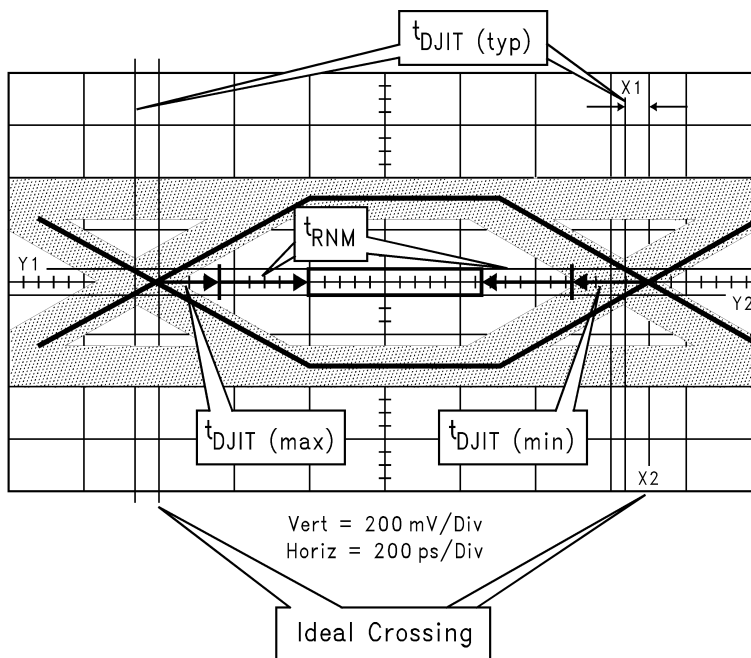


Figure 12. Using t_{DJIT} and t_{RNM} to Generate an Eye Pattern Mask and Validate Signal Quality

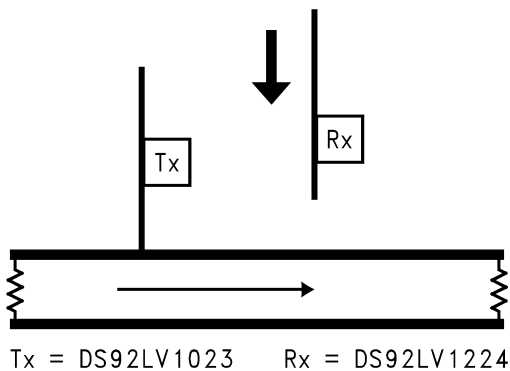


Figure 13. Random Lock Hot Insertion

Pin Diagrams

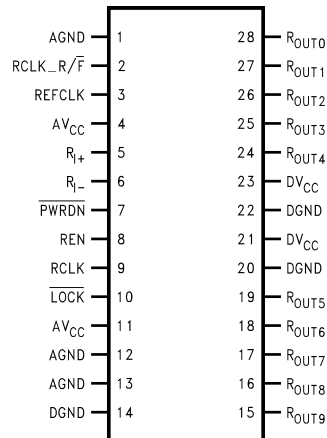


Figure 14. 28-Lead SSOP
See DB Package

DESERIALIZER PIN DESCRIPTION

| Pin Name | I/O | No. | Description |
|---------------------------|-----|--------------|---|
| ROUT | O | 15–19, 24–28 | Data Output. ± 9 mA CMOS level outputs. |
| RCLK_R/ \bar{F} | I | 2 | Recovered Clock Rising/Falling strobe select. TTL level input. Selects RCLK active edge for strobing of ROUT data. High selects rising edge. Low selects falling edge. |
| RI+ | I | 5 | + Serial Data Input. Non-inverting Bus LVDS differential input. |
| RI- | I | 6 | - Serial Data Input. Inverting Bus LVDS differential input. |
| $\overline{\text{PWRDN}}$ | I | 7 | Powerdown. TTL level input. $\overline{\text{PWRDN}}$ driven low shuts down the PLL and TRI-STATES outputs putting the device into a low power sleep mode. |
| $\overline{\text{LOCK}}$ | O | 10 | $\overline{\text{LOCK}}$ goes low when the Deserializer PLL locks onto the embedded clock edge. CMOS level output. Totem pole output structure, does not directly support wire OR connection. |
| RCLK | O | 9 | Recovered Clock. Parallel data rate clock recovered from embedded clock. Used to strobe ROUT, CMOS level output. |
| REN | I | 8 | Output Enable. TTL level input. TRI-STATES ROUT0–ROUT9, $\overline{\text{LOCK}}$ and RCLK when driven low. |
| DVCC | I | 21, 23 | Digital Circuit power supply. |
| DGND | I | 14, 20, 22 | Digital Circuit ground. |
| AVCC | I | 4, 11 | Analog power supply (PLL and Analog Circuits). |
| AGND | I | 1, 12, 13 | Analog ground (PLL and Analog Circuits). |
| REFCLK | I | 3 | Use this pin to supply a REFCLK signal for the internal PLL frequency. |

REVISION HISTORY

| Changes from Original (April 2013) to Revision A | Page |
|--|--------------------------|
| <hr/> <ul style="list-style-type: none">• Changed layout of National Data Sheet to TI format | <hr/> 16 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|----------------------|---------------|--------------|-----------------|------|-------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| DS92LV1224TMSA | ACTIVE | SSOP | DB | 28 | 47 | TBD | Call TI | Call TI | -40 to 85 | DS92LV1224T MSA | Samples |
| DS92LV1224TMSA/NOPB | ACTIVE | SSOP | DB | 28 | 47 | Green (RoHS & no Sb/Br) | SN | Level-3-260C-168 HR | -40 to 85 | DS92LV1224T MSA | Samples |
| DS92LV1224TMSAX | ACTIVE | SSOP | DB | 28 | 2000 | TBD | Call TI | Call TI | -40 to 85 | DS92LV1224T MSA | Samples |
| DS92LV1224TMSAX/NOPB | ACTIVE | SSOP | DB | 28 | 2000 | Green (RoHS & no Sb/Br) | SN | Level-3-260C-168 HR | -40 to 85 | DS92LV1224T MSA | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DS92LV1224TMSAX | SSOP | DB | 28 | 2000 | 330.0 | 16.4 | 8.4 | 10.7 | 2.4 | 12.0 | 16.0 | Q1 |
| DS92LV1224TMSAX/NOP B | SSOP | DB | 28 | 2000 | 330.0 | 16.4 | 8.4 | 10.7 | 2.4 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DS92LV1224TMSAX | SSOP | DB | 28 | 2000 | 367.0 | 367.0 | 35.0 |
| DS92LV1224TMSAX/NOP B | SSOP | DB | 28 | 2000 | 367.0 | 367.0 | 38.0 |

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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