

DS3654

DS3654 Printer Solenoid Driver



Literature Number: SNLS363A

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General Description

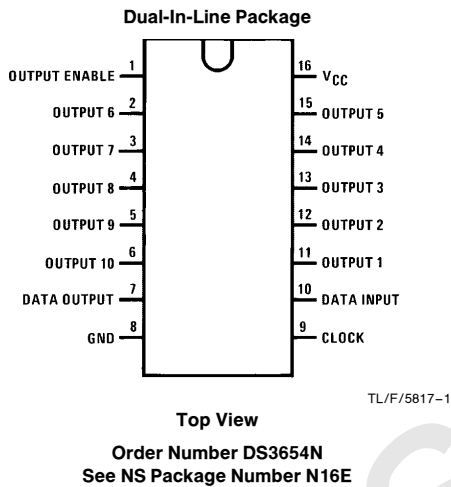
The DS3654 is a serial-to-parallel 10-bit shift register with a clock and data input, a data output from the tenth bit, and 10 open-collector clamped relay driver outputs suitable for driving printer solenoids.

Timing for the circuit is shown in *Figure 1*. Data input is sampled on the positive clock edge. Data output changes

on the negative clock edge, and is always active. Enable transfers data from the shift register to the open-collector outputs. Internal circuitry inhibits output enable for power supply voltage less than 6V.

Each output sinks 250 mA and is internally clamped to ground at 50V to dissipate energy stored in inductive loads.

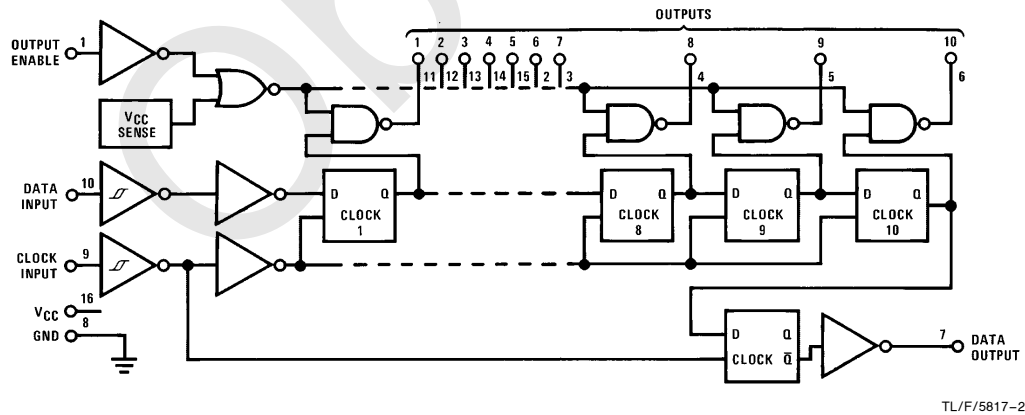
Connection Diagram



Pin Descriptions

Pin No.	Function
1	Output Enable
2	Output 6
3	Output 7
4	Output 8
5	Output 9
6	Output 10
7	Data Output
8	Ground
9	Clock Input
10	Data Input
11	Output 1
12	Output 2
13	Output 3
14	Output 4
15	Output 5
16	VCC

Logic Diagram



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	9.5V Max
Input Voltage	-0.5V Min. 9.5V Max
Output Supply, V_{p-p}	45V Max
Storage Temperature Range	-65°C to +150°C
Output Current (Single Output)	0.4A
Ground Current	4.0A
Peak Power Dissipation $t < 10$ ms, Duty Cycle $< 5\%$	4.5W Max

Maximum Power Dissipation* at 25°C

Molded Package	1687 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate molded package 13.5 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	7.5	9.5	V
Temperature (T_A)	0	+70	°C
Output Supply (V_{p-p})		40	V

Electrical Characteristics (Notes 2, 3 and 4) $V_{p-p} = 30V$ unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Units
Logical "1" Input Voltage		2.6			V
Logical "0" Input Voltage				0.8	V
Logical "1" Output Voltage Clamp	$I_{CLAMP} = 0.1A, V_{EN} = 0V$	45	50	65	V
Logical "1" Output Current	$V_{OH} = 40V, V_{EN} = 0V$			1.0	mA
Logical "0" Output Voltage	$I_{OL} = 250$ mA, $V_{EN} = 2.6V$			1.6	V
Logical "1" Input Current					
Clock	$T_A = 70^\circ C, V_{CL} = 2.6V$	0.2	0.33		mA
Enable	$T_A = 70^\circ C, V_{EN} = 2.6V$	0.2	0.33		mA
Data	$T_A = 70^\circ C, V_D = 2.6V$	0.3	0.57		mA
Clock	$T_A = 0^\circ C, V_{CL} = 2.6V$		0.33	0.5	mA
Enable	$T_A = 0^\circ C, V_{EN} = 2.6V$		0.33	0.5	mA
Data	$T_A = 0^\circ C, V_D = 2.6V$		0.57	0.75	mA
Logical "0" Input Current					
Clock	$T_A = 70^\circ C, V_{CL} = 1V$		125		μA
Enable	$T_A = 70^\circ C, V_{EN} = 1V$		125		μA
Data	$T_A = 70^\circ C, V_D = 1V$		220		μA
Input Pull-Down Resistance					
Clock	$T_A = 25^\circ C, V_{CL} < V_{CC}$		8		k Ω
Enable	$T_A = 25^\circ C, V_{EN} < V_{CC}$		8		k Ω
Data	$T_A = 25^\circ C, V_D < V_{CC}$		4.5		k Ω
Supply Current (I_{CC})					
Outputs Disabled	$T_A \geq 25^\circ C, V_{EN} = 0V, V_{DO} = 0V,$ $V_{CC} = 9.5V$		27	40	mA
Outputs Enabled	$T_A \geq 25^\circ C, V_{EN} = 2.6V, I_{OL} = 250$ mA Each Bit		55	70	mA
Data Output Low (V_{DOL})	$V_D = 0V, I_{OL} = 0V$		0.01	0.5	V
Data Output High (V_{DOH})	$V_D = 2.6V, I_{OH} = -0.75$ mA	2.6	3.4		V
Data Output Pull-Down Resistance	$V_D = 0V, V_{D0} = 1V$		14		k Ω

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 7.5V to 9.5V power supply range. All typical values given are for $V_{CC} = 8.5V$ and $T_A = 25^\circ C$.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Switching Characteristics 0°C to +70°C, $T_A = 25^\circ\text{C}$, nominal power supplies unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Units
Clk, Data and Enable Inputs t_{FC} t_{RC} t_{CLK} $t_{\overline{CLK}}$ t_{HOLD} t_{SET-UP} $t_{RE}, t_{RD IN}$ $t_{FE}, t_{FD IN}$	(Figure 1) $t_{BIT} \geq 10 \mu\text{s}$			2.0 2.0 2 3.5 1.0 1.0 1.0 5.0	μs μs μs μs μs μs μs μs
Output 1–10 t_{RO} t_{FO} t_{PDEH} t_{PDEL}	$V_{p-p} = 20\text{V}$ $R_L = 100\Omega, C_L < 100 \text{pF}$ $R_L = 100\Omega, C_L < 100 \text{pF}$		1.2 1.2 3.5 3.0		μs μs μs μs
Data Output t_{PDH}, t_{PDL} t_{RD} t_{FD}	$R_L = 5 \text{k}\Omega, C_L \leq 10 \text{pF}$		0.8 0.4 0.4	2.5	μs μs μs
Clock to Enable Delay t_{CE}		$2 t_{BIT}$			μs
Enable to Clock Delay		t_{BIT}			μs

Switching Time Waveforms

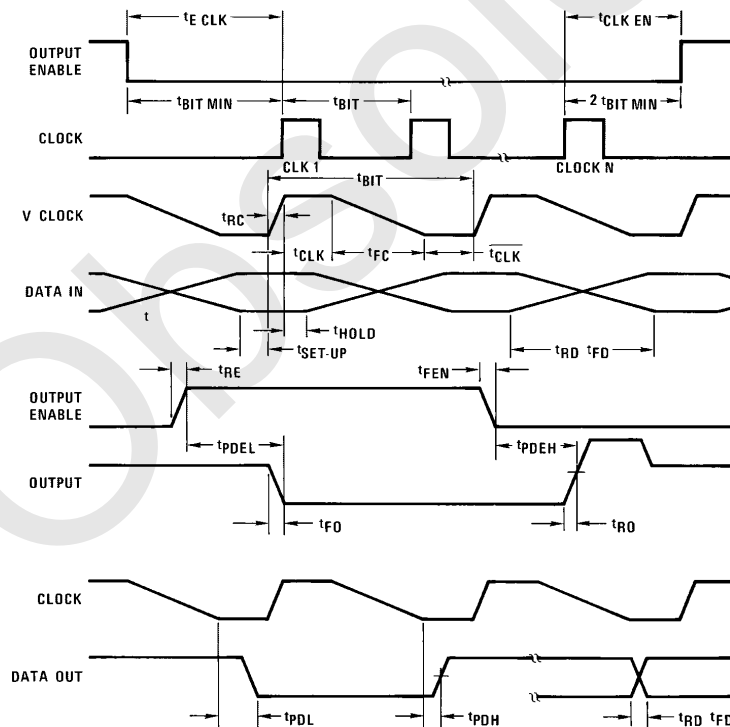


FIGURE 1. Shift Timing

TL/F/5817-3

Definition of Terms

V_{p-p}: Output power supply voltage. The return for open-collector relay driver outputs.

t_{BIT}: Period of the incoming clock.

V_{CLK}: The voltage at the clock input.

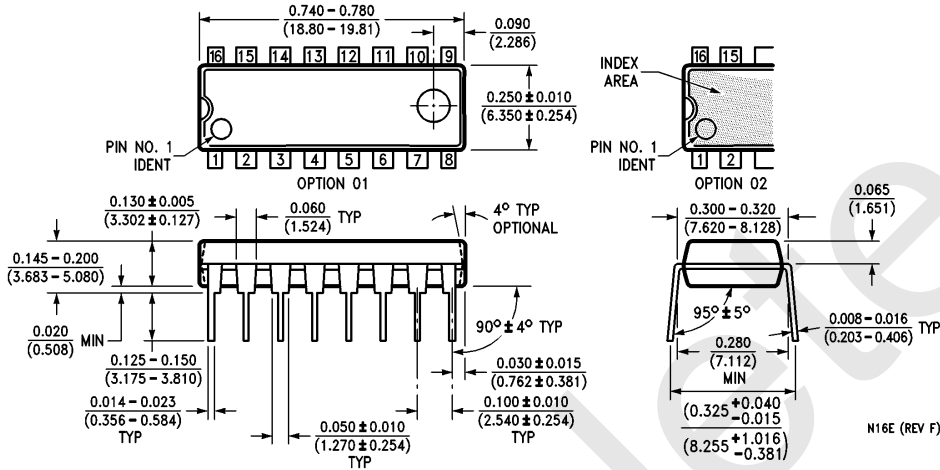
t_{CLK}: The portion of t_{BIT} when V_{CLK} ≥ 2.6V

t_{CLK}: The portion of t_{BIT} when V_{CLK} ≤ 0.8V

t_{SET-UP}: The time prior to the end of t_{CLK} required to insure valid data at the shift register input for subsequent clock transitions.

t_{HOLD}: The time following the start of t_{CLK} required to transfer data within the shift register.

Physical Dimensions inches (millimeters)



Molded Dual-In-Line Package (N)
Order Number DS3654N
NS Package Number N16E

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 1111 West Bardin Road
 Arlington, TX 76017
 Tel: (800) 272-9959
 Fax: (800) 737-7018

National Semiconductor Europe
 Fax: (+49) 0-180-530 85 86
 Email: cnjwge@tevm2.nsc.com
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National Semiconductor Hong Kong Ltd.
 19th Floor, Straight Block,
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