

## DS96173/DS96175 RS-485/RS-422 Quad Differential Line Receivers

Check for Samples: [DS96173](#), [DS96175](#)

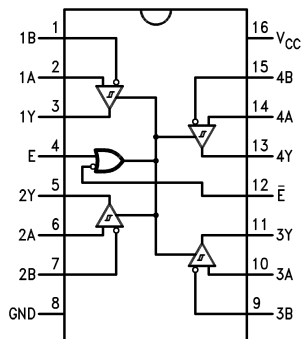
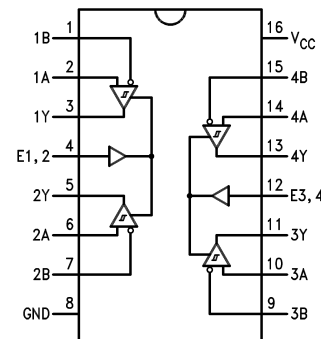
### FEATURES

- Meets EIA Standard RS-485, RS-422A, RS-423A
- Designed for Multipoint Bus Applications
- TRI-STATE Outputs
- Common Mode Input Voltage Range:  $-7V$  to  $+12V$
- Operates from Single  $+5V$  Supply
- Input Sensitivity of  $\pm 200$  mV over Common Mode Range
- Input Hysteresis of 50 mV Typical
- High Input Impedance
- DS96173/DS96175 are Lead and Function Compatible with SN75173/75175 or the AM26LS32/MC3486 Respectively

### DESCRIPTION

The DS96173 and DS96175 are high speed quad differential line receivers designed to meet EIA Standard RS-485. The devices have TRI-STATE outputs and are optimized for balanced multipoint data bus transmission at rates up to 10 Mbps. The receivers feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of 200 mV over a common mode input voltage range of  $-7V$  to  $+12V$ . The receivers are therefore suitable for multipoint applications in noisy environments. The DS96173 features an active high and active low Enable, common to all four receivers. The DS96175 features separate active high Enables for each receiver pair. Compatible RS-485 drivers, transceivers, and repeaters are also offered to provide optimum bus performance. The respective device types are DS96172, DS96174, DS96176 and DS96177.

### Pin Diagrams

**16-Lead PDIP Package - DS96173**

**16-Lead PDIP Package - DS96175**

**See Package Number NFG0016E**


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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings<sup>(1)(2)(3)</sup>

Storage Temperature Range, PDIP package	-65°C to +150°C
Lead Temperature, PDIP package (soldering, 10 sec.)	265°C
Maximum Power Dissipation <sup>(3)</sup> at 25°C	
PDIP Package	1.84W
Supply Voltage	7V
Input Voltage, A or B Inputs	±25V
Differential Input Voltage	±25V
Enable Input Voltage	7V
Low Level Output Current	50 mA

- (1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.
- (2) If Military/Aerospace specified devices are required, please contact Texas Instruments for availability and specifications.
- (3) Derate PDIP package 15 mW/°C above 25°C.

### Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage ( $V_{CC}$ )	4.75	5	5.25	V
Common Mode Input Voltage ( $V_{CM}$ )	-7		+12	V
Differential Input Voltage ( $V_{ID}$ )	-7		+12	V
Output Current High ( $I_{OH}$ )			-400	μA
Output Current LOW ( $I_{OL}$ )			16	mA
Operating Temperature ( $T_A$ )	0	25	70	°C

## Electrical Characteristics<sup>(1)(2)</sup>

over recommended temperature, common mode input voltage, and supply voltage ranges, unless otherwise specified

Parameter	Test Conditions	Min	Typ	Max	Units
$V_{TH}$	Differential Input High Threshold Voltage	$V_O = 2.7V, I_O = -0.4\text{ mA}$		0.2	V
$V_{TL}$	Differential Input <sup>(3)</sup> Low Threshold Voltage	$V_O = 0.5V, I_O = 16\text{ mA}$		-0.2	V
$V_{T+} - V_{T-}$	Hysteresis <sup>(4)</sup>	$V_{CM} = 0V$		50	mV
$V_{IH}$	Enable Input Voltage HIGH			2.0	V
$V_{IL}$	Enable Input Voltage LOW			0.8	V
$V_{IC}$	Enable Input Clamp Voltage	$I_I = -18\text{ mA}$		-1.5	V
$V_{OH}$	Output Voltage HIGH	$V_{ID} = 200\text{ mV}, I_{OH} = -400\text{ }\mu\text{A}$		2.7	V
$V_{OL}$	Output Voltage LOW	$V_{ID} = -200\text{ mV}$	$I_{OL} = 8\text{ mA}$	0.45	V
			$I_{OL} = 16\text{ mA}$	0.50	
$I_{OZ}$	High Impedance State Output	$V_O = 0.4V\text{ to }2.4V$		$\pm 20$	$\mu\text{A}$
$I_I$	Line Input Current <sup>(5)</sup>	Other Input = 0V	$V_I = 12V$	1.0	mA
			$V_I = -7V$	-0.8	
$I_{IH}$	Enable Input Current HIGH	$V_{IH} = 2.7V$		20	$\mu\text{A}$
$I_{IL}$	Enable Input Current LOW	$V_{IL} = 0.4V$		-100	$\mu\text{A}$
$R_I$	Input Resistance			12	k $\Omega$
$I_{OS}$	Short Circuit Output Current	See <sup>(6)</sup>		-15	mA
$I_{CC}$	Supply Current	Outputs Disabled		75	mA

- (1) Unless otherwise specified Min/Max limits apply across the 0°C to +70°C range for the DS96173/DS96175. All typicals are given for  $V_{CC} = 5V$  and  $T_A = 25^\circ\text{C}$ .
- (2) All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are reference to ground unless otherwise specified.
- (3) The algebraic convention, when the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.
- (4) Hysteresis is the difference between the positive-going input threshold voltage,  $V_{T+}$ , and the negative going input threshold voltage,  $V_{T-}$ .
- (5) Refer to EIA Standards RS-485 for exact conditions.
- (6) Only one output at a time should be shorted.

## Switching Characteristics

$V_{CC} = 5V, T_A = 25^\circ\text{C}$

Parameter	Test Conditions	Min	Typ	Max	Units	
$t_{PLH}$	Propagation Delay Time, Low to High Level Output	$V_{ID} = -2.5V\text{ to }2.5V, C_L = 15\text{ pF}$ , <a href="#">Figure 1</a>		15	25	ns
$t_{PHL}$	Propagation Delay Time, High to Low Level Output			15	25	ns
$t_{PZH}$	Output Enable Time to High Level	$C_L = 15\text{ pF}$ , <a href="#">Figure 2</a>		15	22	ns
$t_{PZL}$	Output Enable Time to Low Level	$C_L = 15\text{ pF}$ , <a href="#">Figure 3</a>		15	22	ns
$t_{PHZ}$	Output Disable Time from High Level	$C_L = 5\text{ pF}$ , <a href="#">Figure 2</a>		14	30	ns
$t_{PLZ}$	Output Disable Time from Low Level	$C_L = 5\text{ pF}$ , <a href="#">Figure 3</a>		24	40	ns

**Function Tables<sup>(1)</sup>**

(Each Receiver) DS96173

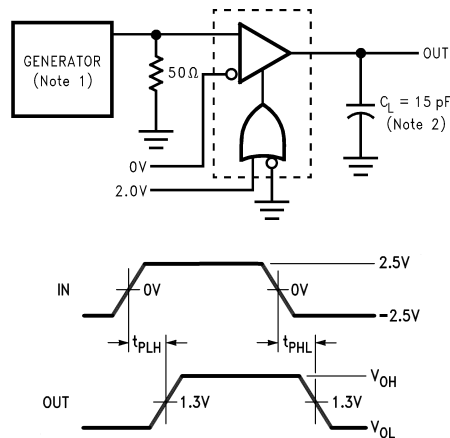
Differential Inputs	Enables		Outputs
A–B	E	$\bar{E}$	V
$V_{ID} > 0.2V$	H	X	H
	X	L	H
$V_{ID} < -0.2V$	H	X	L
	X	L	L
X	L	X	Z
X	X	H	Z

- (1) H = High Level
- L = Low Level
- X = Immaterial
- Z = High Impedance (off)

(Each Receiver) DS96175

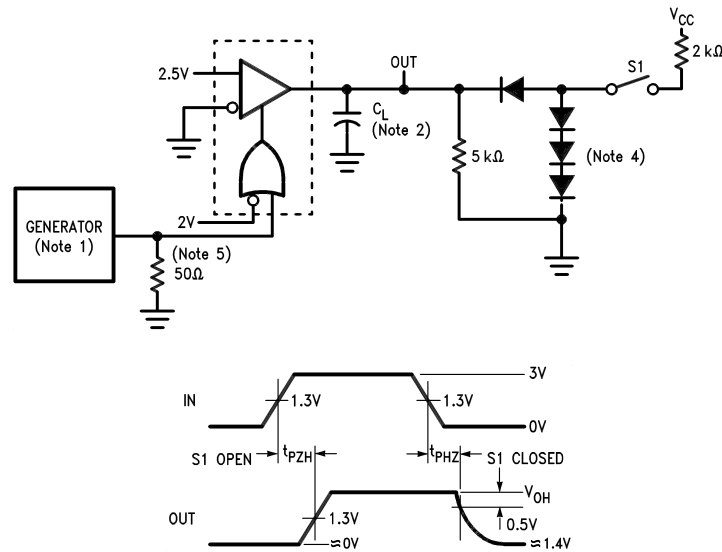
Differential Inputs	Enable	Output
A–B		Y
$V_{ID} \geq 0.2V$	H	H
$V_{ID} \leq -0.2V$	H	L
X	L	Z

**Parameter Measurement Information**



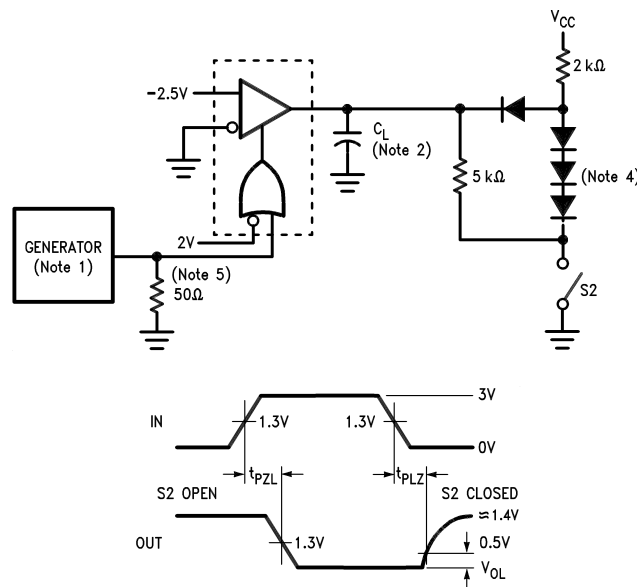
- (1) DS96173 with active high and active low Enables is shown here. DS96175 has active high Enable only.
- (2)  $C_L$  includes probe and stray capacitance.

**Figure 1.  $t_{PLH}$ ,  $t_{PHL}$**



- (1) DS96173 with active high and active low Enables is shown here. DS96175 has active high Enable only.
- (2) All diodes are 1N916 or equivalent.
- (3) To test the active low Enable  $\bar{E}$  of DS96173, ground E and apply an inverted input waveform to  $\bar{E}$ . DS96175 has active high Enable only.

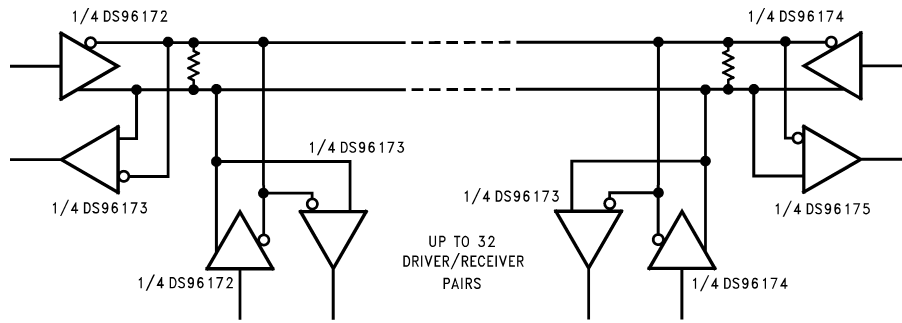
Figure 2.  $t_{PZH}$ ,  $t_{PZH}$



- (1) DS96173 with active high and active low Enables is shown here. DS96175 has active high Enable only.
- (2) All diodes are 1N916 or equivalent.
- (3) To test the active low Enable  $\bar{E}$  of DS96173, ground E and apply an inverted input waveform to  $\bar{E}$ . DS96175 has active high Enable only.

Figure 3.  $t_{PZL}$ ,  $t_{PLZ}$

**TYPICAL APPLICATION**



**NOTE**

The line length should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

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**REVISION HISTORY**

<b>Changes from Revision B (April 2013) to Revision C</b>	<b>Page</b>
• Changed layout of National Data Sheet to TI format .....	<a href="#">6</a>

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DS96175CN	ACTIVE	PDIP	NFG	16	25	TBD	Call TI	Call TI	0 to 70	DS96175CN	<a href="#">Samples</a>
DS96175CN/NOPB	ACTIVE	PDIP	NFG	16	25	Green (RoHS & no Sb/Br)	Call TI	Level-1-NA-UNLIM	0 to 70	DS96175CN	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

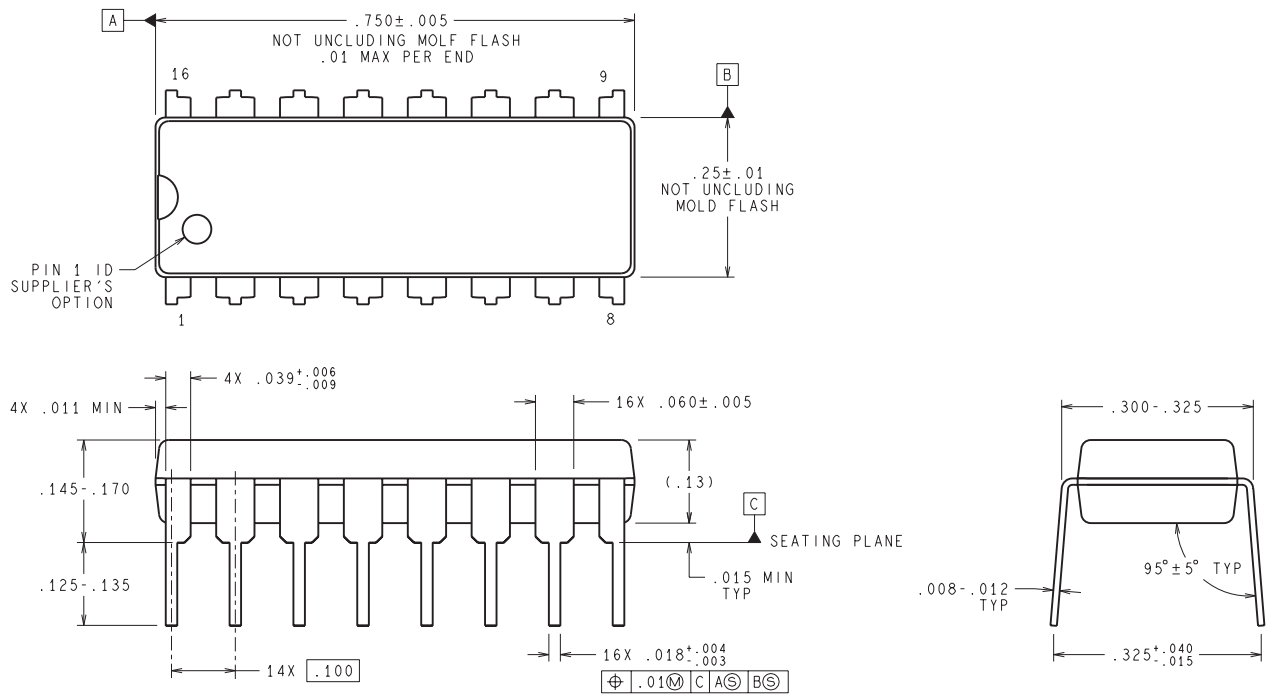
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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