

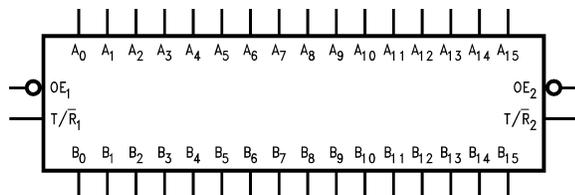
54ABT16245 16-Bit Transceiver with TRI-STATE Outputs

Check for Samples: [54ABT16245](#)

FEATURES

- Bidirectional Non-Inverting Buffers
- Separate Control Logic for Each Byte
- 16-bit Version of the 'ABT245
- A and B Output Sink Capability of 48 mA, Source Capability of 24 mA
- Ensured Latchup Protection
- High Impedance Glitch Free Bus Loading During Entire Power Up and Power Down Cycle
- Non-Destructive Hot Insertion Capability
- Standard Microcircuit Drawing (SMD) 5962-9317501

Logic Symbol



DESCRIPTION

The 'ABT16245 contains sixteen non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus oriented applications. The device is byte controlled. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The T/R inputs determine the direction of data flow through the device. The \overline{OE} inputs disable both the A and B ports by placing them in a high impedance state.

PIN DESCRIPTIONS

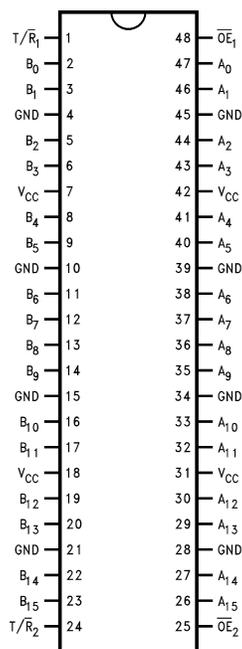
Pin Names	Description
\overline{OE}_n	Output Enable Input (Active Low)
T/\overline{R}_n	Transmit/Receive Input
A_0 – A_{15}	Side A Inputs/Outputs
B_0 – B_{15}	Side B Inputs/Outputs



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Connection Diagram



Pin Assignment for CFP
See Package Number WD

FUNCTIONAL DESCRIPTION

The 'ABT16245 contains sixteen non-inverting bidirectional buffers with TRI-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

TRUTH TABLE⁽¹⁾

Inputs		Outputs
\overline{OE}_1	T/\overline{R}_1	
L	L	Bus B ₀ –B ₇ Data to Bus A ₀ –A ₇
L	H	Bus A ₀ –A ₇ Data to Bus B ₀ –B ₇
H	X	HIGH-Z State on A ₀ –A ₇ , B ₀ –B ₇

- (1) H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Inputs		Outputs
\overline{OE}_2	T/\overline{R}_2	
L	L	Bus B ₈ –B ₁₅ Data to Bus A ₈ –A ₁₅
L	H	Bus A ₈ –A ₁₅ Data to Bus B ₈ –B ₁₅
H	X	HIGH-Z State on A ₈ –A ₁₅ , B ₈ –B ₁₅

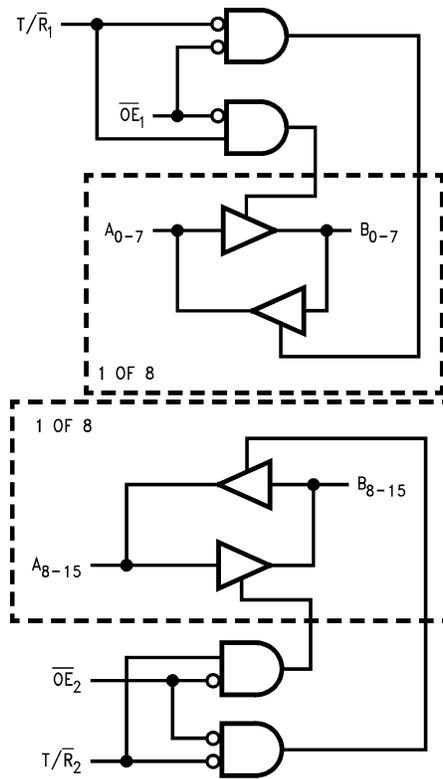


Figure 1. Logic Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾⁽²⁾

Storage Temperature		-65°C to +150°C
Ambient Temperature under Bias		-55°C to +125°C
Junction Temperature under Bias	Ceramic	-55°C to +175°C
V _{CC} Pin Potential to ground Pin		-0.5V to +7.0V
Input Voltage ⁽³⁾		-0.5V to +7.0V
Input Current ⁽³⁾		-30 mA to +5.0 mA
Voltage Applied to Any Output	in the Disabled or Power-off State	-0.5V to 5.5V
	in the HIGH State	-0.5V to V _{CC}
Current Applied to Output	in LOW State (Max)	twice the rated I _{OL} (mA)
DC Latchup Source Current		-500 mA
Over Voltage Latchup (I/O)		10V

- (1) Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) Either voltage limit or current limit is sufficient to protect inputs.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Military	-55°C to +125°C
Supply Voltage	Military	+4.5V to +5.5V
Minimum Input Edge Rate		(ΔV/Δt)
Data Input		50 mV/ns
Enable Input		20 mV/ns

DC Electrical Characteristics

Symbol	Parameter	ABT16245			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA ($\overline{OE}_n, T/\overline{R}_n$)
V _{OH}	Output HIGH Voltage	54ABT	2.5		V	Min	I _{OH} = -3 mA (A _n , B _n)
		54ABT	2.0		V	Min	I _{OH} = -24 mA (A _n , B _n)
V _{OL}	Output LOW Voltage	54ABT		0.55	V	Min	I _{OL} = 48 mA (A _n , B _n)
I _{IH}	Input HIGH Current			5	μA	Max	V _{IN} = 2.7V ($\overline{OE}_n, T/\overline{R}_n$) ⁽¹⁾
				5	μA	Max	V _{IN} = V _{CC} ($\overline{OE}_n, T/\overline{R}_n$)
I _{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V _{IN} = 7.0V ($\overline{OE}_n, T/\overline{R}_n$)
I _{BVIT}	Input HIGH Current Breakdown Test (I/O)			100	μA	Max	V _{IN} = 5.5V (A _n , B _n)
I _{IL}	Input LOW Current			-5	μA	Max	V _{IN} = 0.5V ($\overline{OE}_n, T/\overline{R}_n$) ⁽¹⁾
				-5	μA	Max	V _{IN} = 0.0V ($\overline{OE}_n, T/\overline{R}_n$)
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA ($\overline{OE}_n, T/\overline{R}_n$) All Other Pins Grounded
I _{IH} + I _{OZH}	Output Leakage Current			50	μA	0 – 5.5V	V _{OUT} = 2.7V (A _n , B _n); $\overline{OE} = 2.0V$
I _{IL} + I _{OZL}	Output Leakage Current			-50	μA	0 – 5.5V	V _{OUT} = 0.5V (A _n , B _n); $\overline{OE} = 2.0V$

(1) Ensured, but not tested.

DC Electrical Characteristics (continued)

Symbol	Parameter		ABT16245			Units	V _{CC}	Conditions
			Min	Typ	Max			
I _{OS}	Output Short-Circuit Current		-100		-275	mA	Max	V _{OUT} = 0.0V (A _n , B _n)
I _{CEX}	Output High Leakage Current				50	μA	Max	V _{OUT} = V _{CC} (A _n , B _n)
I _{ZZ}	Bus Drainage Test				100	μA	0.0	V _{OUT} = 5.50V (A _n , B _n); All Others GND
I _{CCH}	Power Supply Current				100	μA	Max	All Outputs HIGH
I _{CCL}	Power Supply Current				60	mA	Max	All Outputs LOW
I _{CCZ}	Power Supply Current				100	μA	Max	$\overline{OE}_n = V_{CC}$, T/ $\overline{R}_n =$ GND or V _{CC} All others at V _{CC} or GND
I _{CCT}	Additional I _{CC} /Input	Outputs Enabled			2.5	mA	Max	V _I = V _{CC} - 2.1V \overline{OE}_n , T/ \overline{R}_n V _I = V _{CC} - 2.1V Data Input V _I = V _{CC} - 2.1V All others at V _{CC} or GND
		Outputs TRI-STATE			2.5	mA		
		Outputs TRI-STATE			50	μA		
I _{CCD}	Dynamic I _{CC}	No Load			0.1	mA/MHz	Max	Outputs Open $\overline{OE}_n =$ GND, T/ $\overline{R}_n =$ GND or V _{CC} One Bit Toggling, 50% Duty Cycle

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	54ABT		Units	Fig. No.
		T _A = -55°C to +125°C V _{CC} = 4.5V–5.5V C _L = 50 pF			
		Min	Max		
t _{PLH}	Propagation Delay Data to Outputs	0.5	4.5	ns	See Figure 23
t _{PHL}		0.5	5.2		
t _{PZH}	Output Enable Time	0.8	6.4	ns	See Figure 22
t _{PZL}		0.9	6.9		
t _{PHZ}	Output Disable Time	1.3	6.9	ns	See Figure 22
t _{PLZ}		1.0	6.9		

CAPACITANCE

Symbol	Parameter	Typ	Units	Conditions, T _A = 25°C
C _{IN}	Input Capacitance	5	pF	V _{CC} = 0.0V (\overline{OE}_n , T/ \overline{R}_n)
C _{I/O} ⁽¹⁾	Output Capacitance	11	pF	V _{CC} = 5.0V (A _n , B _n)

(1) C_{I/O} is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

TYPICAL CHARACTERISTICS

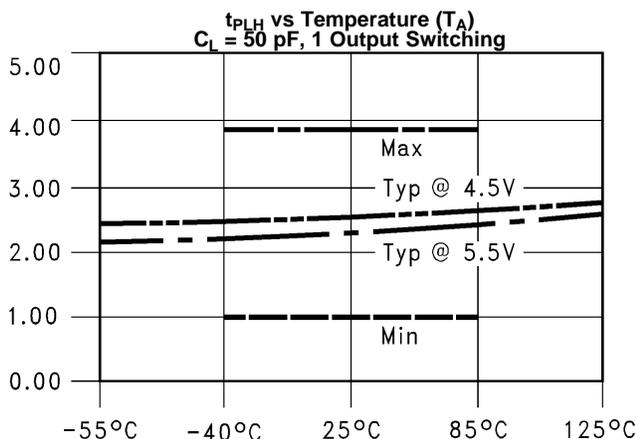


Figure 2.

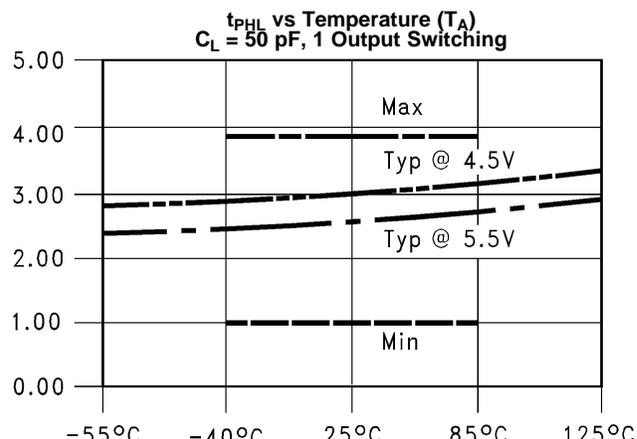


Figure 3.

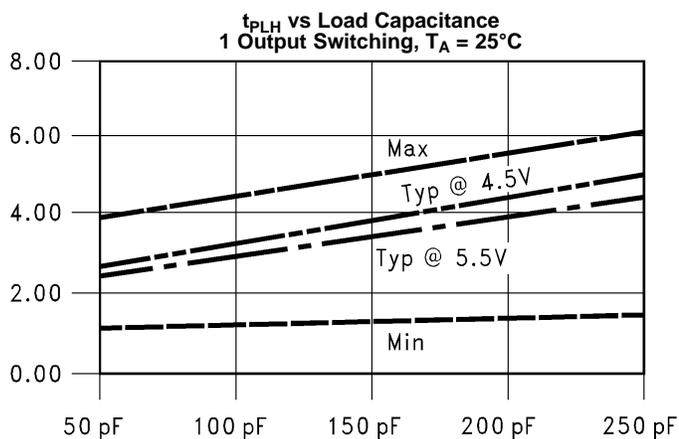


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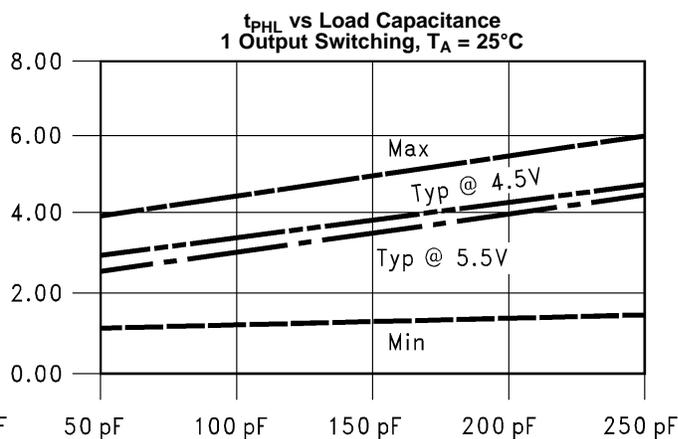


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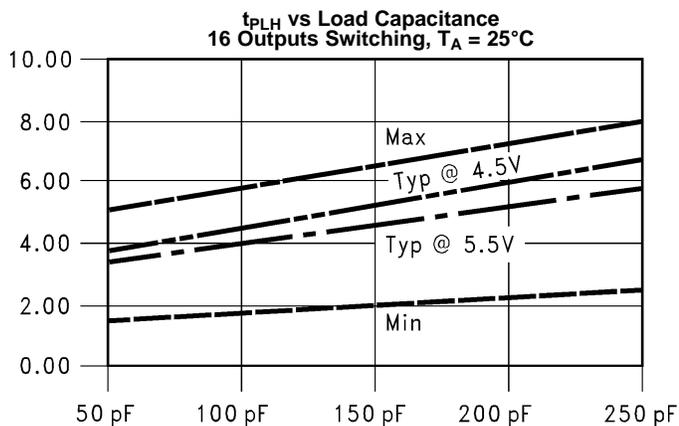


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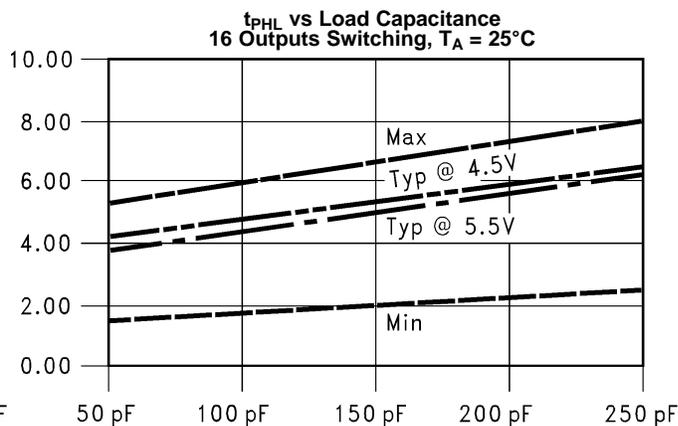
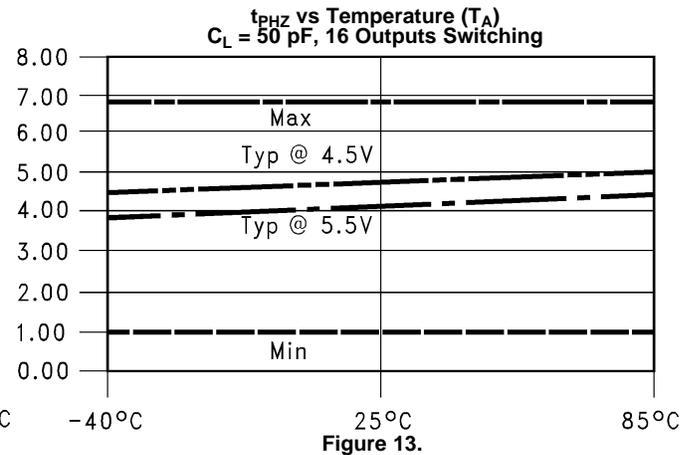
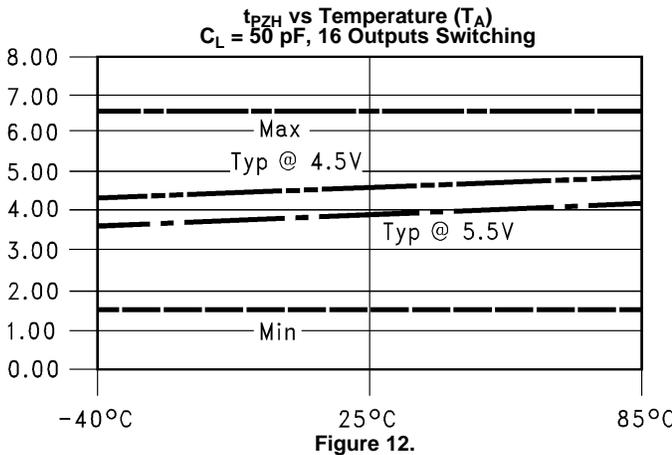
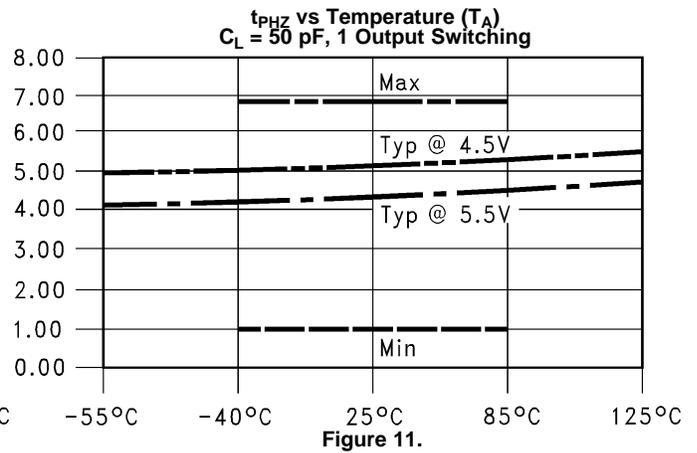
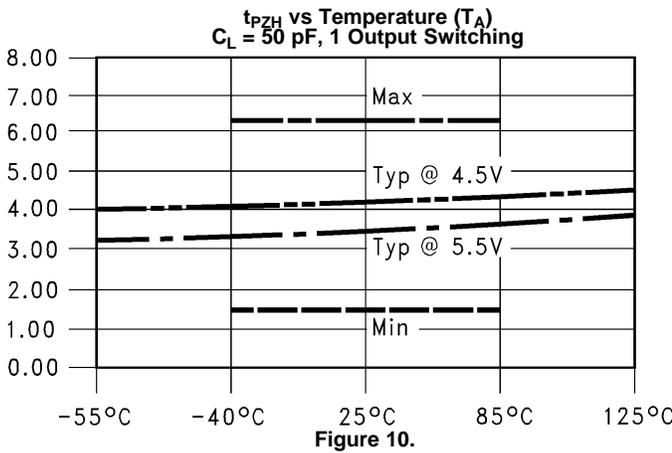
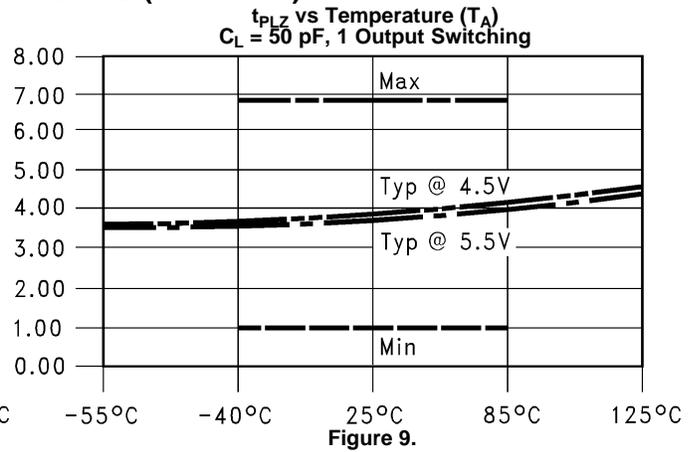
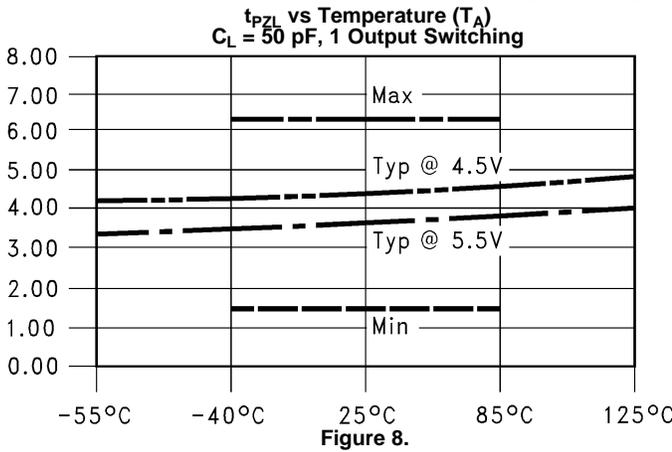


Figure 7.

TYPICAL CHARACTERISTICS (continued)



TYPICAL CHARACTERISTICS (continued)

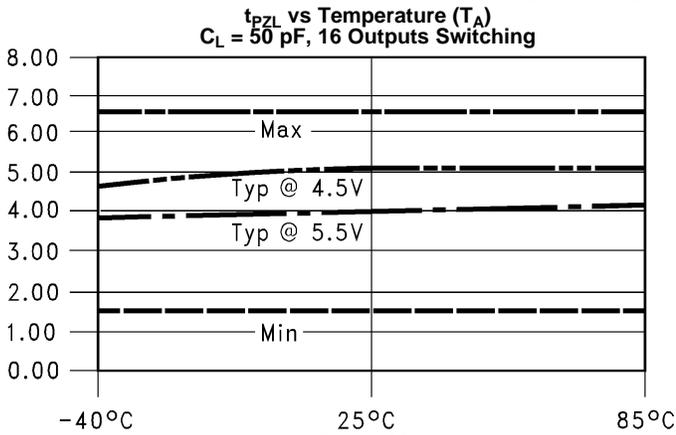


Figure 14.

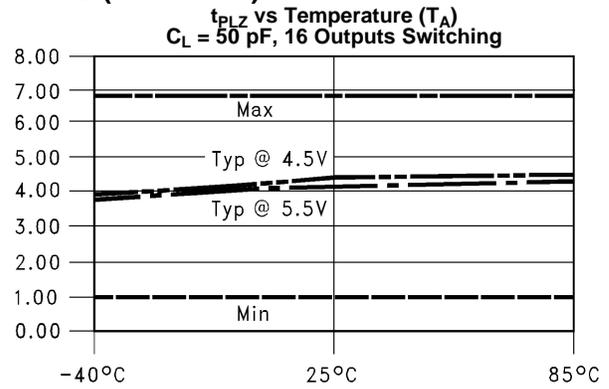


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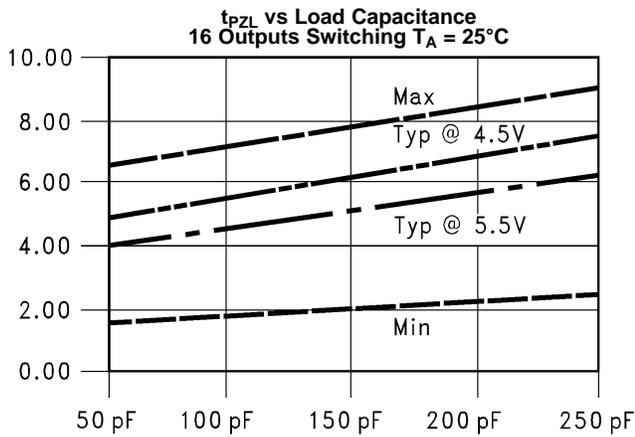


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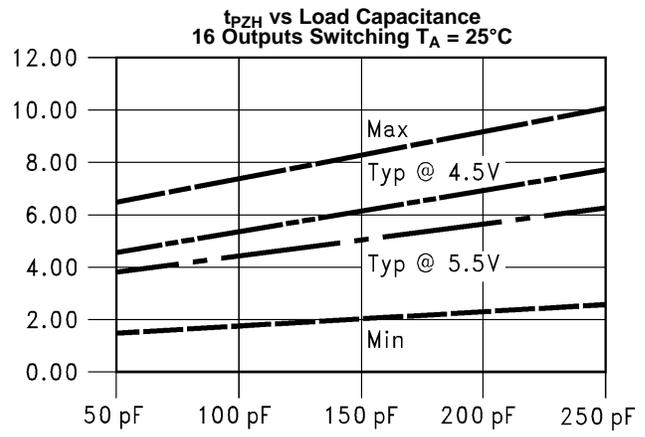


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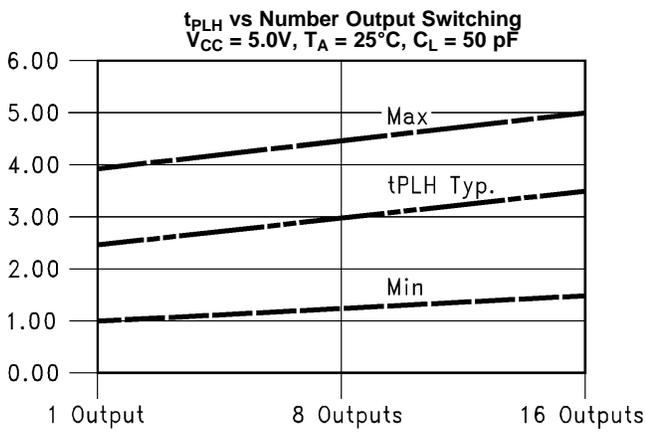


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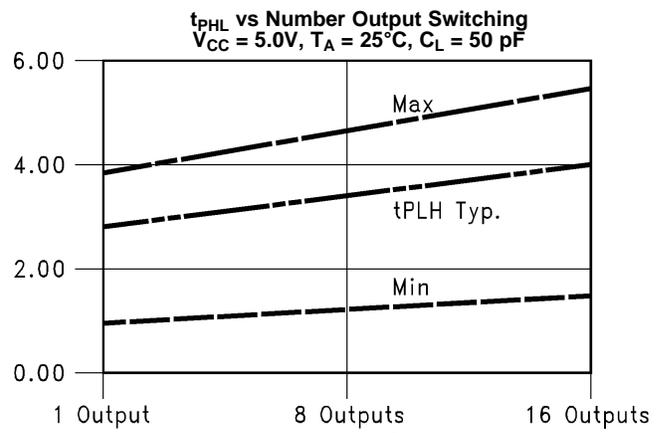
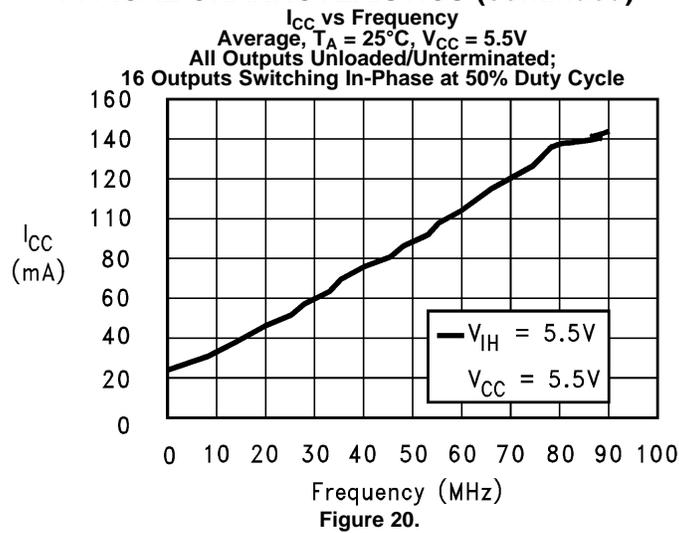
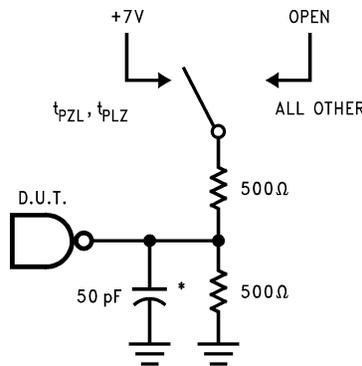


Figure 19.

TYPICAL CHARACTERISTICS (continued)



AC LOADING



*Includes jig and probe capacitance
 Standard AC Test Load

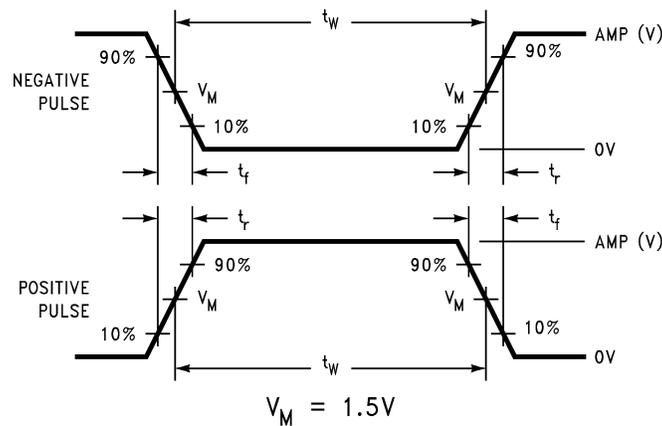
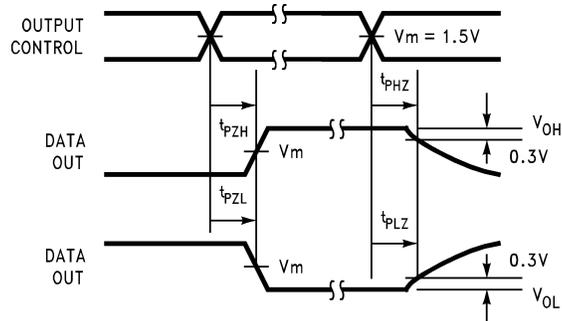
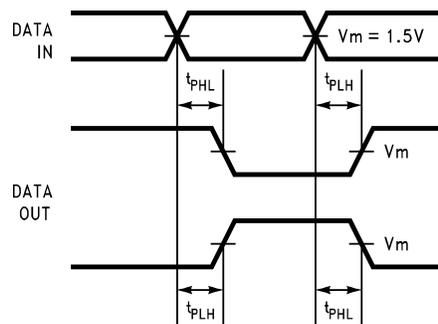


Figure 21. Input Pulse Requirements

Table 1. Test Input Signal Requirements

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

**Figure 22. TRI-STATE Output HIGH and LOW Enable and Disable Times****Figure 23. Propagation Delay Waveforms for Inverting and Non-Inverting Functions**

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	10

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