

54ABT541 Octal Buffer/Line Driver with TRI-STATE Outputs

Check for Samples: [54ABT541](#)

FEATURES

- Non-Inverting Buffers
- Output Sink Capability of 48 mA, Source Capability of 24 mA
- Ensured Latchup Protection
- High Impedance Glitch Free Bus Loading During Entire Power Up and Power Down Cycle
- Nondestructive Hot Insertion Capability
- Flow-Through Pinout for Ease of PC Board Layout
- Disable Time Less than Enable Time to Avoid Bus Contention
- Standard Microcircuit Drawing (SMD) 5962-9471801

DESCRIPTION

The 'ABT541 is an octal buffer and line driver with TRI-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver. The 'ABT541 is similar to the 'ABT244 with broadside pinout.

Connection Diagrams

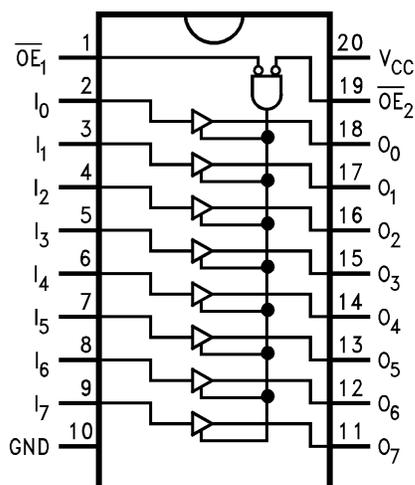


Figure 1. Pin Assignment CDIP and CLGA

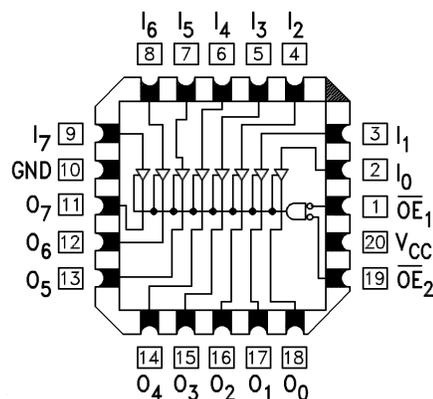


Figure 2. Pin Assignment LCCC

Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	Output Enable Input (Active Low)
I_0 – I_7	Inputs
O_0 – O_7	Outputs



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Truth Table⁽¹⁾

Inputs			Outputs
\overline{OE}_1	\overline{OE}_2	I	ABT541
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

- (1) H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾

Storage Temperature		-65°C to +150°C
Ambient Temperature under Bias		-55°C to +125°C
Junction Temperature under Bias	CDIP	-55°C to +175°C
V _{CC} Pin Potential to Ground Pin		-0.5V to +7.0V
Input Voltage ⁽²⁾		-0.5V to +7.0V
Input Current ⁽²⁾		-30 mA to +5.0 mA
Voltage Applied to Any Output	in the Disabled or Power-Off State	-0.5V to 5.5V
	in the HIGH State	-0.5V to V _{CC}
Current Applied to Output	in LOW State (Max)	twice the rated I _{OL} (mA)
DC Latchup Source Current		-500 mA
Over Voltage Latchup (I/O)		10V

- (1) Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.
 (2) Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	Military	-55°C to +125°C
Supply Voltage	Military	+4.5V to +5.5V
Minimum Input Edge Rate ($\Delta V/\Delta t$)	Data Input	50 mV/ns
	Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter	ABT541			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54ABT	2.5		V	Min	I _{OH} = -3 mA
		54ABT	2.0		V	Min	I _{OH} = -24 mA
V _{OL}	Output LOW Voltage	54ABT		0.55	V	Min	I _{OL} = 48 mA
I _{IH}	Input HIGH Current			5	μA	Max	V _{IN} = 2.7V ⁽¹⁾ V _{IN} = V _{CC}
I _{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V _{IN} = 7.0V
I _{IL}	Input LOW Current			-5	μA	Max	V _{IN} = 0.5V ⁽¹⁾
				-5			V _{IN} = 0.0V
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OZH}	Output Leakage Current			50	μA	0 - 5.5V	V _{OUT} = 2.7V; $\overline{OE}_n = 2.0V$
I _{OZL}	Output Leakage Current			-50	μA	0 - 5.5V	V _{OUT} = 0.5V; $\overline{OE}_n = 2.0V$
I _{OS}	Output Short-Circuit Current	-100	-275		mA	Max	V _{OUT} = 0.0V
I _{CEX}	Output High Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
I _{ZZ}	Bus Drainage Test			100	μA	0.0	V _{OUT} = 5.5V; All Others GND
I _{CCH}	Power Supply Current			50	μA	Max	All Outputs HIGH
I _{CCL}	Power Supply Current			30	mA	Max	All Outputs LOW
I _{CCZ}	Power Supply Current			50	μA	Max	$\overline{OE}_n = V_{CC}$; All Others at V _{CC} or Ground
I _{CCT}	Additional I _{CC} /Input	Outputs Enabled	2.5		mA	Max	V _I = V _{CC} - 2.1V Enable Input V _I = V _{CC} - 2.1V Data Input V _I = V _{CC} - 2.1V; All Others at V _{CC} or Ground
		Outputs TRI-STATE	2.5		mA		
		Outputs TRI-STATE	50		μA		
I _{CCD}	Dynamic I _{CC} ⁽¹⁾	No Load		0.1	mA/ MHz	Max	Outputs Open, $\overline{OE}_n = GND$, One Bit Toggling ⁽²⁾ , 50% Duty Cycle

(1) Specified, but not tested.

(2) For 8 bits toggling, I_{CCD} < 0.8 mA/MHz.

DC Electrical Characteristics

Symbol	Parameter	Min	Max	Units	V _{CC}	Conditions C _L = 50 pF, R _L = 500Ω
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}		1.0	V	5.0	T _A = 25°C ⁽¹⁾
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}		-1.45	V	5.0	T _A = 25°C ⁽¹⁾

(1) Max number of outputs defined as (n). n - 1 data inputs are driven 0V to 3V. One output at LOW. Specified, but not tested.

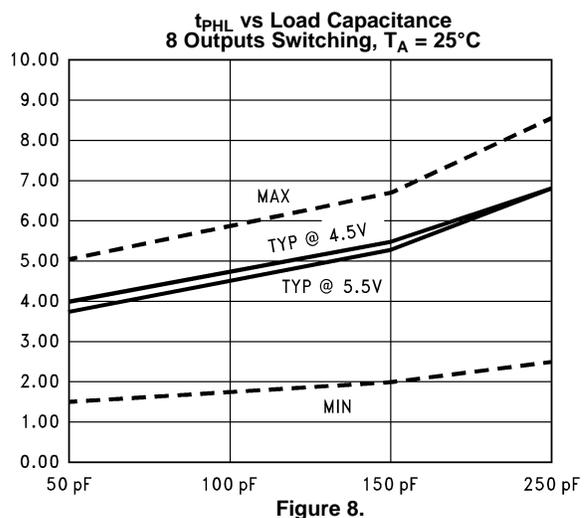
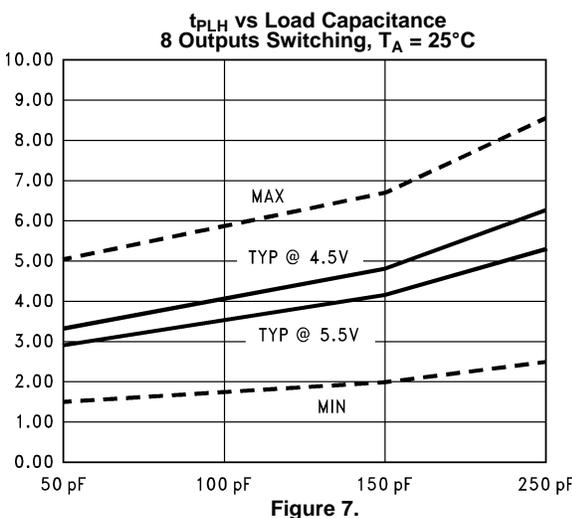
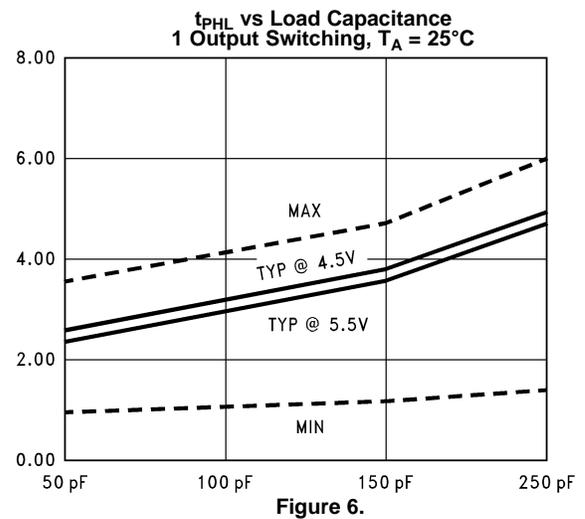
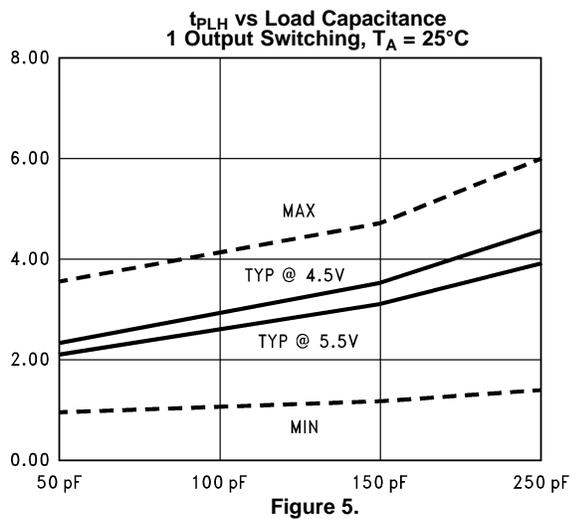
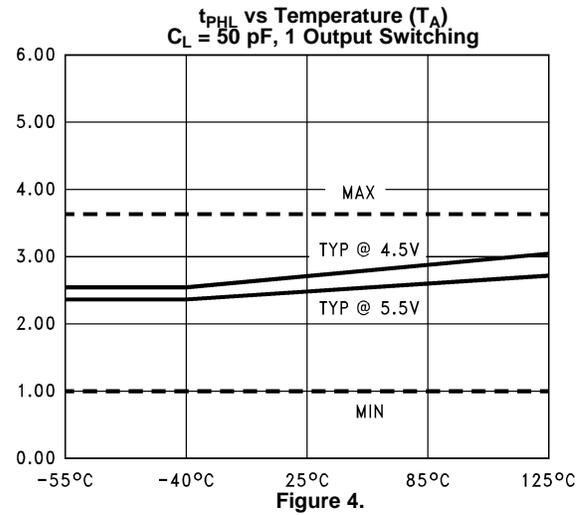
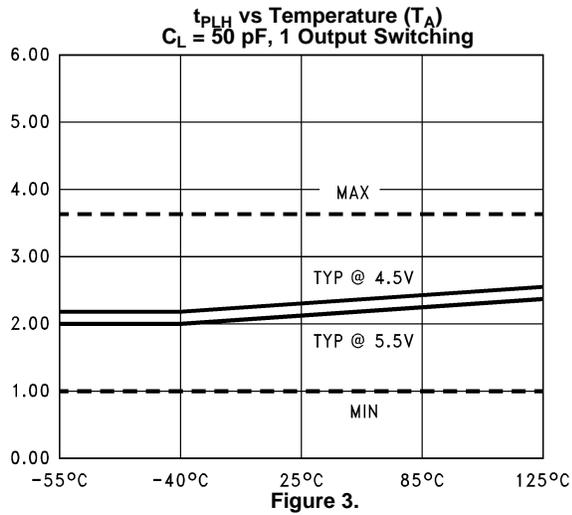
AC Electrical Characteristics

Symbol	Parameter	54ABT		Units	Fig. No.
		T _A = -55°C to +125°C V _{CC} = 4.5V–5.5V C _L = 50 pF			
		Min	Max		
t _{PLH}	Propagation Delay	1.0	5.0	ns	See Figure 23
t _{PHL}	Data to Outputs	1.0	5.3		
t _{PZH}	Output Enable Time	1.1	7.2	ns	See Figure 24
t _{PZL}		1.5	7.9		
t _{PHZ}	Output Disable Time	1.5	7.5	ns	See Figure 24
t _{PLZ}		1.5	7.9		

Capacitance

Symbol	Parameter	Typ	Units	Conditions T _A = 25°C
C _{IN}	Input Capacitance	5.0	pF	V _{CC} = 0.0V
C _{OUT} ⁽¹⁾	Output Capacitance	9.0	pF	V _{CC} = 5.0V

(1) C_{OUT} is measured at frequency of f = 1 MHz, per MIL-STD-883B, Method 3012.



Dashed lines represent design characteristics; for specifications refer to [AC Electrical Characteristics](#) Table.

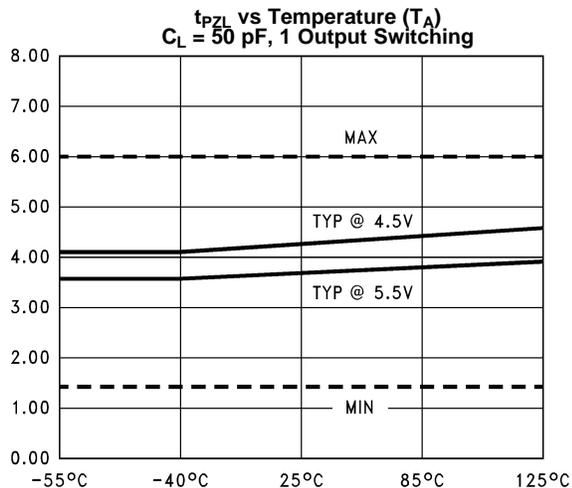


Figure 9.

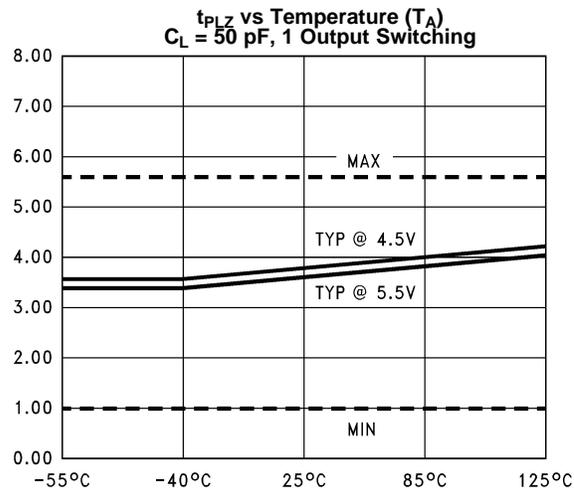


Figure 10.

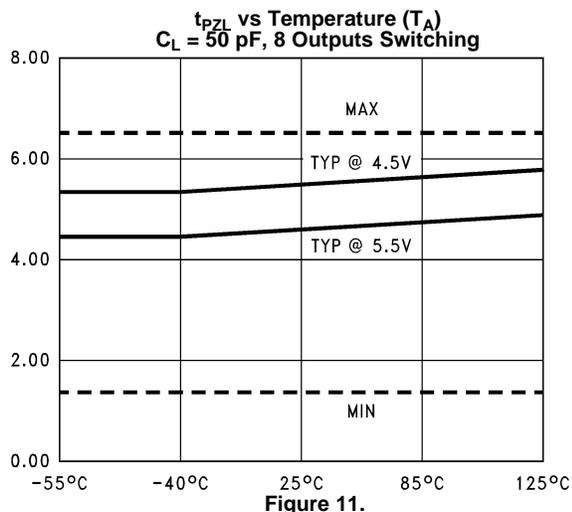


Figure 11.

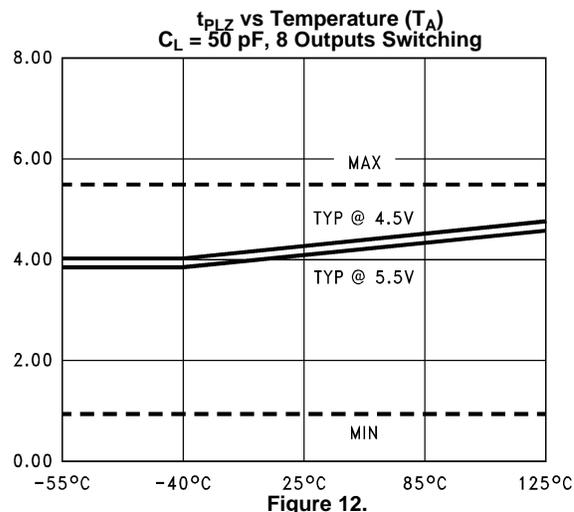


Figure 12.

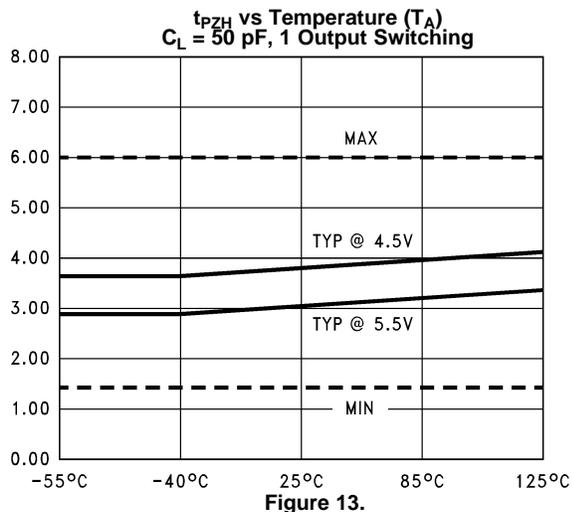


Figure 13.

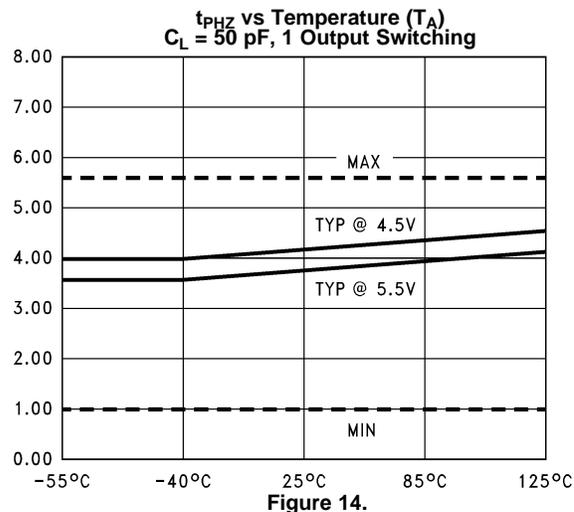


Figure 14.

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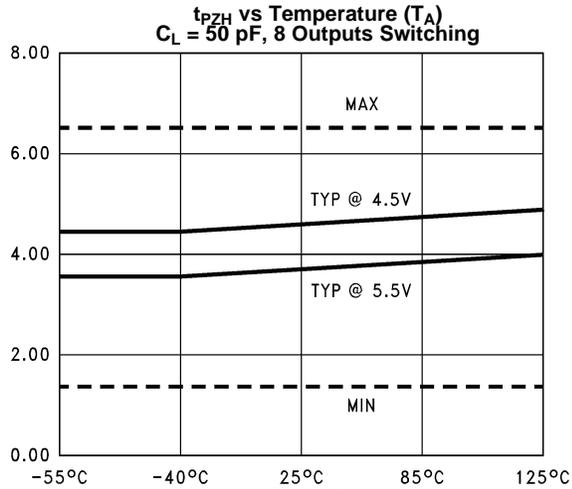


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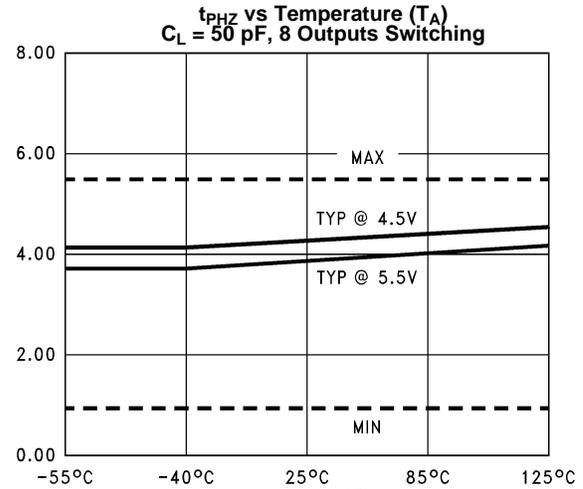


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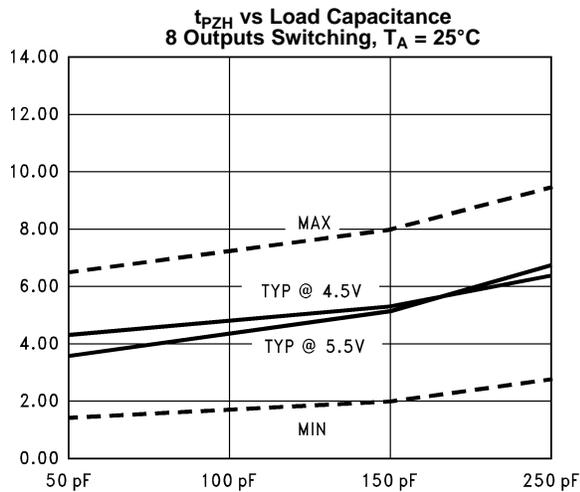


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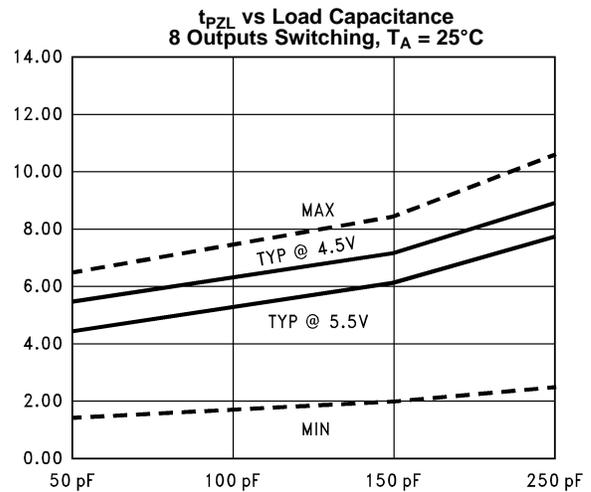


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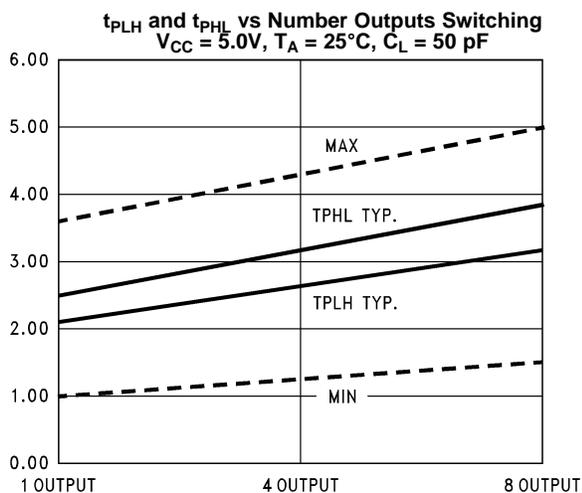


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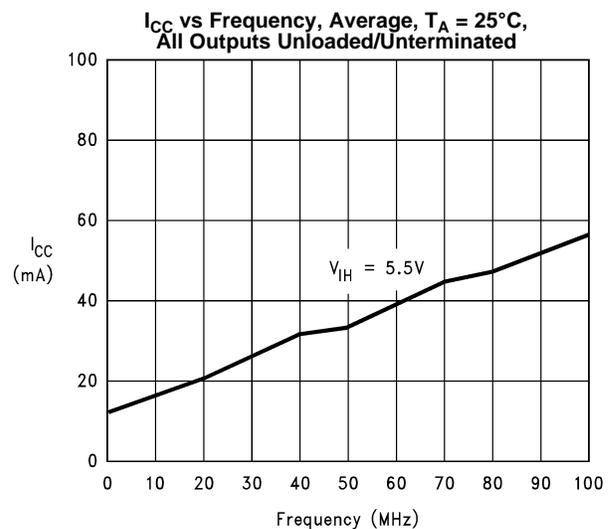
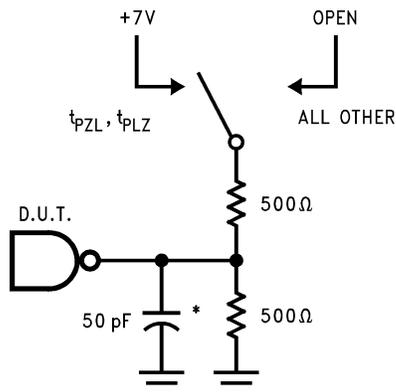


Figure 20.

Dashed lines represent design characteristics; for specifications refer to [AC Electrical Characteristics](#) Table.

AC Loading



*Includes jig and probe capacitance

Figure 21. Standard AC Test Load

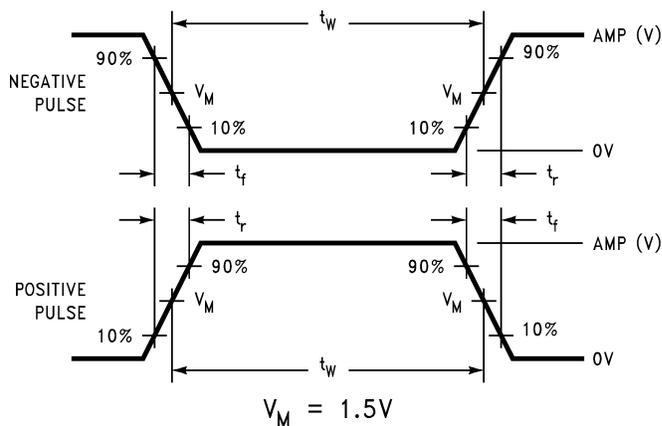


Figure 22. Test Input Signal Levels

Table 1. Test Input Signal Requirements

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

AC Waveforms

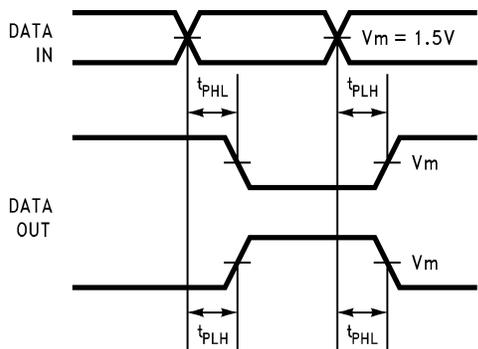


Figure 23. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

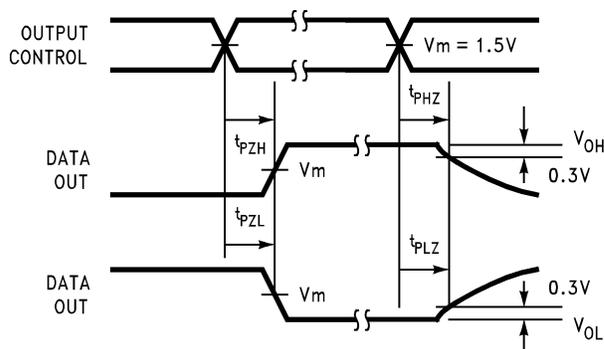


Figure 24. TRI-STATE Output HIGH and LOW Enable and Disable Time

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	8

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