54ABT543 Octal Registered Transceiver with TRI-STATE® Outputs

Check for Samples: 54ABT543

FEATURES

- **Back-to-Back Registers for Storage**
- **Bidirectional Data Path**
- **A and B Outputs have Current Sourcing Capability of 24 mA and Current Sinking Capability of 48 mA**
- **Separate Controls for Data Flow in each Direction**
- **Ensured Latchup Protection**
- **High Impedance Glitch Free Bus Loading during Entire Power Up and Power Down Cycle**
- **Nondestructive Hot Insertion Capability**
- **Standard Military Drawing (SMD) 5962-9231401**

DESCRIPTION

The 'ABT543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow.

CONNECTION DIAGRAM

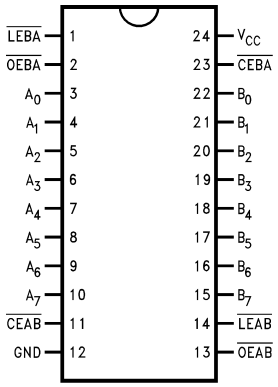


Figure 1. Pin Assignment for CDIP and CPGA
For CPGA See Package Number NAQ

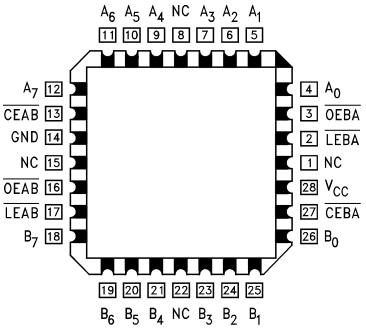


Figure 2. Pin Assignment for LCCC
See Package Number FK

PIN DESCRIPTIONS

Pin Names	Description
$\overline{OEAB}$, $\overline{OEBA}$	Output Enable Inputs
$\overline{LEAB}$, $\overline{LEBA}$	Latch Enable Inputs
$\overline{CEAB}$, $\overline{CEBA}$	Chip Enable Inputs
A_0–A_7	Side A Inputs or TRI-STATE Outputs
B_0–B_7	Side B Inputs or TRI-STATE Outputs

FUNCTIONAL DESCRIPTION

The 'ABT543 contains two sets of D-type latches, with separate input and output controls for each. For data flow from A to B, for example, the A to B Enable ($\overline{CEAB}$) input must be low in order to enter data from the A port or take data from the B port as indicated in the Data I/O Control Table. With $\overline{CEAB}$ low, a low signal on ($\overline{LEAB}$) input makes the A to B latches transparent; a subsequent low to high transition of the $\overline{LEAB}$ line puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the B output buffers are active and reflect the data present on the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$.

Table 1. DATA I/O CONTROL TABLE(1)

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$		
H	X	X	Latched	High Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	High Z
L	X	L	—	Driving

(1) H = High Voltage Level
L = Low Voltage Level
X = Immaterial

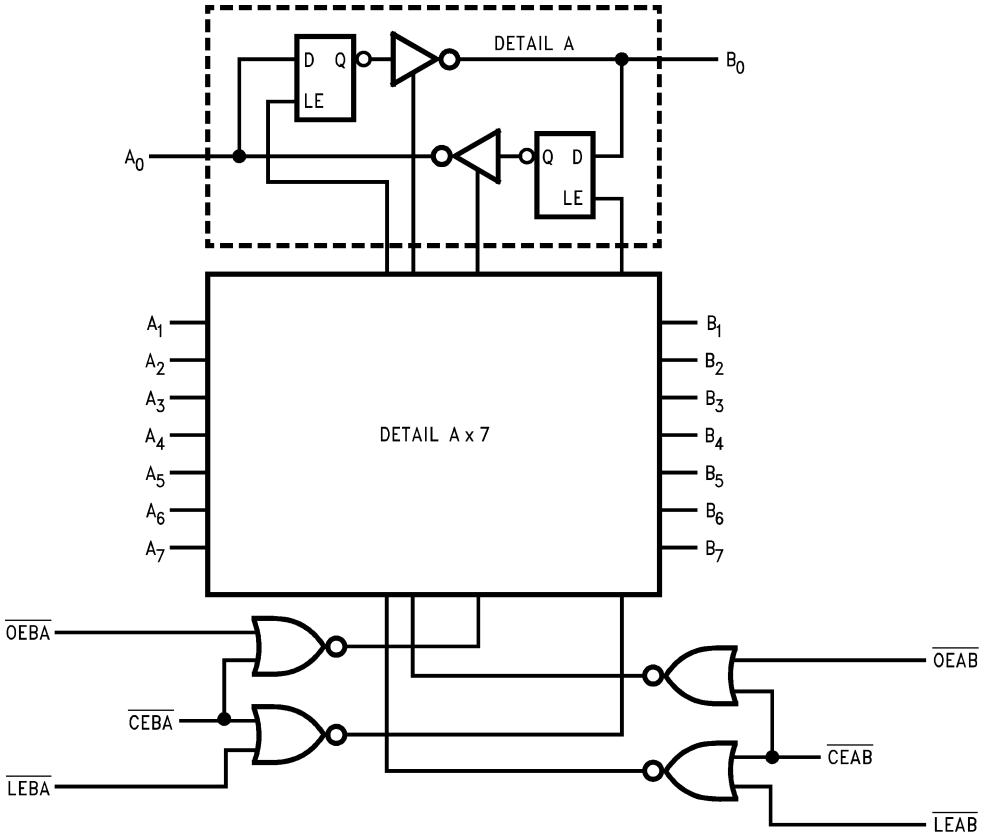


Figure 3. Logic Diagram

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)

Storage Temperature		−65°C to +150°C
Ambient Temperature under Bias		−55°C to +125°C
Junction Temperature under Bias	Ceramic	−55°C to +175°C
V_{CC} Pin Potential to Ground Pin		−0.5V to +7.0V
Input Voltage (2)		−0.5V to +7.0V
Input Current (2)		−30 mA to +5.0 mA
Voltage Applied to Any Output		
in the Disable or Power-Off State		−0.5V to +5.5V
in the HIGH State		−0.5V to V_{CC}
Current Applied to Output	in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current		−500 mA
Over Voltage Latchup (I/O)		10V

(1) Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.
(2) Either voltage limit or current limit is sufficient to protect inputs.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Military	−55°C to +125°C
Supply Voltage	Military	+4.5V to +5.5V
Minimum Input Edge Rate		(ΔV/Δt)
Data Input		50 mV/ns
Enable Input		20 mV/ns
Clock Input		100 mV/ns

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		ABT543 Min	ABT543 Typ	ABT543 Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH Voltage	54ABT	2.5					I_{OH} = −3 mA, (A_n, B_n)
		54ABT	2.0			V	Min	I_{OH} = −24 mA, (A_n, B_n)
V_{OL}	Output LOW Voltage	54ABT			0.55	V	Min	I_{OL} = 48 mA, (A_n, B_n)
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 µA, (Non-I/O Pins) All Other Pins Grounded
I_{IH}	Input HIGH Current				5	µA	Max	V_{IN} = 2.7V (Non-I/O Pins) (1) V_{IN} = V_{CC} (Non-I/O Pins)
I_{BVI}	Input HIGH Current Breakdown Test				7	µA	Max	V_{IN} = 7.0V (Non-I/O Pins)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)				100	µA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{IL}	Input LOW Current				−5	µA	Max	V_{IN} = 0.5V (Non-I/O Pins) (1) V_{IN} = 0.0V (Non-I/O Pins)
I_{IH} + I_{OZH}	Output Leakage Current				50	µA	0V–5.5 V	V_{OUT} = 2.7V (A_n, B_n); $\overline{OEAB}$ or $\overline{CEAB}$ = 2V
I_{IL} + I_{OZL}	Output Leakage Current				−50	µA	0V–5.5 V	V_{OUT} = 0.5V (A_n, B_n); $\overline{OEAB}$ or $\overline{CEAB}$ = 2V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current				50	µA	Max	V_{OUT} = V_{CC} (A_n, B_n)
I_{ZZ}	Bus Drainage Test				100	µA	0.0V	V_{OUT} = 5.5V (A_n, B_n); All Others GND
I_{CCLH}	Power Supply Current				50	µA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				50	µA	Max	Outputs TRI-STATE All Others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input				2.5	mA	Max	V_I = V_{CC} − 2.1V All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} (1)	No Load			0.18	mA/MHz	Max	Outputs Open, $\overline{CEAB}$ and $\overline{OEAB}$ = GND, $\overline{CEBA}$ = V_{CC}, One Bit Toggling, 50% Duty Cycle, (2)

(1) Ensured but not tested.
(2) For 8-bit toggling. I_{CCD} < 1.4 mA/MHz.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	V_{CC}	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		1.1	V	5.0	T_A = 25°C (1)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}		-0.45	V	5.0	T_A = 25°C (1)

(1) Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at LOW.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	54ABT T_A = −55°C to +125°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF		Units	Fig. No.
		Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	1.6 1.6	6.4 6.2	ns	See Figure 6
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEAB}$ to B_n, $\overline{LEBA}$ to A_n $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n	 1.6 1.6	 6.6 6.4	ns	See Figure 6
t_{PZH} t_{PZL}	Enable Time $\overline{LEAB}$ to B_n, $\overline{LEBA}$ to A_n $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n	 1.3 1.8	 6.4 7.4	ns	See Figure 8
t_{PHZ} t_{PLZ}	Disable Time $\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n	2.0 1.5	7.2 7.0	ns	See Figure 8

AC OPERATING REQUIREMENTS

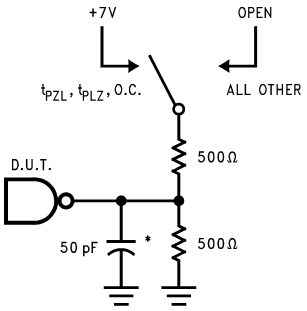
Symbol	Parameter	54ABT T_A = −55°C to +125°C, V_{CC} = 4.5V–5.5V, C_L = 50 pF		Units	Fig. No.
		Min	Max		
$t_S(H)$ $t_S(L)$	Setup Time, HIGH or LOW A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$	3.5 3.0		ns	See Figure 9
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$	2.0 2.0		ns	See Figure 9
$t_S(H)$ $t_S(L)$	Setup Time, HIGH or LOW A_n or B_n to $\overline{CEAB}$ or $\overline{CEBA}$	3.3 2.5		ns	See Figure 9
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW A_n or B_n to $\overline{CEAB}$ or $\overline{CEBA}$	2.0 2.0		ns	See Figure 9
$t_W(L)$	Pulse Width, LOW	3.5		ns	See Figure 7

CAPACITANCE

Symbol	Parameter	Typ	Units	Conditions: T_A = 25°C
C_{IN}	Input Capacitance	5.0	pF	V_{CC} = 0V (non I/O pins)
$C_{I/O}$ (1)	Output Capacitance	11.0	pF	V_{CC} = 5.0V (A_n, B_n)

(1) $C_{I/O}$ is measured at frequency, f = 1 MHz, PER MIL-STD-883, METHOD 3012.

AC LOADING



*Includes jig and probe capacitance

Figure 4. Standard AC Test Load

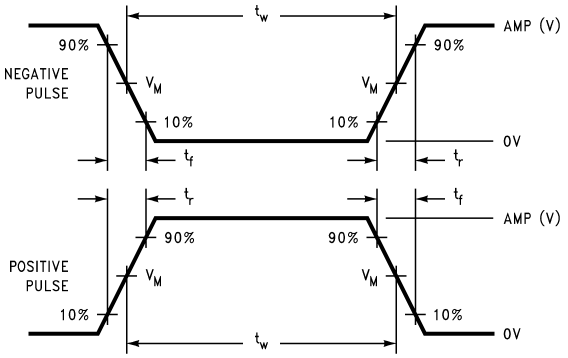


Figure 5. V_M = 1.5V Input Pulse Requirements

Table 2. Test Input Signal Requirements

Amplitude	Rep. Rate	t_w	t_r	t_f
3V	1 MHz	500 ns	2.5 ns	2.5 ns

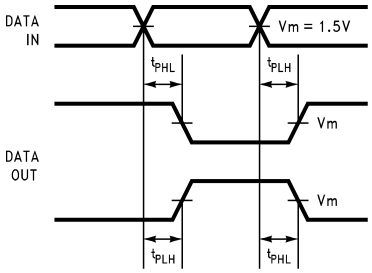


Figure 6. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

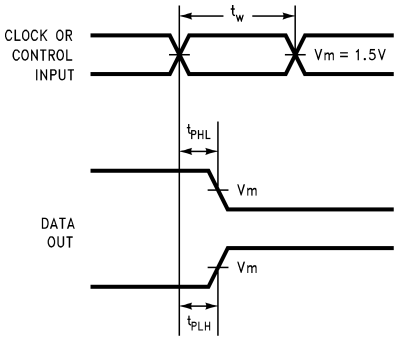


Figure 7. Propagation Delay, Pulse Width Waveforms

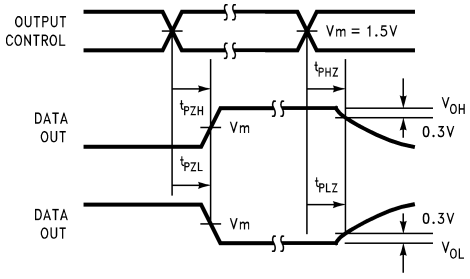


Figure 8. TRI-STATE Output HIGH and LOW Enable and Disable Times

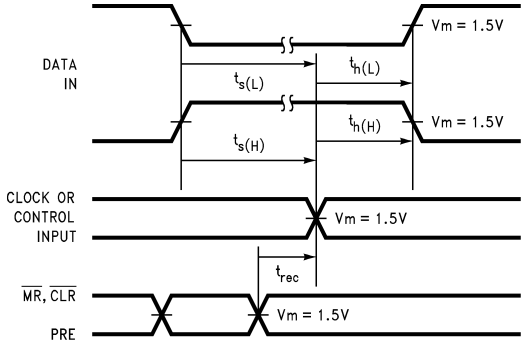


Figure 9. Setup Time, Hold Time and Recovery Time Waveforms

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	6

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