

54ACT823 9-Bit D Flip-Flop

Check for Samples: [54ACT823](#)

FEATURES

- Outputs Source/Sink 24 mA
- TRI-STATE Outputs for Bus Interfacing
- Inputs and Outputs are on Opposite Sides
- ACT823 has TTL-Compatible Inputs
- Standard Microcircuit Drawing (SMD) 5962-9161001

Logic Symbols

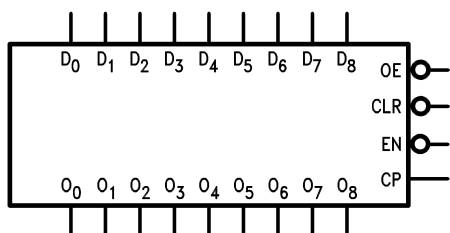


Figure 1.

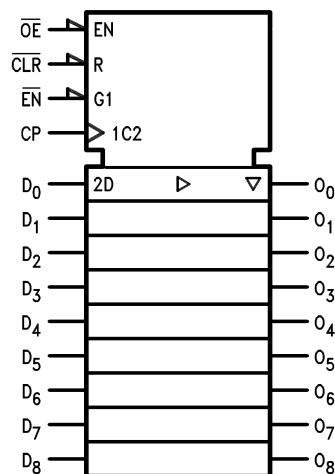


Figure 2. IEEE/IEC

Pin Names	Description
D ₀ –D ₈	Data Inputs
O ₀ –O ₈	Data Outputs
\overline{OE}	Output Enable
\overline{CLR}	Clear
CP	Clock Input
\overline{EN}	Clock Enable



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Connection Diagrams

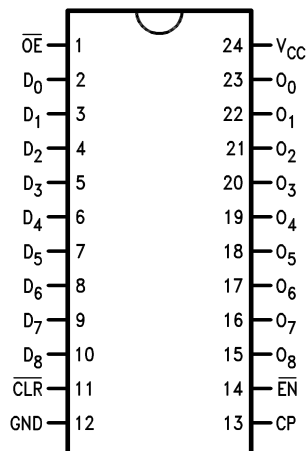


Figure 3. Pin Assignment for CDIP and CLGA

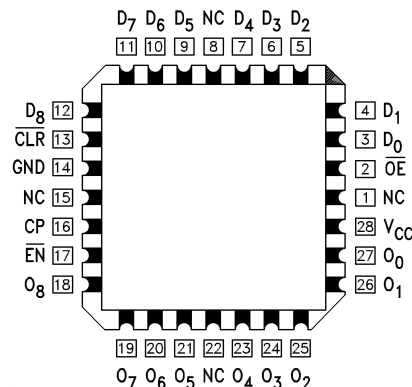


Figure 4. Pin Assignment for LCCC

FUNCTIONAL DESCRIPTION

The ACT823 consists of nine D-type edge-triggered flip-flops. These have TRI-STATE outputs for bus systems organized with inputs and outputs on opposite sides. The buffered clock (CP) and buffered Output Enable (\overline{OE}) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the \overline{LOW} -to-HIGH CP transition. With \overline{OE} LOW, the contents of the flip-flops are available at the outputs. When \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops. In addition to the Clock and Output Enable pins, there are Clear (\overline{CLR}) and Clock Enable (\overline{EN}) pins. These devices are ideal for parity bus interfacing in high performance systems.

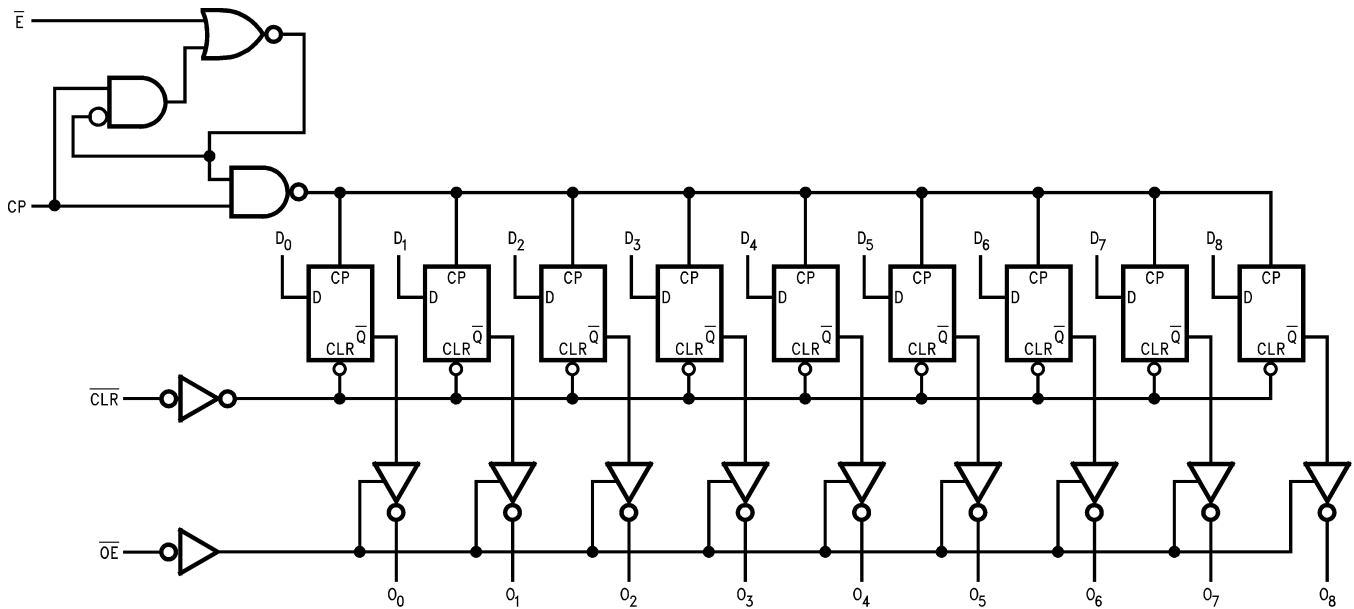
When \overline{CLR} is LOW and \overline{OE} is LOW, the outputs are LOW. When \overline{CLR} is HIGH, data can be entered into the flip-flops. When \overline{EN} is LOW, data on the inputs is transferred to the outputs on the \overline{LOW} -to-HIGH clock transition. When the \overline{EN} is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

Table 1. Function Table⁽¹⁾

Inputs					Internal	Output	Function
\overline{OE}	\overline{CLR}	\overline{EN}	CP	D	Q	O	
H	X	L	N	L	L	Z	High Z
H	X	L	N	H	H	Z	High Z
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	Clear
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	Hold
H	H	L	N	L	L	Z	Load
H	H	L	N	H	H	Z	Load
L	H	L	N	L	L	L	Load
L	H	L	N	H	H	H	Load

- (1) H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance
 N = \overline{LOW} -to-HIGH Transition
 NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

Supply Voltage (V_{CC})		-0.5V to 7.0V
DC Input Diode Current (I_{IK})	$V_I = -0.5V$	-20 mA
	$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)		-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	$V_O = -0.5V$	-20 mA
	$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)		-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)		± 50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})		± 50 mA
Storage Temperature (T_{STG})		-65°C to +150°C
Junction Temperature (T_J)	CDIP	175°C

- (1) Absolute Maximum Ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. TI does not recommend operation of FACT[®] circuits outside databook specifications.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	ACT	4.5V to 5.5V
Input Voltage (V_I)		0V to V_{CC}
Output Voltage (V_O)		0V to V_{CC}
Operating Temperature (T_A)	54ACT	-55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) ACT Devices	V_{IN} from 0.8V to 2.0V, V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Electrical Characteristics⁽¹⁾

Symbol	Parameter	V _{CC} (V)	T _A = -55°C to +125°C	Units	Conditions
V _{IH}	Minimum High Level Input Voltage	4.5	2.0	V	V _{OUT} = 0.1V or V _{CC} -0.1V
		5.5	2.0		
V _{IL}	Maximum Low Level Input Voltage	4.5	0.8	V	V _{OUT} = 0.1V or V _{CC} -0.1V
		4.5	0.8		
V _{OH}	Minimum High Level Output Voltage	4.5	3.7	V	I _{OH} = -24 mA
V _{OL}	Maximum Low Level Output Voltage	4.5	0.5	V	I _{OL} = 24 mA
I _{IN}	Maximum Input Leakage Current	5.5	±1.0	µA	V _I = V _{CC} , GND
I _{OZ}	Maximum TRI-STATE Current	5.5	±10.0	µA	V _I = V _{IL} , V _{IH} V _O = V _{CC} , GND
I _{CCT}	Maximum I _{CC} /Input	5.5	1.6	mA	V _I = V _{CC} -2.1V
I _{OLD}	Minimum Dynamic Output Current ⁽²⁾	5.5	50	mA	V _{OLD} = 1.65V Max
I _{OHD}		5.5	-50	mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5	160	µA	V _{IN} = V _{CC} or GND

(1) All outputs loaded; thresholds on input associated with output under test.

(2) Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V) ⁽¹⁾	T _A = -55°C to +125°C C _L = 50 pF		Units	Fig. No.
			Min	Max		
f _{max}	Maximum Clock Frequency	5.0	95		MHz	
t _{PLH}	Propagation Delay CP to O _n	5.0	1.0	12.0	ns	
t _{PHL}	Propagation Delay CP to O _n	5.0	1.0	12.0	ns	
t _{PHL}	Propagation Delay CLR to O _n	5.0	1.0	18.0	ns	
t _{PZH}	Output Enable Time OE to O _n	5.0	1.0	11.5	ns	
t _{PZL}	Output Enable Time OE to O _n	5.0	1.0	12.0	ns	
t _{PHZ}	Output Disable Time OE to O _n	5.0	1.0	13.5	ns	
t _{PLZ}	Output Disable Time OE to O _n	5.0	1.0	12.0	ns	

(1) Voltage Range 5.0 is 5.0V ±0.5V.

AC Operating Requirements

Symbol	Parameter	$V_{CC}(V)^{(1)}$	$T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50$ pF	Units	Fig.
			Ensured Minimum		
t_s	Setup Time, HIGH or LOW D to CP	5.0	4.0	ns	
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	3.0	ns	
t_s	Setup Time, HIGH or LOW \overline{EN} to CP	5.0	4.0	ns	
t_h	Hold Time, HIGH or LOW \overline{EN} to CP	5.0	3.0	ns	
t_w	CP Pulse Width HIGH or LOW	5.0	6.0	ns	
t_w	\overline{CLR} Pulse Width, LOW	5.0	7.5	ns	
t_{rec}	\overline{CLR} to CP Recovery Time	5.0	4.5	ns	

(1) Voltage Range 5.0 is $5.0V \pm 0.5V$.

Table 2. Capacitance

Symbol	Parameter	Max	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = OPEN$
C_{PD}	Power Dissipation Capacitance	4.4	pF	$V_{CC} = 5.0V$

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
<hr/> <ul style="list-style-type: none">• Changed layout of National Data Sheet to TI format	<hr/> 6

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