100355 Low Power Quad Multiplexer/Latch

Check for Samples: 100355

FEATURES

- **Greater than 40% Power Reduction of the 100155**
- **2000V ESD Protection**
- **Pin/Function Compatible with 100155**
- **Voltage Compensated Operating Range = −4.2V to −5.7V**
- **Standard Microcircuit Drawing**
  - **(SMD) 5962-9165401**

DESCRIPTION

The 100355 contains four transparent latches, each of which can accept and store data from two sources. When both Enable ($\overline{E}_n$) inputs are LOW, the data that appears at an output is controlled by the Select (S_n) inputs, as shown in the Operating Mode table. In addition to routing data from either D_0 or D_1, the Select inputs can force the outputs LOW for the case where the latch is transparent (both Enables are LOW) and can steer a HIGH signal from either D_0 or D_1 to an output. The Select inputs can be tied together for applications requiring only that data be steered from either D_0 or D_1. A positive-going signal on either Enable input latches the outputs. A HIGH signal on the Master Reset (MR) input overrides all the other inputs and forces the Q outputs LOW. All inputs have 50 kΩ pulldown resistors.

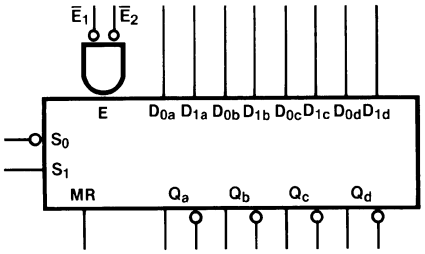


Table 1. PIN DESCRIPTION

Pin Names	Description
$\overline{E}_1$, $\overline{E}_2$	Enable Inputs (Active LOW)
$\overline{S}_0$, S_1	Select Inputs
MR	Master Reset
D_{na}–D_{nd}	Data Inputs
Q_a–Q_d	Data Outputs
$\overline{Q}_a$–$\overline{Q}_d$	Complementary Data Outputs

Connection Diagrams

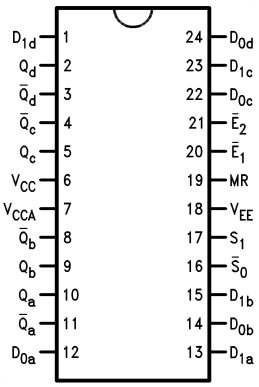


Figure 1. 24-Pin CERDIP

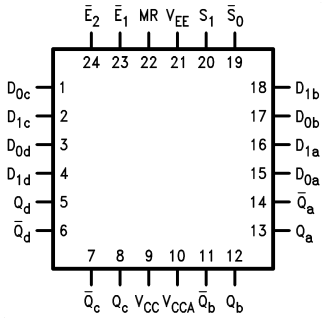
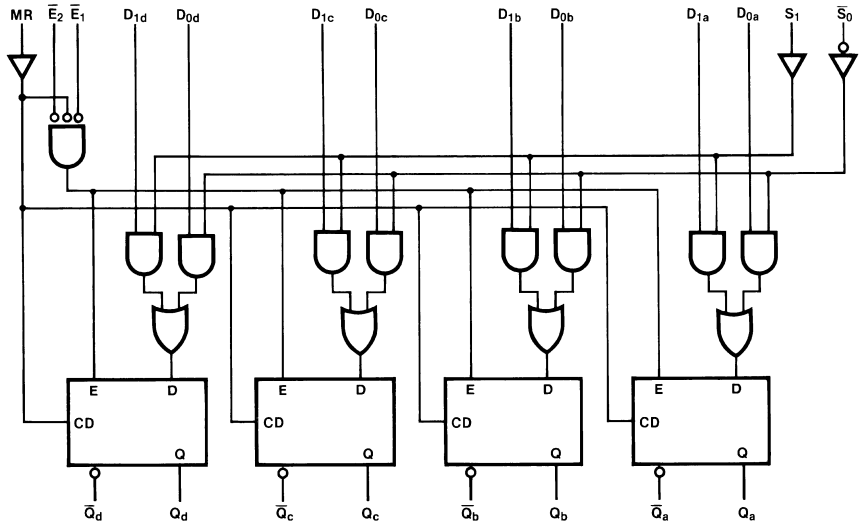


Figure 2. 24-Pin CPGA
See NAQ0024C Package

Logic Diagram



Operating Mode Table

Controls[1]				Outputs
$\overline{E}_1$	$\overline{E}_2$	S_1	$\overline{S}_0$	Q_n
H	X	X	X	Latched [2]
X	H	X	X	Latched [2]
L	L	L	L	D_{0x}
L	L	H	L	$D_{0x} + D_{1x}$
L	L	L	H	L
L	L	H	H	D_{1x}

(1) H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

(2) Stores data present before $\overline{E}$ went HIGH

TRUTH TABLE

Inputs							Outputs	
MR	$\overline{E}_1$	$\overline{E}_2$	S_1	$\overline{S}_0$	D_{1x}	D_{0x}	$\overline{Q}_x$	Q_x
H	X	X	X	X	X	X	H	L
L	L	L	H	H	H	X	L	H
L	L	L	H	H	L	X	H	L
L	L	L	L	L	X	H	L	H
L	L	L	L	L	X	L	H	L
L	L	L	L	H	X	X	H	L
L	L	L	H	L	H	X	L	H
L	L	L	H	L	X	H	L	H
L	L	L	H	L	L	L	H	L
L	H	X	X	X	X	X	Latched (1)	
L	X	H	X	X	X	X	Latched (1)	

(1) Stores data present before $\overline{E}$ went HIGH

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)(2)

Above which the useful life may be impaired.

Storage Temperature (T_{STG})		−65°C to +150°C
Maximum Junction Temperature (T_J)	Ceramic	+175°C
V_{EE} Pin Potential to Ground Pin		−7.0V to +0.5V
Input Voltage (DC)		V_{EE} to +0.5V
Output Current (DC Output HIGH)		−50 mA
ESD (3)		≥2000V

(1) Absolute Maximum Ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) ESD testing conforms to MIL-STD-883, Method 3015.

RECOMMENDED OPERATING CONDITIONS

Case Temperature (T_C)	Military	−55°C to +125°C
Supply Voltage (V_{EE})		−5.7V to −4.2V

MILITARY VERSION
DC ELECTRICAL CHARACTERISTICS

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C

Symbol	Parameter		Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage		−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	See (1) (2) (3)
			−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage		−1830	−1620	mV	0°C to +125°C			
			−1830	−1555	mV	−55°C			
V_{OHC}	Output HIGH Voltage		−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V	See (1) (2) (3)
			−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage			−1610	mV	0°C to +125°C			
				−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage		−1165	−870	mV	−55°C to +125°C	Ensured HIGH Signal for ALL Inputs		See (1) (2) (3) (4)
V_{IL}	Input LOW Voltage		−1830	−1475	mV	−55°C to +125°C	Ensured LOW Signal for ALL Inputs		See (1) (2) (3) (4)
I_{IL}	Input LOW Current		0.50		µA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)		See (1) (2) (3)
I_{IH}	Input HIGH Current	$\overline{S}_0$, S_1		220	µA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)		See (1) (2) (3)
		$\overline{E}_1$, $\overline{E}_2$		350					
		D_{na}–D_{nd}		340					
		MR		430					
		$\overline{S}_0$, S_1		320	µA	−55°C			
		$\overline{E}_1$, $\overline{E}_2$		500					
		D_{na}–D_{nd}		490					
		MR		630					
I_{EE}	Power Supply Current		−95	−32	mA	−55°C to +125°C	Inputs Open		See (1) (2) (3)

(1) F100K 300 Series cold temperature testing is performed by temperature soaking (to Ensure junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides “cold start” specs which can be considered a worst case condition at cold temperatures.
(2) Screen tested 100% on each device at −55°C, +25°C, and +125°C Temp., Subgroups 1, 2, 3, 7, and 8.
(3) Sample tested (Method 5005, Table 1) on each Mfg. lot at +25°, +125°C, and −55°C Temp., Subgroups 1, 2, 3, 7, and 8.
(4) Ensured by applying specified input condition and testing V_{OH}/V_{OL}.

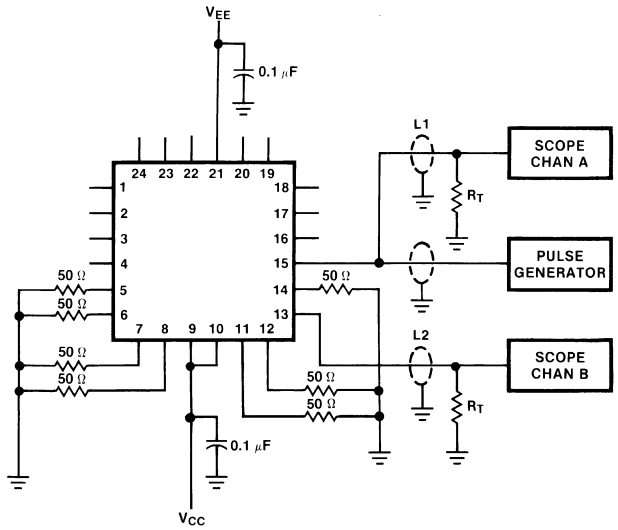
MILITARY VERSION
AC ELECTRICAL CHARACTERISTICS

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter		T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
			Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay D_{na}–D_{nd} to Output (Transparent Mode)		0.40	2.30	0.50	2.20	0.50	2.60	ns	Figure 4, Figure 6	See (1) (2) (3)
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_0$, S_1 to Output (Transparent Mode)		0.60	3.00	0.80	2.70	0.80	3.20	ns		
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$, $\overline{E}_2$ to Output		0.50	2.60	0.60	2.30	0.70	2.70	ns		
t_{PLH} t_{PHL}	Propagation Delay MR to Output		0.60	2.80	0.70	2.60	0.70	2.90	ns	Figure 4, Figure 7	See (1) (2) (3)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%		0.40	1.90	0.40	1.90	0.40	1.90	ns	Figure 4 Figure 6	See (4)
t_S	Setup Time	D_{na}–D_{nd}	0.90		0.90		0.90		ns	Figure 8	See (4)
		$\overline{S}_0$, S_1	2.40		2.40		2.40				
		MR (Release Time)	1.50		1.50		1.50			Figure 7	
t_H	Hold Time	D_{na}–D_{nd}	0.40		0.40		0.40		ns	Figure 8	See (4)
		$\overline{S}_0$, S_1	0.00		0.00		0.00				
t_{pw} (L)	Pulse Width LOW $\overline{E}_1$, $\overline{E}_2$		2.00		2.00		2.00		ns	Figure 6	See (4)
t_{pw} (H)	Pulse Width HIGH MR		2.00		2.00		2.00		ns	Figure 7	See (4)

(1) F100K 300 Series cold temperature testing is performed by temperature soaking (to Ensure junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides “cold start” specs which can be considered a worst case condition at cold temperatures.
(2) Screen tested 100% on each device at +25°C, Temperature only, Subgroup A9.
(3) Sample tested (Method 5005, Table 1) on each Mfg. lot at +25°, Subgroup A9, and at +125°C, and −55°C Temp., Subgroups A10 & A11.
(4) Not tested at +25°C, +125°C and −55°C Temperature (design characterization data).

Figure 3. TEST CIRCUIT



Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 µF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

Figure 4. AC Test Circuit

Figure 5. SWITCHING WAVEFORMS

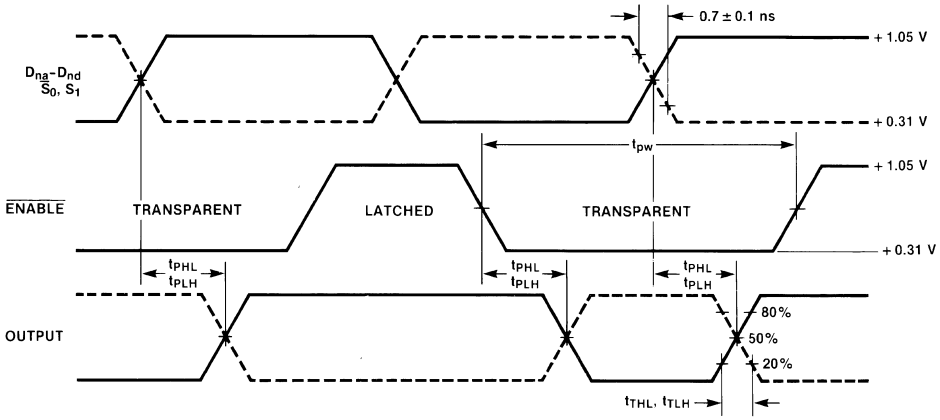


Figure 6. Enable Timing

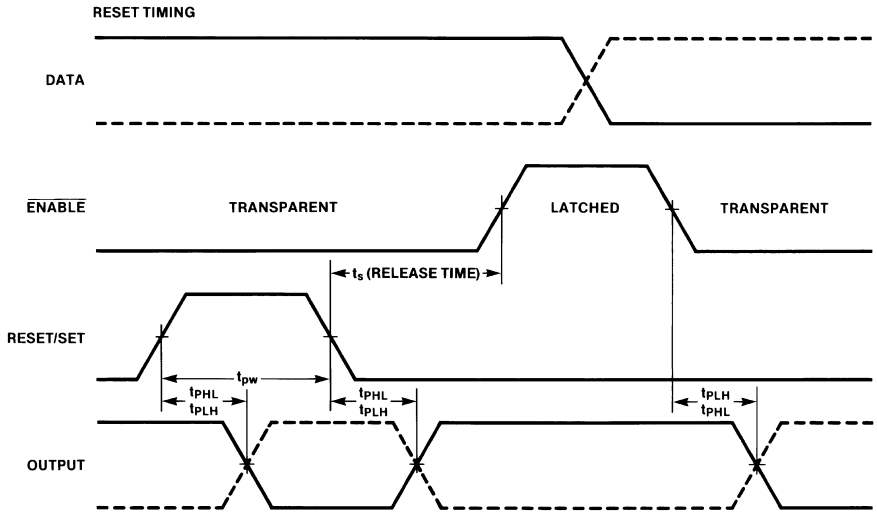
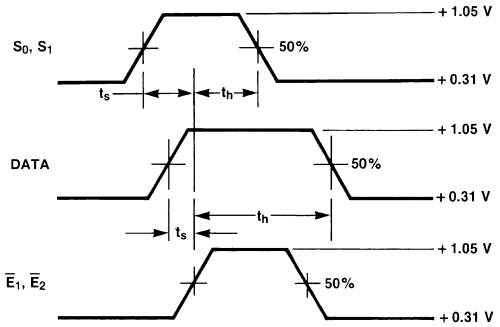


Figure 7. Reset Timing



Notes:

t_s is the minimum time before the transition of the enable that information must be present at the data input.

t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input.

Figure 8. Data Setup and Hold Times

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	7

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265