

100352

100352 Low Power 8-Bit Buffer with Cut-Off Drivers



Literature Number: SNOS112

100352 Low Power 8-Bit Buffer with Cut-Off Drivers

General Description

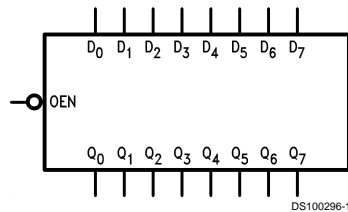
The 100352 contains an 8-bit buffer, individual inputs (Dn), outputs (Qn), and a data output enable pin ($\overline{\text{OEN}}$). A Q output follows its D input when the $\overline{\text{OEN}}$ pin is LOW. A HIGH on $\overline{\text{OEN}}$ holds the outputs in a cut-off state. The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is -2.0V , presenting a high impedance to the data bus. This high impedance reduces termination power and prevents loss of low state noise margin when several loads share the bus.

The 100352 outputs are designed to drive a doubly terminated 50Ω transmission line (25Ω load impedance). All inputs have $50\text{ k}\Omega$ pull-down resistors.

Features

- Cut-off drivers
- Drives 25Ω load
- Low power operation
- 2000V ESD protection
- Voltage compensated operating range = -4.2V to -5.7V
- Available to industrial grade temperature range
- Available to MIL-STD-883

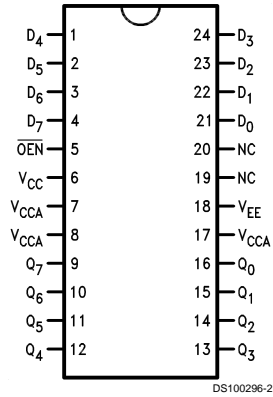
Logic Symbol



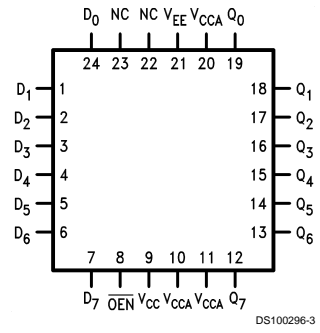
Pin Names	Description
D ₀ -D ₇	Data Inputs
$\overline{\text{OEN}}$	Output Enable Input
Q ₀ -Q ₇	Data Outputs
NC	No Connect

Connection Diagrams

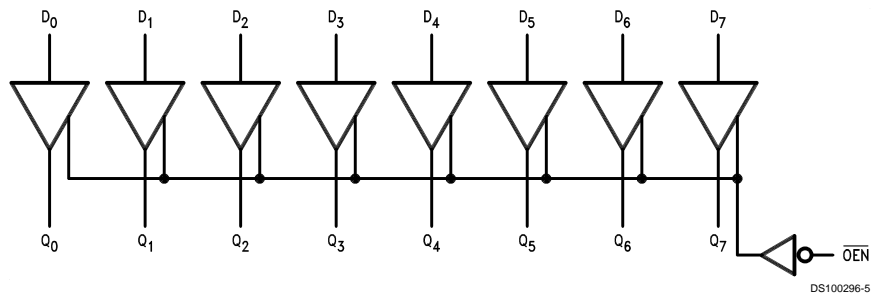
24-Pin DIP



24-Pin Quad Cerpak



Logic Diagram



Truth Table

Inputs		Outputs
Dn	\overline{OEN}	Qn
L	L	L
H	L	H
X	H	Cutoff

H = HIGH Voltage Level
 L = LOW Voltage Level
 Cutoff = Lower-than-LOW State
 X = Don't Care

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Above which the useful life may be impaired	
Storage Temperature (T_{STG})	-65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
V_{EE} Pin Potential to Ground Pin	-7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	-100 mA

ESD (Note 2)

≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Military	-55°C to +125°C
Supply Voltage (V_{EE})	-5.7V to -4.2V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Military Version DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55^\circ C$ to $+125^\circ C$

Symbol	Parameter	Min	Max	Units	T_C	Conditions	Notes	
V_{OH}	Output HIGH Voltage	-1025	-870	mV	0°C to +125°C	$V_{IN} = V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 25Ω to -2.0V	(Notes 3, 4, 5)
		-1085	-870	mV	-55°C			
V_{OL}	Output LOW Voltage	-1830	-1620	mV	0°C to +125°C			
		-1830	-1555	mV	-55°C			
V_{OHC}	Output HIGH Voltage	-1035		mV	0°C to +125°C	$V_{IN} = V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 25Ω to -2.0V	(Notes 3, 4, 5)
		-1085		mV	-55°C			
V_{OLC}	Output LOW Voltage		-1610	mV	0°C to +125°C			
			-1555	mV	-55°C			
V_{OLZ}	Cut-Off LOW Voltage		-1950	mV	0°C to +125°C	$V_{IN} = V_{IH(Min)}$, or $V_{IL(Max)}$	OEN = HIGH	(Notes 3, 4, 5)
			-1850	mV	-55°C			
V_{IH}	Input HIGH Voltage	-1165	-870	mV	-55°C to +125°C	Guaranteed HIGH signal for All inputs		1, 2, 3, 4
V_{IL}	Input LOW Voltage	-1830	-1475	mV	-55°C to +125°C	Guaranteed LOW signal for All inputs		(Notes 3, 4, 5, 6)
I_{IL}	Input LOW Current	0.50		μA	-55°C to +125°C	$V_{EE} = 4.2V$ $V_{IN} = V_{IL(Min)}$		(Notes 3, 4, 5)
I_{IH}	Input HIGH Current		240	μA	0°C to +125°C	$V_{EE} = -5.7V$ $V_{IN} = V_{IH(Max)}$		(Notes 3, 4, 5)
			340	μA	-55°C			
I_{EE}	Power Supply Current	-145 -150	-55	mA	-55°C to +125°C	Inputs Open $V_{EE} = -4.2V$ to $-4.8V$ $V_{EE} = -4.2V$ to $-5.7V$		(Notes 3, 4, 5)

Note 3: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals -55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 4: Screen tested 100% on each device at -55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 5: Sample tested (Method 5005, Table I) on each manufactured lot at -55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 6: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH}	Propagation Delay	0.30	2.60	0.50	2.40	0.50	2.70	ns	Figures 1, 2	(Notes 7, 8, 10, 11)
t_{PHL}	Dn to Output									
t_{PZH}	Propagation Delay	1.20	4.40	1.40	4.20	1.20	4.40	ns	Figures 1, 2	(Notes 7, 8, 9, 11)
t_{PHZ}	OEN to Output	0.70	3.00	0.70	2.80	0.70	3.20			

AC Electrical Characteristics (Continued)

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{TLH}	Transition Time	0.40	2.50	0.40	2.40	0.40	2.70	ns	Figures 1, 2	(Note 10)
t_{THL}	20% to 80%, 80% to 20%									

Note 7: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

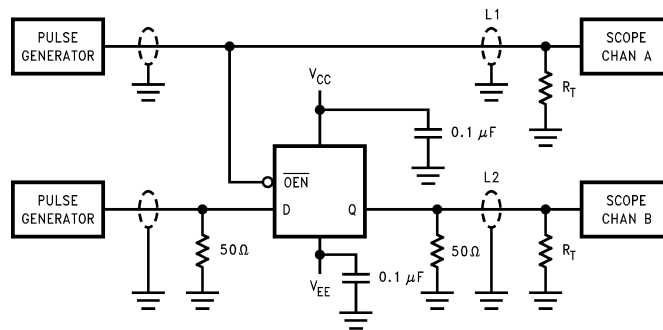
Note 8: Screen tested 100% on each device at $+25^\circ C$ temperature only, Subgroup A9.

Note 9: Sample tested (Method 5005, Table I) on each manufactured lot at $+25^\circ C$, Subgroup A9, and at $+125^\circ C$ and $-55^\circ C$ temperatures, Subgroups A10 and A11.

Note 10: Not tested at $+25^\circ C$, $+125^\circ C$, and $-55^\circ C$ temperature (design characterization data).

Note 11: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Test Circuitry



DS100296-6

Notes:

V_{CC} , $V_{CCA} = +2V$, $V_{EE} = -2.5V$

L1 and L2 = equal length 50 ohm impedance lines

$R_T = 50\Omega$ terminator internal to scope

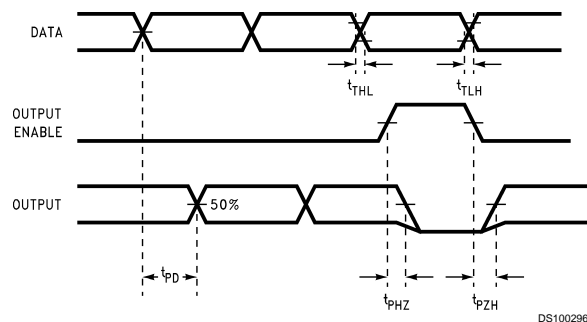
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 25 ohm to GND

C_L = Fixture and stray capacitance ≤ 3 pF

FIGURE 1. AC Test Circuit

Switching Waveforms



DS100296-7

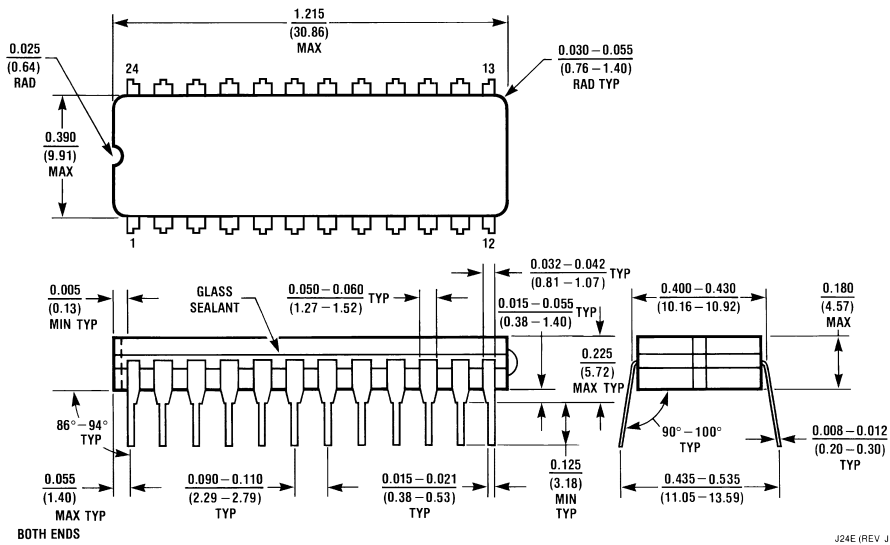
Note:

The output AC measurement point for cut-off propagation delay testing = the 50% voltage point between active V_{OL} and V_{OH} .

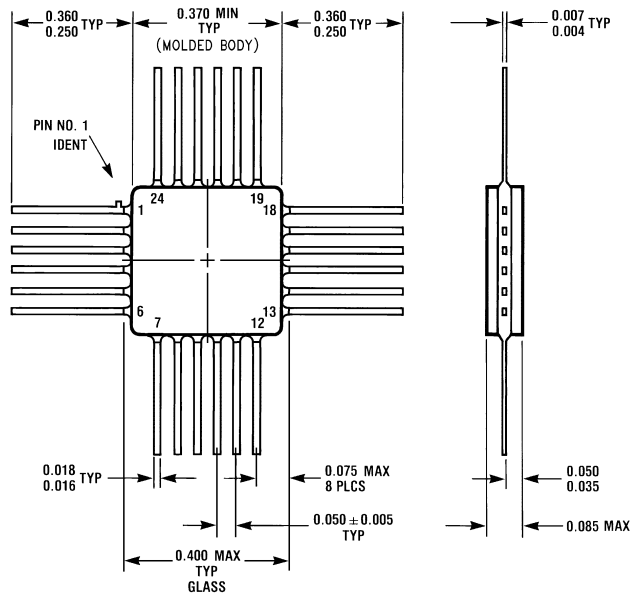
FIGURE 2. Propagation Delay, Cut-Off and Transition Times



Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Ceramic Dual-In-Line Package (0.400" Wide) (D)
NS Package Number J24E



24-Lead Quad Cerpak (F)
NS Package Number W24B

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