

100343

100343 Low Power 8-Bit Latch



Literature Number: SNOS114

100343 Low Power 8-Bit Latch

General Description

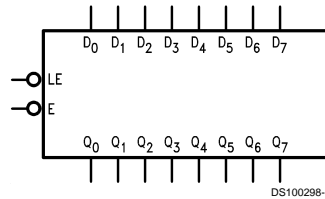
The 100343 contains eight D-type latches, individual inputs, (D_n), outputs (Q_n), a common enable pin (\bar{E}), and a latch enable pin (\overline{LE}). A Q output follows its D input when both \bar{E} and \overline{LE} are LOW. When either \bar{E} or \overline{LE} (or both) are HIGH, a latch stores the last valid data present on its D input prior to \bar{E} or \overline{LE} going HIGH.

The 100343 outputs are designed to drive a 50 Ω termination resistor to -2.0V. All inputs have 50 k Ω pull-down resistors.

Features

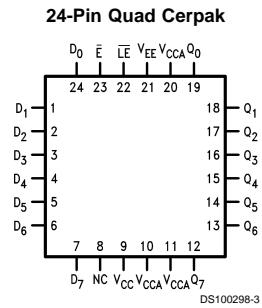
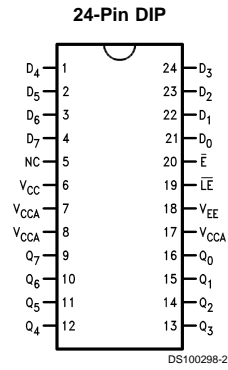
- Low power operation
- 2000V ESD protection
- Voltage compensated operating range = -4.2V to -5.7V
- Available to MIL-STD-883

Logic Symbol

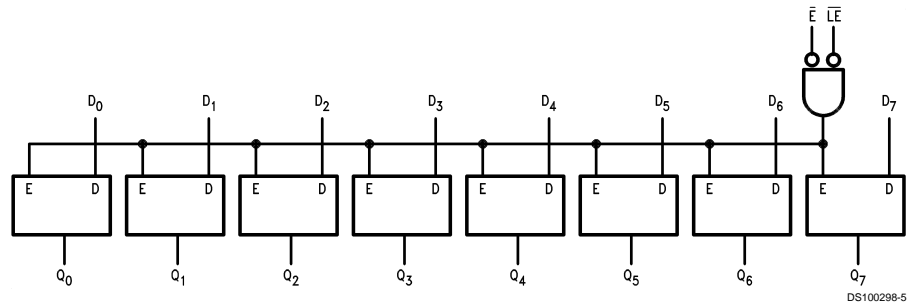


Pin Names	Description
D_0 - D_7	Data Inputs
\bar{E}	Enable Input
\overline{LE}	Latch Enable Input
Q_0 - Q_7	Data Outputs
NC	No Connect

Connection Diagrams



Logic Diagram



Truth Table

Inputs			Outputs
D_n	\bar{E}	\bar{LE}	Q_n
L	L	L	L
H	L	L	H
X	H	X	Latched (Note 1)
X	X	H	Latched (Note 1)

H = HIGH voltage level

L = LOW voltage level

X = Don't care

Note 1: Retains data present before either \bar{LE} or \bar{E} went HIGH

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	-65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
V_{EE} Pin Potential to Ground Pin	-7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	-50 mA
ESD (Note 3)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Military	-55°C to +125°C
Supply Voltage (V_{EE})	-5.7V to -4.2V

Note 2: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: ESD testing conforms to MIL-STD-883, Method 3015.

Military Version DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55°C$ to $+125°C$

Symbol	Parameter	Min	Max	Units	T_C	Conditions	Notes	
V_{OH}	Output HIGH Voltage	-1025	-870	mV	0°C to +125°C	$V_{IN} = V_{IH}$ (Max) or V_{IL} (Min)	Loading with 50Ω to -2.0V	1, 2, 3
		-1085	-870	mV	-55°C			
V_{OL}	Output LOW Voltage	-1830	-1620	mV	0°C to +125°C			
		-1830	-1555	mV	-55°C			
V_{OHC}	Output HIGH Voltage	-1035		mV	0°C to +125°C	$V_{IN} = V_{IH}$ (Max) or V_{IL} (Min)	Loading with 50Ω to -2.0V	1, 2, 3
		-1085		mV	-55°C			
V_{OLC}	Output LOW Voltage		-1610	mV	0°C to +125°C			
			-1555	mV	-55°C			
V_{IH}	Input HIGH Voltage	-1165	-870	mV	-55°C to +125°C	Guaranteed HIGH Signal for All Inputs	1, 2, 3, 4	
V_{IL}	Input LOW Voltage	-1830	-1475	mV	-55°C to +125°C	Guaranteed LOW Signal for All Inputs	1, 2, 3, 4	
I_{IL}	Input LOW Current	0.50		μA	-55°C to +125°C	$V_{EE} = -4.2V$ $V_{IN} = V_{IL}$ (Min)	1, 2, 3	
I_{IH}	Input HIGH Current		240	μA	0°C to +125°C	$V_{EE} = -5.7V$ $V_{IN} = V_{IH}$ (Max)	1, 2, 3	
			340	μA	-55°C			
I_{EE}	Power Supply Current				-55°C to +125°C	Inputs Open	1, 2, 3	
		-100	-35	mA		$V_{EE} = -4.2V$ to $-4.8V$		
		-105	-35	mA		$V_{EE} = -4.2V$ to $-5.7V$		

Note 4: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals -55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 5: Screen tested 100% on each device at -55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 6: Sample tested (Method 5005, Table I) on each manufactured lot at -55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 7: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

Military Version AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55°C$		$T_C = +25°C$		$T_C = +125°C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH}	Propagation Delay	0.50	2.70	0.50	2.30	0.50	2.80	ns	Figures 1, 2, 3	(Notes 8, 9, 10, 12)
t_{PHL}	D_n to Output									

Military Version AC Electrical Characteristics (Continued)

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH}	Propagation Delay	0.90	3.40	1.0	3.10	1.10	3.90	ns	Figures 1, 2, 3	(Notes 8, 9, 10, 12)
t_{PHL}	\overline{LE} , \overline{E} to Output									
t_{TLH}	Transition Time	0.40	2.50	0.40	2.40	0.40	2.70	ns	Figures 1, 3	(Note 11)
t_{THL}	20% to 80%, 80% to 20%									
t_s	Setup Time								Figures 1, 4	(Note 11)
	D_0-D_7	0.60		0.60		0.60		ns		
t_h	Hold Time								Figures 1, 4	(Note 11)
	D_0-D_7	1.50		1.50		1.70		ns		
$t_{pw(H)}$	Pulse Width HIGH								Figures 1, 4	(Note 11)
	\overline{LE} , \overline{E}	2.40		2.40		2.40		ns		

Note 8: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

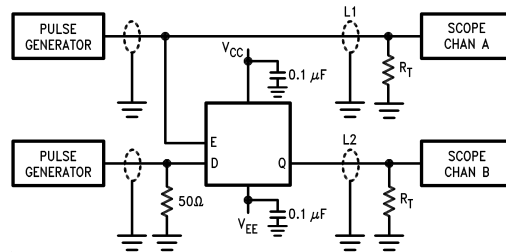
Note 9: Screen tested 100% on each device at $+25^\circ C$ temperature only, Subgroup A9.

Note 10: Sample tested (Method 5005, Table I) on each manufactured lot at $+25^\circ C$, Subgroup A9, and at $+125^\circ C$ and $-55^\circ C$ temperatures, Subgroups A10 and A11.

Note 11: Not tested at $+25^\circ C$, $+125^\circ C$, and $-55^\circ C$ temperature (design characterization data).

Note 12: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Test Circuitry



DS100298-6

Note 13: V_{CC} , $V_{CCA} = +2V$, $V_{EE} = -2.5V$

Note 14: L1 and L2 = equal length 50Ω impedance lines

$R_T = 50\Omega$ terminator internal to scope

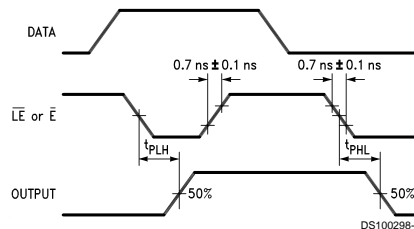
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

$C_L =$ Fixture and stray capacitance ≤ 3 pF

FIGURE 1. AC Test Circuit

Switching Waveforms



DS100298-7

FIGURE 2. Propagation Delays

Switching Waveforms (Continued)

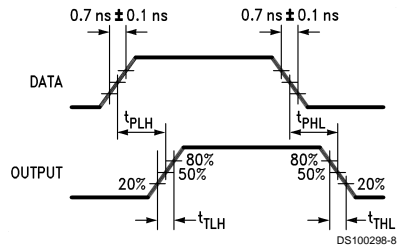


FIGURE 3. Propagation and Transition Times

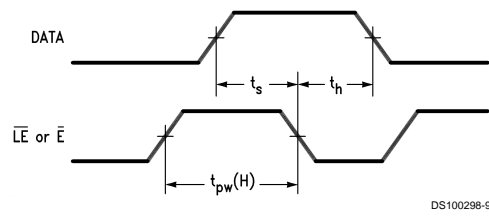
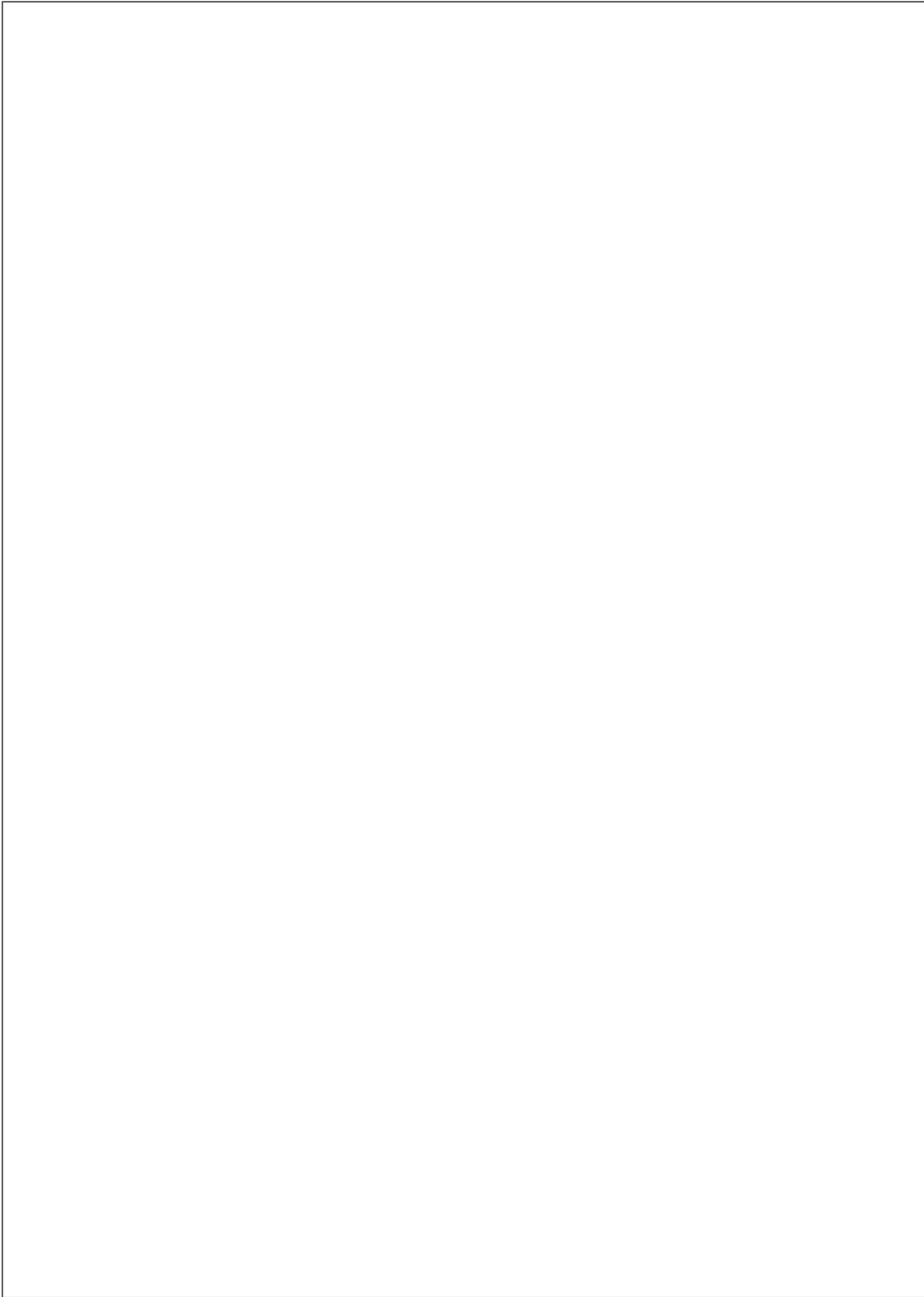
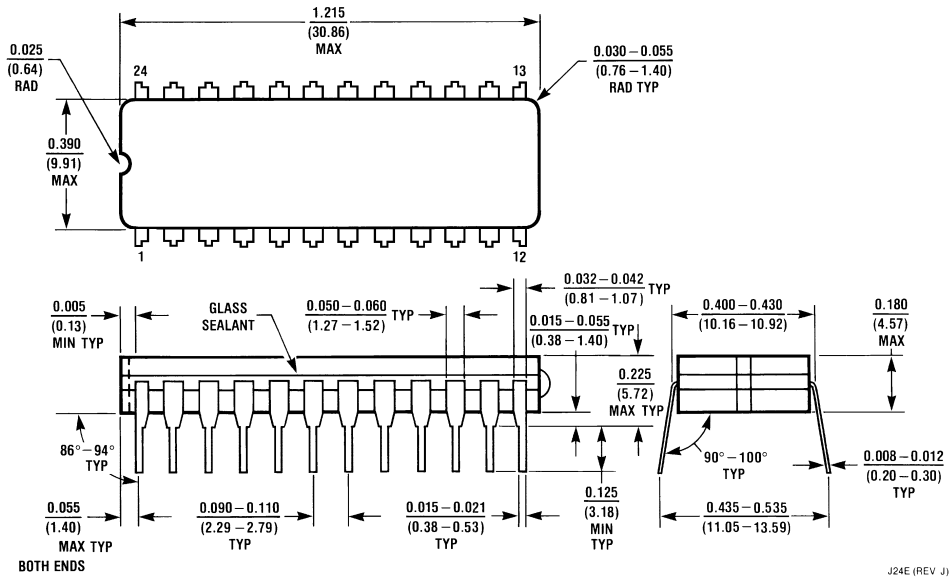


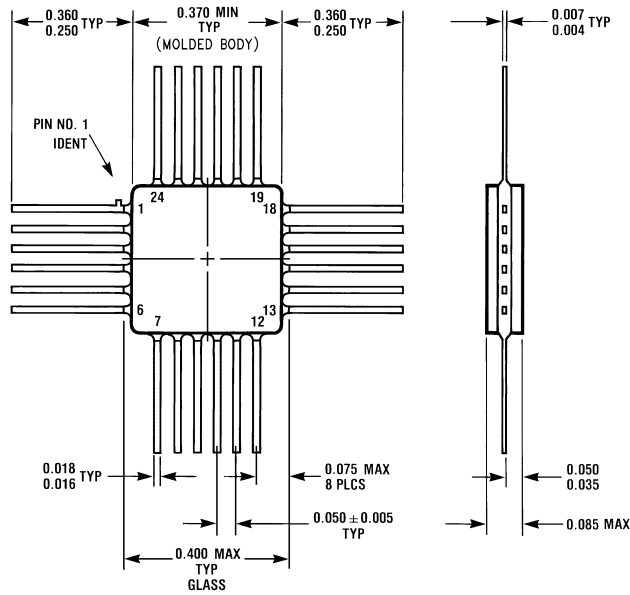
FIGURE 4. Setup, Hold and Pulse Width Times



Physical Dimensions inches (millimeters) unless otherwise noted



24-Pin Ceramic Dual-In-Line Package (D)
NS Package Number J24E



24-Lead Quad Cerpak (F)
NS Package Number W24B

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