

100302 Low Power Quint 2-Input OR/NOR Gate

Check for Samples: [100302](#)

FEATURES

- 43% Power Reduction of the 100102
- 2000V ESD Protection
- Pin/Function Compatible with 100102
- Voltage Compensated Operating Range = -4.2V to -5.7V
- Standard Microcircuit Drawing
 - (SMD) 5962-9152802

DESCRIPTION

The 100302 is a monolithic quint 2-input OR/NOR gate with common enable. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Logic Symbol

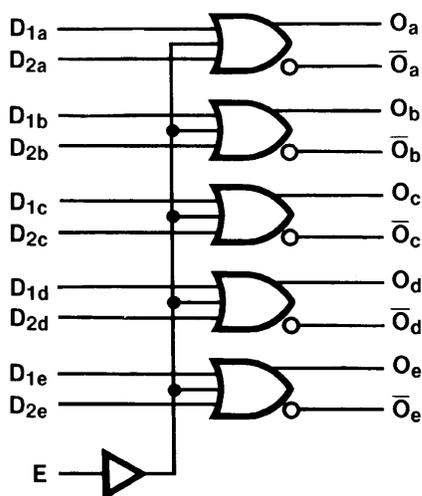


Table 1. Pin Descriptions

Pin Names	Description
$D_{na}-D_{ne}$	Data Inputs
E	Enable Input
O_a-O_e	Data Outputs
$\bar{O}_a-\bar{O}_e$	Complementary Data Outputs

TRUTH TABLE⁽¹⁾

D_{1x}	D_{2x}	E	O_x	\bar{O}_x
L	L	L	L	H
L	L	H	H	L
L	H	L	H	L
L	H	H	H	L
H	L	L	H	L
H	L	H	H	L
H	H	L	H	L
H	H	H	H	L

(1) H = HIGH Voltage Level
L = LOW Voltage Level



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Connection Diagram

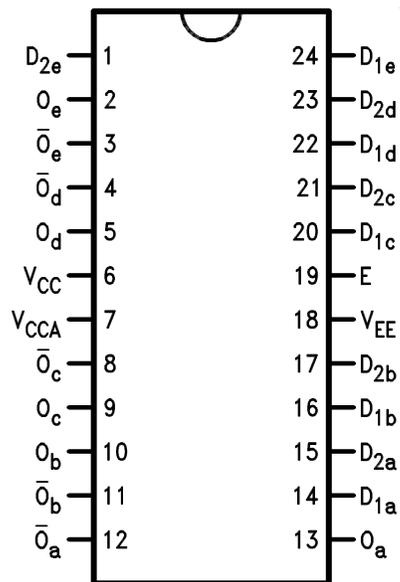


Figure 1. 24-Pin Cerdip

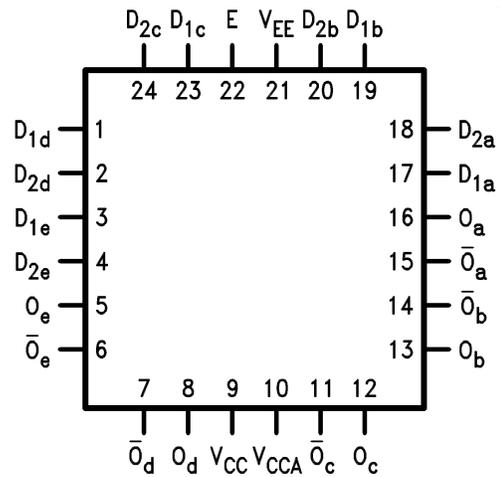


Figure 2. 24-Pin CPGA
See NAQ0024C Package



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾⁽²⁾

Above which the useful life may be impaired

Storage Temperature (T _{STG})		-65°C to +150°C
Maximum Junction Temperature (T _J)	Ceramic	+175°C
V _{EE} Pin Potential to Ground Pin		-7.0V to +0.5V
Input Voltage (DC)		V _{EE} to +0.5V
Output Current (DC Output HIGH)		-50 mA
ESD ⁽³⁾		≥2000V

- (1) Absolute Maximum Ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
- (3) ESD testing conforms to MIL-STD-883, Method 3015.

RECOMMENDED OPERATING CONDITIONS

Case Temperature (T _C)	Military	-55°C to +125°C
Supply Voltage (V _{EE})		-5.7V to -4.2V

DC ELECTRICAL CHARACTERISTICS - MILITARY VERSION

V_{EE} = -4.2V to -5.7V, V_{CC} = V_{CCA} = GND, T_C = -55°C to +125°C ⁽¹⁾

Symbol	Parameter	Min	Max	Units	T _C	Conditions	Notes	
V _{OH}	Output HIGH Voltage	-1025	-870	mV	0°C to +125°C	V _{IN} = V _{IH(Max)} or V _{IL} (Min)	Loading with 50Ω to -2.0V	See ⁽¹⁾⁽²⁾⁽³⁾
		-1085	-870	mV	-55°C			
V _{OL}	Output LOW Voltage	-1830	-1620	mV	0°C to +125°C	V _{IN} = V _{IH(Max)} or V _{IL} (Min)	Loading with 50Ω to -2.0V	See ⁽¹⁾⁽²⁾⁽³⁾
		-1830	-1555	mV	-55°C			
V _{OHC}	Output HIGH Voltage	-1035		mV	0°C to +125°C	V _{IN} = V _{IH(Max)} or V _{IL} (Min)	Loading with 50Ω to -2.0V	See ⁽¹⁾⁽²⁾⁽³⁾
		-1085		mV	-55°C			
V _{OLC}	Output LOW Voltage		-1610	mV	0°C to +125°C	V _{IN} = V _{IH(Max)} or V _{IL} (Min)	Loading with 50Ω to -2.0V	See ⁽¹⁾⁽²⁾⁽³⁾
			-1555	mV	-55°C			
V _{IH}	Input HIGH Voltage	-1165	-870	mV	-55°C to +125°C	Ensured HIGH Signal for All Inputs	See ⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾	
V _{IL}	Input LOW Voltage	-1830	-1475	mV	-55°C to +125°C	Ensured LOW Signal for All Inputs	See ⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾	
I _{IL}	Input LOW Current	0.50		μA	-55°C to +125°C	V _{EE} = -4.2V V _{IN} = V _{IH} (Max)	See ⁽²⁾⁽³⁾⁽¹⁾	
I _{IH}	Input HIGH Current		240	μA	0°C to +125°C	V _{EE} = -5.7V V _{IN} = V _{IL} (Min)	See ⁽¹⁾⁽²⁾⁽³⁾	
			340	μA	-55°C			
I _{EE}	Power Supply Current	-48	-17	mA	-55°C to +125°C	Inputs Open	See ⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾	

- (1) Sample tested (Method 5005, Table I) on each manufactured lot at -55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.
- (2) F100K 300 Series cold temperature testing is performed by temperature soaking (to ensure junction temperature equals -55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.
- (3) Screen tested 100% on each device at -55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.
- (4) Ensured by applying specified input condition and testing V_{OH}/V_{OL}.

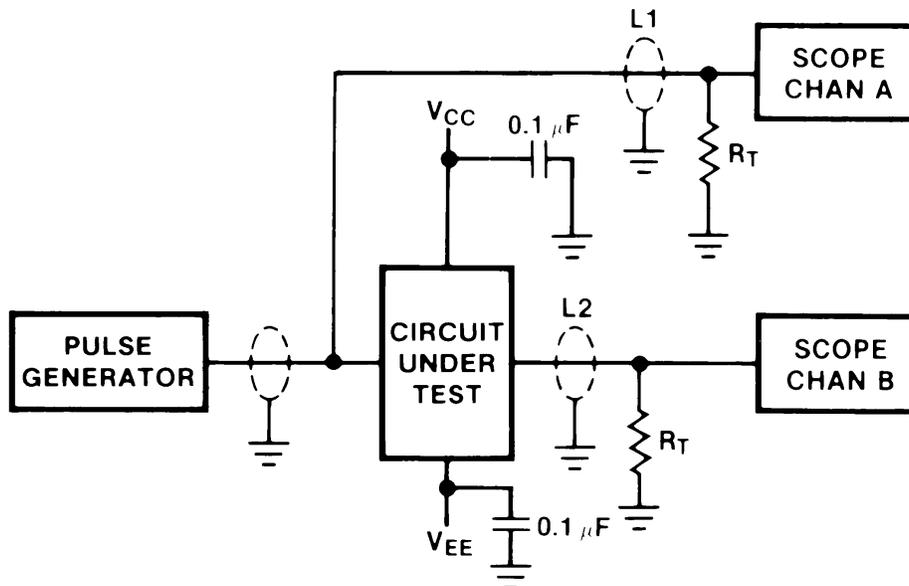
AC ELECTRICAL CHARACTERISTICS

 $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.30	1.80	0.40	1.50	0.40	1.70	ns	See Figure 3 and Figure 4	See (1)(2)(3)(4)(5)
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.60	2.60	0.80	2.30	0.80	2.80	ns		
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	1.20	0.30	1.20	0.30	1.20	ns		See (4)

- (1) F100K 300 Series cold temperature testing is performed by temperature soaking (to ensure junction temperature equals $-55^\circ C$), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.
- (2) Screen tested 100% on each device at $+25^\circ C$ temperature only, Subgroup A9.
- (3) Sample tested (Method 5005, Table I) on each manufactured lot at $+25^\circ C$, Subgroup A9, and at $+125^\circ C$ and $-55^\circ C$ temperatures, Subgroups A10 and A11.
- (4) Not tested at $+25^\circ C$, $+125^\circ C$, and $-55^\circ C$ temperature (design characterization data).
- (5) The propagation delay specified is for single output switching. Delays may vary up to 100 ps with multiple outputs switching.

TEST CIRCUITRY



$V_{CC}, V_{CCA} = +2V$, $V_{EE} = -2.5V$
 $L1$ and $L2$ = equal length 50Ω impedance lines
 $R_T = 50\Omega$ terminator internal to scope
 Decoupling $0.1 \mu F$ from GND to V_{CC} and V_{EE}
 All unused outputs are loaded with 50Ω to GND
 C_L = Fixture and stray capacitance ≤ 3 pF

Figure 3. AC Test Circuit

Switching Waveforms

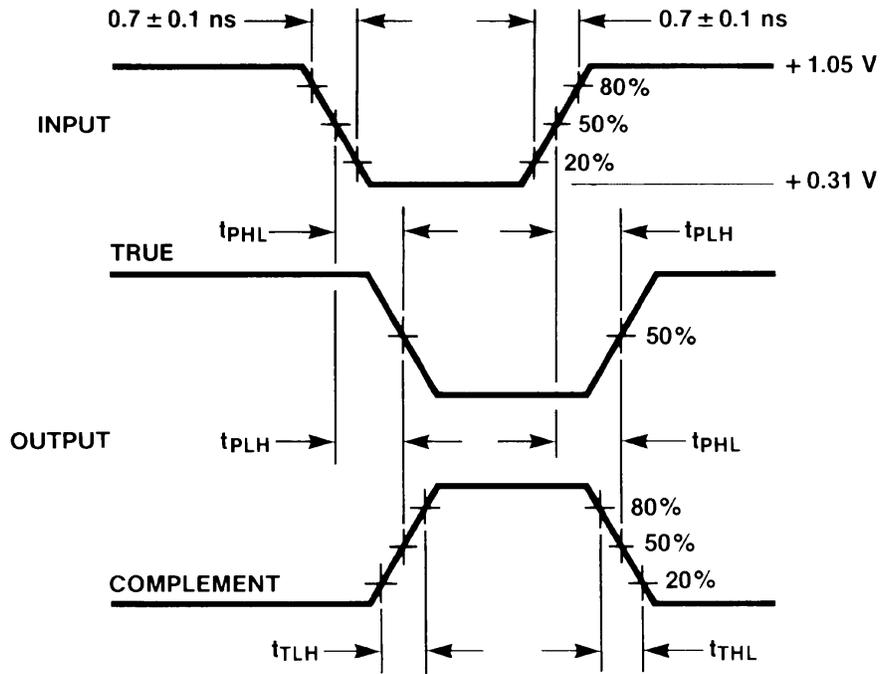


Figure 4. Propagation Delay and Transition Times

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	5

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