

100304 Low Power Quint AND/NAND Gate

Check for Samples: [100304](#)

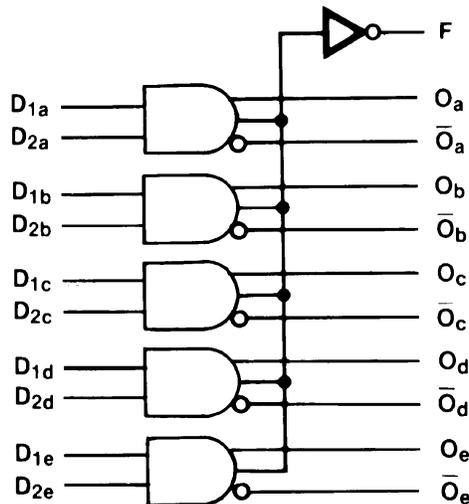
FEATURES

- Low Power Operation
- 2000V ESD Protection
- Pin/Function Compatible with 100104
- Voltage Compensated Operating Range = –4.2V to –5.7V
- Available to Industrial Grade Temperature Range
- Available to Standard Microcircuit Drawing
 - (SMD) 5962-9153701

DESCRIPTION

The 100304 is monolithic quint AND/NAND gate. The Function output is the wire-NOR of all five AND gate outputs. All inputs have 50 kΩ pull-down resistors.

Logic Symbol



Logic Equation

$$F = (D_{1a} \cdot D_{2a}) + (D_{1b} \cdot D_{2b}) + (D_{1c} \cdot D_{2c}) + (D_{1d} \cdot D_{2d}) + (D_{1e} \cdot D_{2e}). \quad (1)$$

Table 1. Pin Descriptions

Pin Names	Description
D_{na} – D_{ne}	Data Inputs
F	Function Output
O_a – O_e	Data Outputs
\bar{O}_a – \bar{O}_e	Complementary Data Outputs



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Connection Diagram

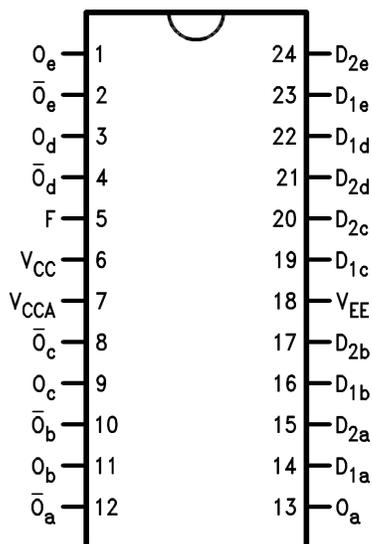


Figure 1. 24-Pin Cerdip

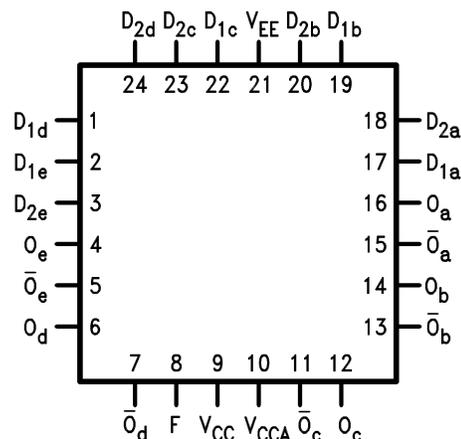


Figure 2. 24-Pin CPGA
See NAQ0024C Package



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾⁽²⁾

Above which the useful life may be impaired

Storage Temperature (T _{STG})		-65°C to +150°C
Maximum Junction Temperature (T _J)	Ceramic	+175°C
V _{EE} Pin Potential to Ground Pin		-7.0V to +0.5V
Input Voltage (DC)		V _{EE} to +0.5V
Output Current (DC Output HIGH)		-50 mA
ESD ⁽³⁾		≥2000V

- (1) Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
- (3) ESD testing conforms to MIL-STD-883, Method 3015.

RECOMMENDED OPERATING CONDITIONS

Case Temperature (T _C)	Military	-55°C to +125°C
Supply Voltage (V _{EE})		-5.7V to -4.2V

DC ELECTRICAL CHARACTERISTICS - MILITARY VERSION
 $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55^{\circ}C$ to $+125^{\circ}C$

Symbol	Parameter	Min	Max	Units	T_C	Conditions	Notes
V_{OH}	Output HIGH Voltage	-1025	-870	mV	$0^{\circ}C$ to $+125^{\circ}C$	$V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$	Loading with 50Ω to $-2.0V$
		-1085	-870	mV	$-55^{\circ}C$		
V_{OL}	Output LOW Voltage	-1830	-1620	mV	$0^{\circ}C$ to $+125^{\circ}C$		
		-1830	-1555	mV	$-55^{\circ}C$		
V_{OHC}	Output HIGH Voltage	-1035		mV	$0^{\circ}C$ to $+125^{\circ}C$	$V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$	Loading with 50Ω to $-2.0V$
		-1085		mV	$-55^{\circ}C$		
V_{OLC}	Output LOW Voltage		-1610	mV	$0^{\circ}C$ to $+125^{\circ}C$		
			-1555	mV	$-55^{\circ}C$		
V_{IH}	Input HIGH Voltage	-1165	-870	mV	$-55^{\circ}C$ to $+125^{\circ}C$	Ensured HIGH Signal for All Inputs	See (1)(2)(3)(4)
V_{IL}	Input LOW Voltage	-1830	-1475	mV	$-55^{\circ}C$ to $+125^{\circ}C$	Ensured LOW Signal for All Inputs	See (1)(2)(3)(4)
I_{IL}	Input LOW Current	0.50		μA	$-55^{\circ}C$ to $+125^{\circ}C$	$V_{EE} = -4.2V$ $V_{IN} = V_{IL} (Min)$	See (1)(2)(3)
I_{IH}	Input High Current					$V_{EE} = -5.7V$ $V_{IN} = V_{IH} (Max)$	See (1)(2)(3)
	$D_{2a}-D_{2e}$		250	μA	$0^{\circ}C$ to $+125^{\circ}C$		
	$D_{1a}-D_{1e}$		350				
	$D_{2a}-D_{2e}$		350	μA	$-55^{\circ}C$		
	$D_{1a}-D_{1e}$		500				
I_{EE}	Power Supply Current	-75	-25	mA	$-55^{\circ}C$ to $+125^{\circ}C$	Inputs Open	See (5)(6)(7)

- (1) F100K 300 Series cold temperature testing is performed by temperature soaking (to ensure junction temperature equals $-55^{\circ}C$), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.
- (2) Screen tested 100% on each device at $-55^{\circ}C$, $+25^{\circ}C$, and $+125^{\circ}C$, Subgroups, 1, 2 3, 7, and 8.
- (3) Sample tested (Method 5005, Table I) on each manufactured lot at $-55^{\circ}C$, $+25^{\circ}C$, and $+125^{\circ}C$, Subgroups A1, 2, 3, 7, and 8.
- (4) Ensured by applying specified input condition and testing V_{OH}/V_{OL} .
- (5) F100K 300 Series cold temperature testing is performed by temperature soaking (to ensure junction temperature equals $-55^{\circ}C$), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.
- (6) Screen tested 100% on each device at $-55^{\circ}C$, $+25^{\circ}C$, and $+125^{\circ}C$, Subgroups, 1, 2 3, 7, and 8.
- (7) Sample tested (Method 5005, Table I) on each manufactured lot at $-55^{\circ}C$, $+25^{\circ}C$, and $+125^{\circ}C$, Subgroups A1, 2, 3, 7, and 8.

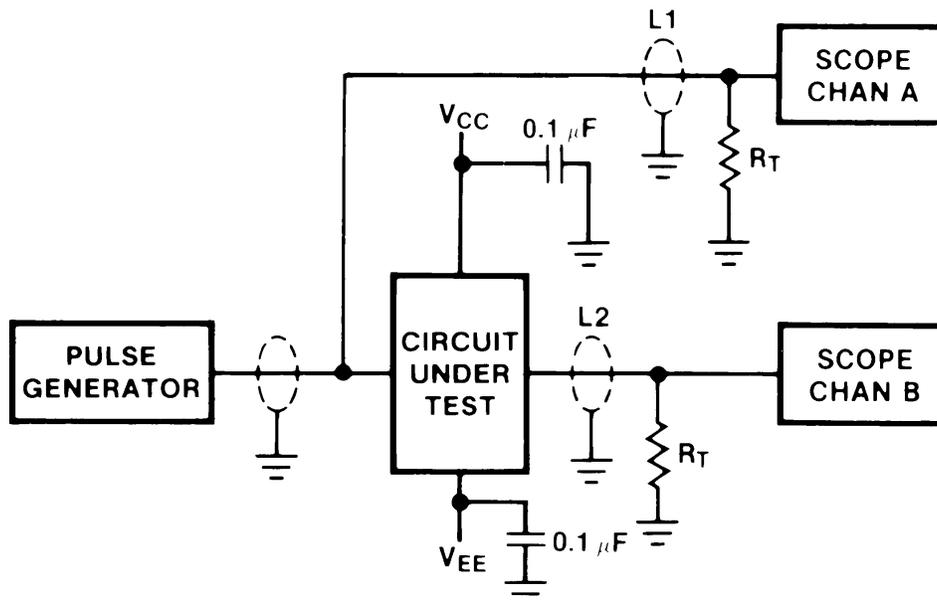
AC ELECTRICAL CHARACTERISTICS

 $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay $D_{na} - D_{ne}$ to O, \bar{O}	0.30	1.90	0.40	1.80	0.30	2.30	ns	See Figure 3 and Figure 4	See (1)(2)(3)
t_{PLH} t_{PHL}	Propagation Delay Data to F	0.80	2.90	0.90	2.80	0.90	3.40	ns		
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.20	1.80	0.30	1.60	0.20	2.00	ns		See (4)

- (1) F100K 300 Series cold temperature testing is performed by temperature soaking (to ensure junction temperature equals $-55^\circ C$), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.
- (2) Screen tested 100% on each device at $+25^\circ C$ temperature only, Subgroup A9.
- (3) Sample tested (Method 5005, Table I) on each mfg. lot at $+25^\circ C$, Subgroup A9, and at $+125^\circ C$ and $-55^\circ C$ temperatures, Subgroups A10 and A11.
- (4) Not tested at $+25^\circ C$, $+125^\circ C$, and $-55^\circ C$ temperature (design characterization data).

TEST CIRCUITRY



$V_{CC}, V_{CCA} = +2V$, $V_{EE} = -2.5V$
 $L1$ and $L2$ = equal length 50Ω impedance lines
 $R_T = 50\Omega$ terminator internal to scope
 Decoupling $0.1 \mu F$ from GND to V_{CC} and V_{EE}
 All unused outputs are loaded with 50Ω to GND
 C_L = Fixture and stray capacitance ≤ 3 pF

Figure 3. AC Test Circuit

Switching Waveforms

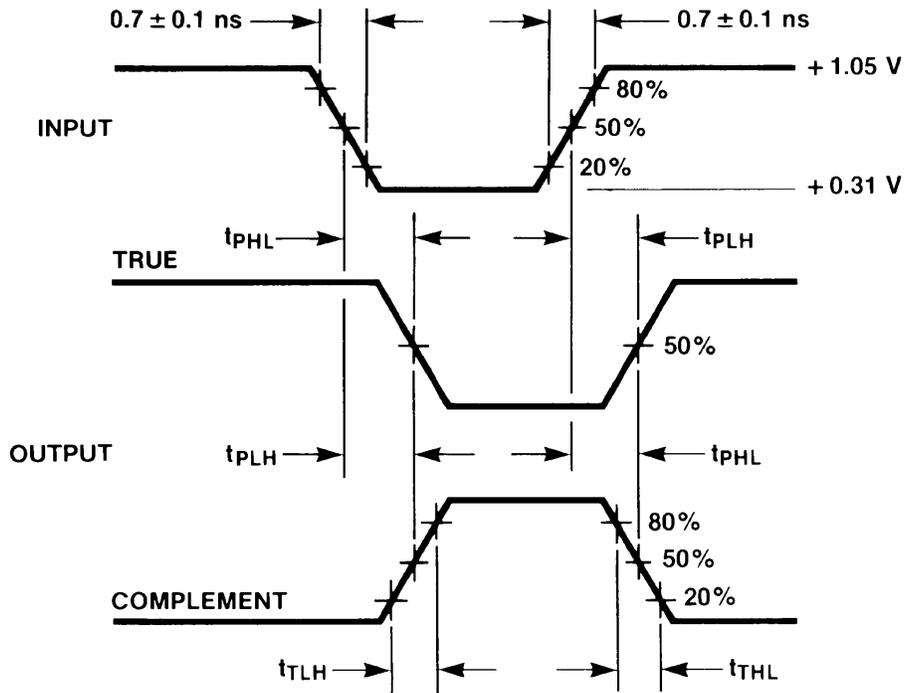


Figure 4. Propagation Delay and Transition Times

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	5

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