

## 100324 Low Power Hex TTL-to-ECL Translator

Check for Samples: [100324](#)

### FEATURES

- Pin/Function Compatible with 100124
- Meets 100124 AC Specifications
- 50% Power Reduction of the 100124
- Differential Outputs
- 2000V ESD Protection
- –4.2V to –5.7V Operating Range
- Standard Microcircuit Drawing
  - (SMD) 5962-9153001

### DESCRIPTION

The 100324 is a hex translator, designed to convert TTL logic levels to 100K ECL logic levels. The inputs are compatible with standard or Schottky TTL. A common Enable (E), when LOW, holds all inverting outputs HIGH and holds all true outputs LOW. The differential outputs allow each circuit to be used as an inverting/non-inverting translator, or as a differential line driver. The output levels are voltage compensated over the full –4.2V to –5.7V range.

When the circuit is used in the differential mode, the 100324, due to its high common mode rejection, overcomes voltage gradients between the TTL and ECL ground systems. The  $V_{EE}$  and  $V_{TTL}$  power may be applied in either order.

The 100324 is pin and function compatible with the 100124 with similar AC performance, but features power dissipation roughly half of the 100124 to ease system cooling requirements.

### Logic Diagram

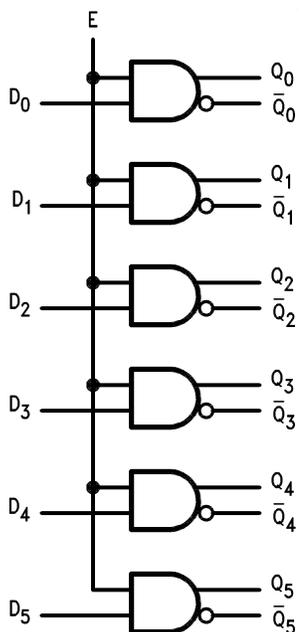


Table 1. Pin Descriptions

Pin Names	Description
$D_0$ – $D_5$	Data Inputs
E	Enable Input
$Q_0$ – $Q_5$	Data Outputs
$\bar{Q}_0$ – $\bar{Q}_5$	Complementary Data Outputs



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## Connection Diagrams

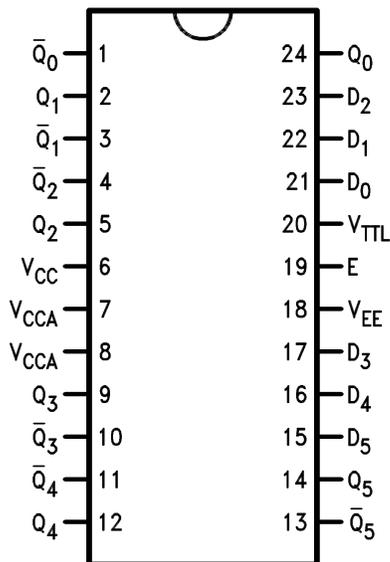


Figure 1. 24-Pin CDIP

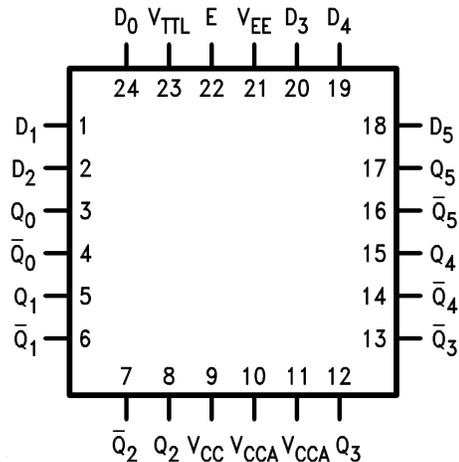


Figure 2. 24-Pin CLGA



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS <sup>(1)(2)</sup>

Above which the useful life may be impaired.

Storage Temperature (T <sub>STG</sub> )		-65°C to +150°C
Maximum Junction Temperature (T <sub>J</sub> )	CDIP/CLGA	+175°C
V <sub>EE</sub> Pin Potential to Ground Pin		-7.0V to +0.5V
V <sub>TTL</sub> Pin Potential to Ground Pin		-0.5V to +6.0V
Input Voltage (DC)		-0.5V to +6.0V
Output Current (DC Output HIGH)		-50 mA
ESD <sup>(3)</sup>		≥2000V

- (1) Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
- (3) ESD testing conforms to MIL-STD-883, Method 3015.

## RECOMMENDED OPERATING CONDITIONS

Case Temperature (T <sub>C</sub> )	Military	-55°C to +125°C
Supply Voltage (V <sub>EE</sub> )		-5.7V to -4.2V

**DC ELECTRICAL CHARACTERISTICS - MILITARY VERSION**
 $V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = -55^\circ C$  to  $+125^\circ C$ ,  $V_{TTL} = +4.5V$  to  $+5.5V$ 

Symbol	Parameter	Min	Max	Units	$T_C$	Conditions	Notes	
$V_{OH}$	Output HIGH Voltage	-1025	-870	mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH}$ (Max) or $V_{IL}$ (Min)	Loading with $50\Omega$ to $-2.0V$	See (1)(2)(3)
		-1085	-870	mV	$-55^\circ C$			
$V_{OL}$	Output LOW Voltage	-1830	-1620	mV	$0^\circ C$ to $+125^\circ C$			
		-1830	-1555	mV	$-55^\circ C$			
$V_{OHC}$	Output HIGH Voltage	-1035		mV	$0^\circ C$ to $+125^\circ C$	$V_{IN} = V_{IH}$ (Max) or $V_{IL}$ (Min)	Loading with $50\Omega$ to $-2.0V$	See (1)(2)(3)
		-1085		mV	$-55^\circ C$			
$V_{OLC}$	Output LOW Voltage		-1610	mV	$0^\circ C$ to $+125^\circ C$			
			-1555	mV	$-55^\circ C$			
$V_{IH}$	Input HIGH Voltage	2.0	5.0	V	$-55^\circ C$ to $+125^\circ C$	Over $V_{TTL}$ , $V_{EE}$ , $T_C$ Range	See (1)(2)(3)(4)	
$V_{IL}$	Input LOW Voltage	0.0	0.8	V	$-55^\circ C$ to $+125^\circ C$	Over $V_{TTL}$ , $V_{EE}$ , $T_C$ Range	See (1)(2)(3)(4)	
$I_{IH}$	Input HIGH Current Breakdown Test		20	$\mu A$	$-55^\circ C$ to $+125^\circ C$	$V_{IN} = +2.7V$	See (1)(2)(3)	
			100	$\mu A$	$-55^\circ C$ to $+125^\circ C$	$V_{IN} = +7.0V$		
$I_{IL}$	Input LOW Current Data Enable	-0.9		mA	$-55^\circ C$ to $+125^\circ C$	$V_{IN} = +0.4V$	See (1)(2)(3)	
		-5.4						
$V_{FCD}$	Input Clamp Diode Voltage		-1.2	V	$-55^\circ C$ to $+125^\circ C$	$I_{IN} = -18$ mA	See (1)(2)(3)	
$I_{EE}$	$V_{EE}$ Power Supply Current	-70	-22	mA	$-55^\circ C$ to $+125^\circ C$	All Inputs $V_{IN} = +4.0V$	See (1)(2)(3)	
$I_{TTL}$	$V_{TTL}$ Power Supply Current		38	mA	$-55^\circ C$ to $+125^\circ C$	All Inputs $V_{IN} = GND$	See (5)(6)(7)	

- (1) F100K 300 Series cold temperature testing is performed by temperature soaking (to ensure junction temperature equals  $-55^\circ C$ ), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.
- (2) Screen tested 100% on each device at  $-55^\circ C$ ,  $+25^\circ C$ , and  $+125^\circ C$ , Subgroups 1, 2, 3, 7, and 8.
- (3) Sample tested (Method 5005, Table I) on each manufactured lot at  $-55^\circ C$ ,  $+25^\circ C$ , and  $+125^\circ C$ , Subgroups A1, 2, 3, 7, and 8.
- (4) Ensured by applying specified input condition and testing  $V_{OH}/V_{OL}$ .
- (5) F100K 300 Series cold temperature testing is performed by temperature soaking (to ensure junction temperature equals  $-55^\circ C$ ), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.
- (6) Screen tested 100% on each device at  $-55^\circ C$ ,  $+25^\circ C$ , and  $+125^\circ C$ , Subgroups 1, 2, 3, 7, and 8.
- (7) Sample tested (Method 5005, Table I) on each manufactured lot at  $-55^\circ C$ ,  $+25^\circ C$ , and  $+125^\circ C$ , Subgroups A1, 2, 3, 7, and 8.

**AC ELECTRICAL CHARACTERISTICS - MILITARY VERSION**
 $V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TTL} = +4.5V$  to  $+5.5V$ 

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
$t_{PLH}$	Propagation Delay	0.50	3.00	0.50	2.90	0.30	3.30	ns	See Figure 3 and Figure 4	See (1)(2)(3)
$t_{PHL}$	Data and Enable to Output									
$t_{TLH}$	Transition Time	0.35	1.80	0.45	1.80	0.45	1.80	ns		See (4)
$t_{THL}$	20% to 80%, 80% to 20%									

- (1) F100K 300 Series cold temperature testing is performed by temperature soaking (to ensure junction temperature equals  $-55^\circ C$ ), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.
- (2) Screen tested 100% on each device at  $+25^\circ C$  temperature only, Subgroup A9.
- (3) Sample tested (Method 5005, Table I) on each manufactured lot at  $+25^\circ C$ , Subgroup A9, and at  $+125^\circ C$  and  $-55^\circ C$  temperatures, Subgroups A10 and A11.
- (4) Not tested at  $+25^\circ C$ ,  $+125^\circ C$ , and  $-55^\circ C$  temperature (design characterization data).

### SWITCHING WAVEFORM

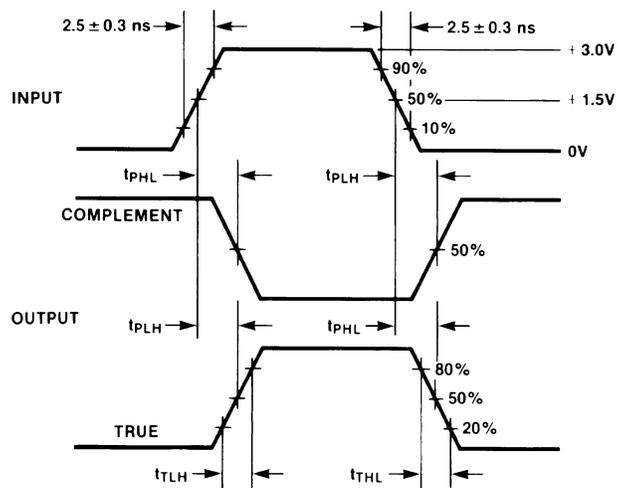
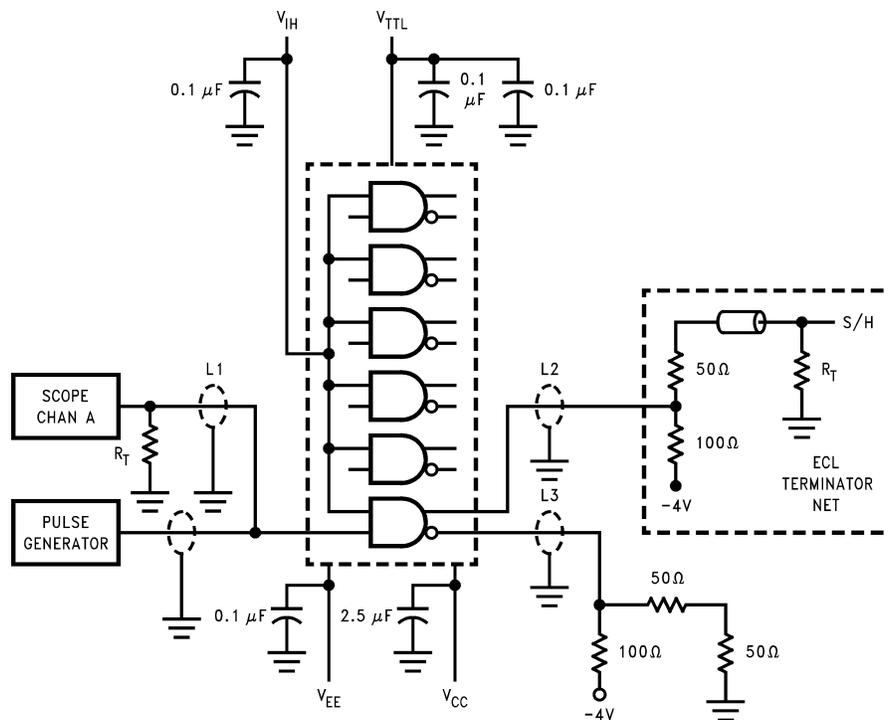


Figure 3. Propagation Delay and Transition Times

### AC Test Circuit



$V_{CC}, V_{CCA} = 0V, V_{EE} = -4.5V, V_{TTL} = +5.0V, V_{IH} = +3.0V$   
 $L1, L2$  and  $L3$  = equal length  $50\Omega$  impedance lines  
 $R_T = 50\Omega$  terminator internal to scope  
 Decoupling  $0.1 \mu F$  from GND to  $V_{CC}, V_{EE}$  and  $V_{TTL}$   
 All unused outputs are loaded with  $50\Omega$  to  $-2V$  or with equivalent ECL terminator network  
 $C_L$  = Fixture and stray capacitance  $\leq 3 pF$

Figure 4.

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**REVISION HISTORY**

<b>Changes from Revision A (April 2013) to Revision B</b>	<b>Page</b>
• Changed layout of National Data Sheet to TI format .....	<a href="#">4</a>

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