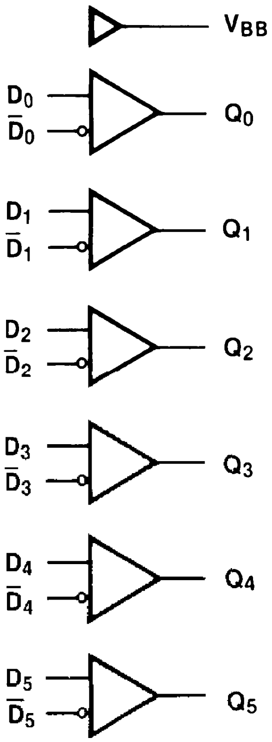
# 100325 Low Power Hex ECL-to-TTL Translator

**Check for Samples:** 100325

## FEATURES

- **Pin/Function Compatible with 100125**
- **Meets 100125 AC Specifications**
- **50% Power Reduction of the 100125**
- **Differential Inputs with Built in Offset**
- **Standard FAST® Outputs**
- **2000V ESD Protection**
- **-4.2V to -5.7V Operating Range**
- **Available to Microcircuit Drawing**
  - **(SMD) 5962-9153101**

### Logic Diagram



## DESCRIPTION

The 100325 is a hex translator for converting F100K logic levels to TTL logic levels. Differential inputs allow each circuit to be used as an inverting, non-inverting or differential receiver. An internal reference voltage generator provides $V_{BB}$ for single-ended operation, or for use in Schmitt trigger applications. All inputs have 50 kO pull-down resistors. When the inputs are either unconnected or at the same potential the outputs will go low.

When used in single-ended operation the apparent input threshold of the true inputs is 20 mV to 40 mV higher (positive) than the threshold of the complementary inputs. The $V_{EE}$ and $V_{TTL}$ power may be applied in either order.

### Pin Descriptions

| Pin Names | Description |
|---|---|
| $D_0$–$D_5$ | Data Inputs |
| $\overline{D_0}$–$\overline{D_5}$ | Inverting Data Inputs |
| $Q_0$–$Q_5$ | Data Outputs |

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## Connection Diagrams

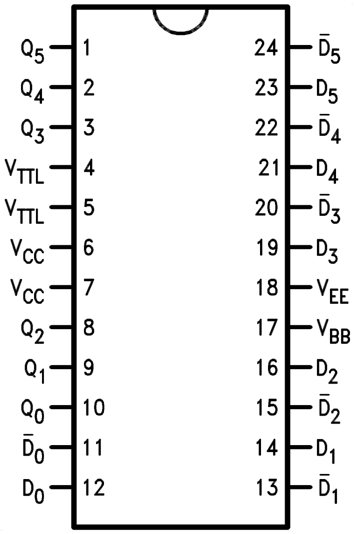


**Figure 1. 24-Pin CERDIP**

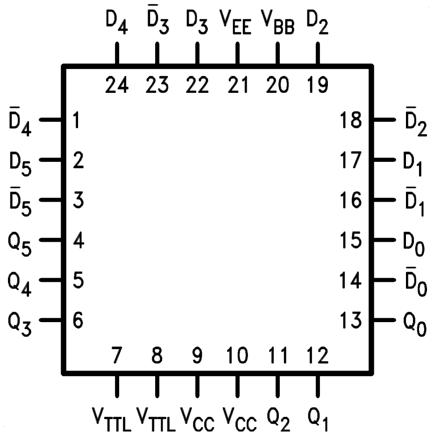


**Figure 2. 24-Pin CPGA**
**See NAQ0024C Package**

### TRUTH TABLE(1)

| Inputs | | Outputs |
|---|---|---|
| $D_n$ | $\overline{D}_n$ | $Q_n$ |
| L | H | L |
| H | L | H |
| L | L | L |
| H | H | L |
| Open | Open | L |
| $V_{EE}$ | $V_{EE}$ | L |
| L | $V_{BB}$ | L |
| H | $V_{BB}$ | H |
| $V_{BB}$ | L | H |
| $V_{BB}$ | H | L |

(1) H = HIGH Voltage Level
L = LOW Voltage Level

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS (1)(2)

Above which the useful life may be impaired.

| | | |
|---|---|---|
| Storage Temperature ($T_{STG}$) | | -65°C to +150°C |
| Maximum Junction Temperature ($T_J$) | Ceramic | +175°C |
| $V_{EE}$ Pin Potential to Ground Pin | | -7.0V to +0.5V |
| $V_{TTL}$ Pin Potential to Ground Pin | | -0.5V to +6.0V |
| Input Voltage (DC) | | $V_{EE}$ to +0.5V |
| Voltage Applied to Output in HIGH State (with $V_{CC}$ = 0V) | | -0.5V to $V_{CC}$ |
| Current Applied to Output in LOW State (Max) | | twice the rated $I_{OL}$ (mA) |
| ESD (3) | | =2000V |

(1) Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) ESD testing conforms to MIL-STD-883, Method 3015.

## RECOMMENDED OPERATING CONDITIONS

| | | |
|---|---|---|
| Case Temperature ($T_C$) | Military | -55°C to +125°C |
| Supply Voltage ($V_{EE}$) | | -5.7V to -4.2V |

## DC ELECTRICAL CHARACTERISTICS - MILITARY VERSION

$V_{EE}$ = -4.2V to -5.7V, $V_{CC}$ = $V_{CCA}$ = GND, $T_C$ = -55°C to +125°C, $C_L$ = 50 pF, $V_{TTL}$ = +4.5V to +5.5V

| Symbol | Parameter | Min | Max | Units | $T_C$ | Conditions | | Notes |
|---|---|---|---|---|---|---|---|---|
| $V_{BB}$ | Output Reference Voltage | -1380 | -1260 | mV | 0°C to +125°C | $I_{VBB}$ = -3 µA, $V_{EE}$ = -4.2V | | See (1)(2)(3) |
| | | | | | | $I_{VBB}$ = -2.1 mA | $V_{EE}$ = -5.7V | |
| | | -1396 | -1260 | | -55°C | $I_{VBB}$ = -3 mA | | |
| $V_{IH}$ | Input HIGH Voltage | -1165 | -870 | mV | -55°C to +125°C | Ensured HIGH Signal for All Inputs (with One Input Tied to $V_{BB}$) | | See (1)(2)(3)(4) |
| $V_{IL}$ | Input LOW Voltage | -1830 | -1475 | mV | -55°C to +125°C | Ensured LOW Signal for All Inputs (with One Input Tied to $V_{BB}$) | | See (1)(2)(3)(4) |
| $V_{OH}$ | Output HIGH Voltage | 2.5 | | mV | 0°C to +125°C | $I_{OH}$ = -2.0 mA | $V_{IN}$ = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$ | See (1)(2)(3) |
| | | 2.4 | | | -55°C | | | |
| $V_{OL}$ | Output LOW Voltage | | 0.5 | mV | -55°C to +125°C | $I_{OL}$ = 20 mA | | |
| $V_{DIFF}$ | Input Voltage Differential | 150 | | mV | -55°C to +125°C | Required for Full Output Swing | | See (1)(2)(3) |
| $V_{CM}$ | Common Mode Voltage | -2000 | -500 | mV | -55°C to +125°C | | | See (1)(2)(3)(4) |
| $I_{IH}$ | Input HIGH Current | | 350 | µA | 0°C to +125°C | $V_{IN}$ = $V_{IH\ (Max)}$, $D_0$–$D_5$ = $V_{BB}$ , $\overline{D}_0$–$\overline{D}_5$ = $V_{IL\ (Min)}$ | | See (1)(2)(3) |
| | | | 500 | | -55°C | | | |
| $I_{IL}$ | Input LOW Current | 0.50 | | µA | -55°C to +125°C | $V_{IN}$ = $V_{IL\ (Min)}$, $D_0$–$D_5$ = $V_{BB}$ | | See (1)(2)(3) |

(1) F100K 300 Series cold temperature testing is performed by temperature soaking (to ensure junction temperature equals -55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides “cold start” specs which can be considered a worst case condition at cold temperatures.
(2) Screen tested 100% on each device at -55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.
(3) Sample tested (Method 5005, Table I) on each manufactured lot at -55°C, + 25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.
(4) Ensured by applying specified input condition and testing $V_{OH}$/$V_{OL}$.

## DC ELECTRICAL CHARACTERISTICS - MILITARY VERSION (continued)

$V_{EE}$ = -4.2V to -5.7V, $V_{CC}$ = $V_{CCA}$ = GND, $T_C$ = -55°C to +125°C, $C_L$ = 50 pF, $V_{TTL}$ = +4.5V to +5.5V

| Symbol | Parameter | Min | Max | Units | $T_C$ | Conditions | Notes |
|---|---|---|---|---|---|---|---|
| $I_{OS}$ | Output Short Circuit Current | -150 | -60 | mA | -55°C to +125°C | $V_{OUT}$ = GND<br>Test One Output at a Time | See [1][2][3] |
| $I_{CEX}$ | Output HIGH Leakage Current | | 250 | µA | -55°C to +125°C | $V_{OUT}$ = 5.5V | See [1][2][3] |
| $I_{EE}$ | $V_{EE}$ Power Supply Current | -35 | -12 | mA | -55°C to +125°C | $D_0$–$D_5$ = $V_{BB}$ | See [1][2][3] |
| $I_{TTL}$ | $V_{TTL}$ Power Supply Current | | 65 | mA | -55°C to +125°C | $D_0$–$D_5$ = $V_{BB}$ | See [1][2][3] |

## AC ELECTRICAL CHARACTERISTICS

$V_{EE}$ = -4.2V to -5.7V, $V_{CC}$ = GND, $V_{TTL}$ = +4.5V to +5.5V

| Symbol | Parameter | $T_C$ = -55°C | | $T_C$ = +25°C | | $T_C$ = +125°C | | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay Data to Output | 1.50 | 5.00 | 1.60 | 4.70 | 1.70 | 5.70 | ns | $C_L$ = 50 pF | See [1][2][3] |

(1) F100K 300 Series cold temperature testing is performed by temperature soaking (to ensure junction temperature equals -55°C), then testing immediately after power-up. This provides “cold start” specs which can be considered a worst case condition at cold temperatures.
(2) Screen tested 100% on each device at +25°C, temperature only, Subgroup A9.
(3) Sample tested (Method 5005, Table I) on each manufactured lot at +25°C, Subgroup A9, and at +125°C and -55°C temperatures, Subgroups A10 and A11.

## SWITCHING WAVEFORM

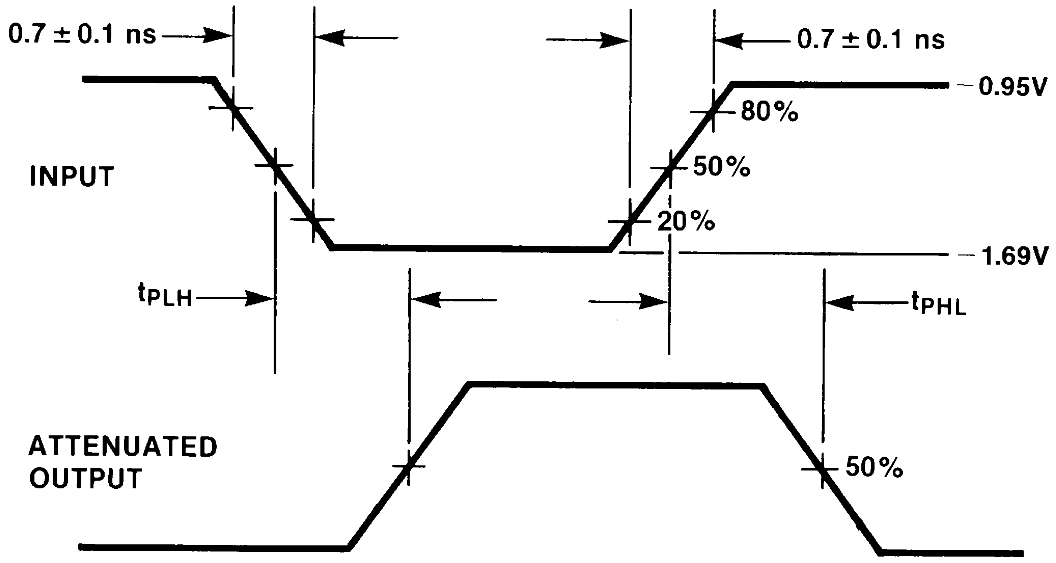
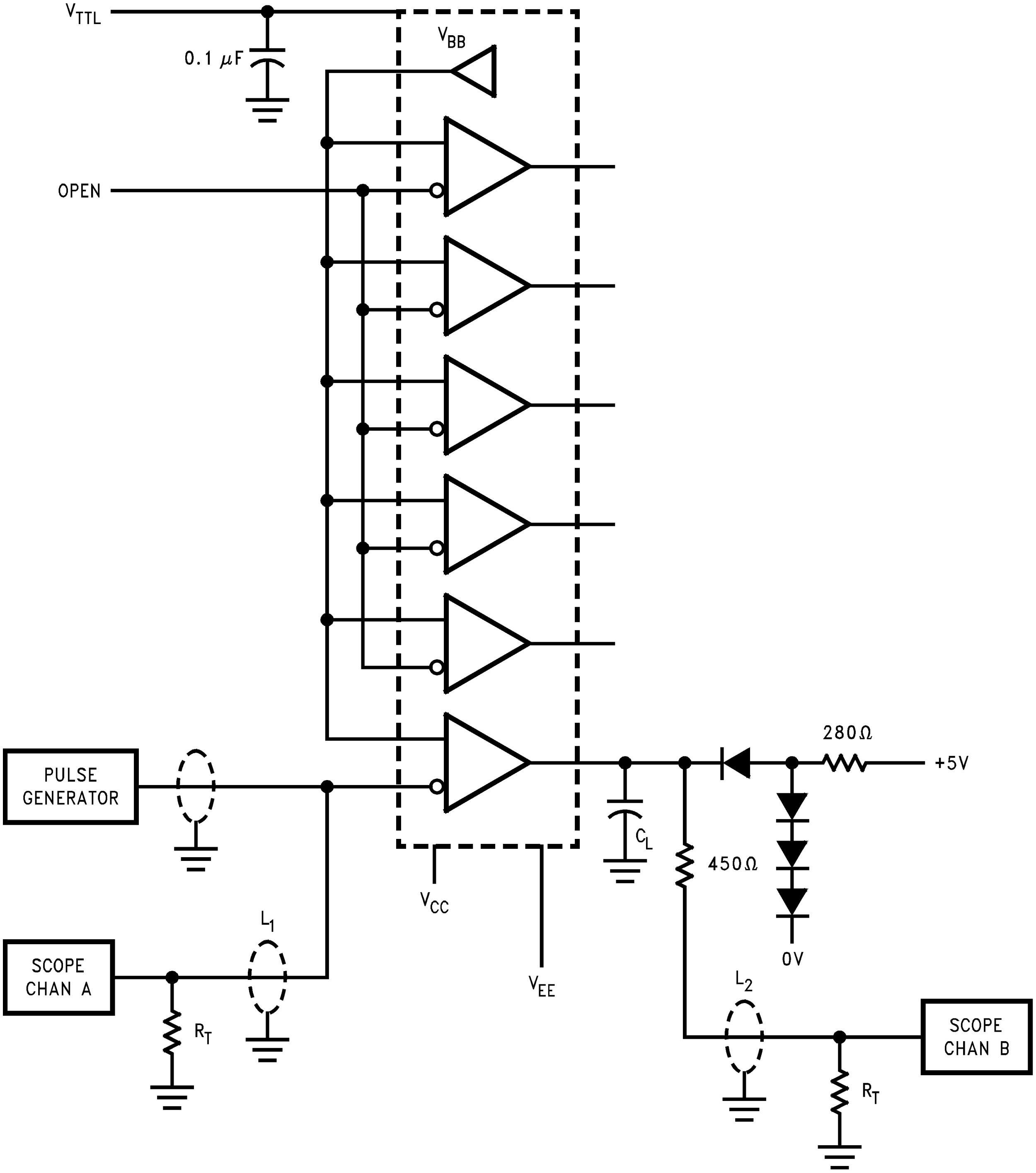


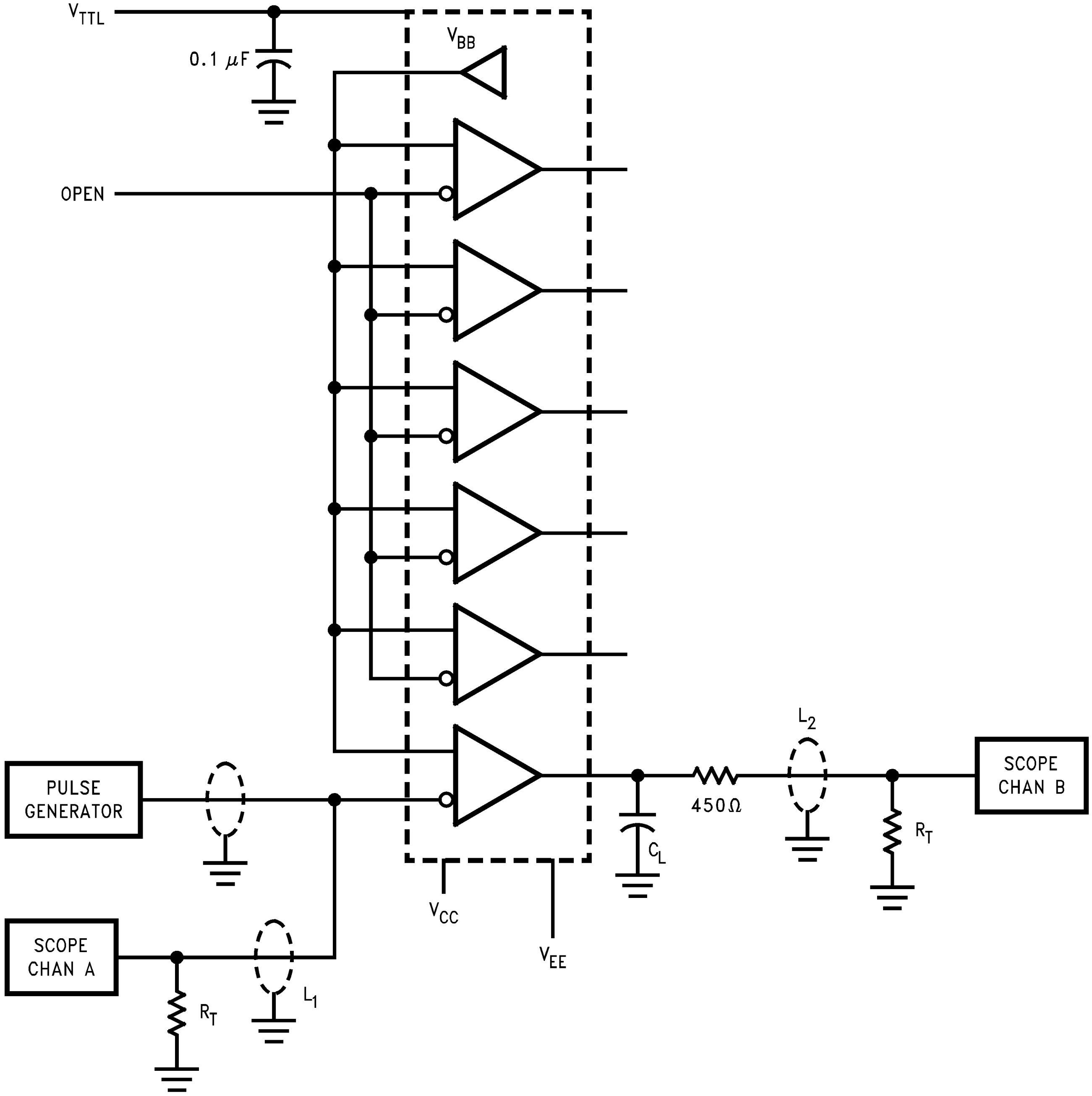
Figure 3. Propagation Delay

## Test Circuits



$V_{CC}$ = 0V, $V_{EE}$ = -4.5V, $V_{TTL}$ = +5V
L1 and L2 = equal length 50O impedance lines
$R_T$ = 50O terminator internal to scope
Decoupling 0.1 µF from GND to $V_{CC}$, $V_{EE}$ and $V_{TTL}$
All unused outputs are loaded with 500O to GND
$C_L$ = Fixture and stray capacitance = 15 pF

**Figure 4. AC Test Circuit for 15 pF Loading**



$V_{CC}$ = 0V, $V_{EE}$ = -4.5V, $V_{TTL}$ = +5V
L1 and L2 = equal length 50O impedance lines
$R_T$ = 50O terminator internal to scope
Decoupling 0.1 µF from GND to $V_{CC}$, $V_{EE}$ and $V_{TTL}$
All unused outputs are loaded with 500O to GND
$C_L$ = Fixture and stray capacitance = 50 pF

**Figure 5. AC Test Circuit for 50 pF Loading**

# REVISION HISTORY

| **Changes from Revision A (April 2013) to Revision B** | **Page** |
|---|---|
| • Changed layout of National Data Sheet to TI format | 6 |

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