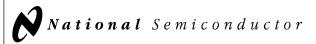
# MM54C922,MM54C923,MM74C922,MM74C923

MM54C922 MM74C922 16-Key Encoder MM54C923 MM74C923 20-Key Encoder



Literature Number: SNOS345A



# MM54C922/MM74C922 16-Key Encoder MM54C923/MM74C923 20-Key Encoder

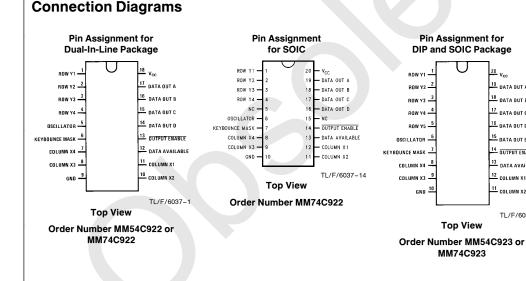
### **General Description**

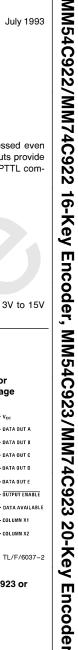
These CMOS key encoders provide all the necessary logic to fully encode an array of SPST switches. The keyboard scan can be implemented by either an external clock or external capacitor. These encoders also have on-chip pullup devices which permit switches with up to 50 k $\Omega$  on resistance to be used. No diodes in the switch array are needed to eliminate ghost switches. The internal debounce circuit needs only a single external capacitor and can be defeated by omitting the capacitor. A Data Available output goes to a high level when a valid keyboard entry has been made. The Data Available output returns to a low level when the entered key is released, even if another key is depressed. The Data Available will return high to indicate acceptance of the new key after a normal debounce period; this two-key rollover is provided between any two switches.

An internal register remembers the last key pressed even after the key is released. The TRI-STATE® outputs provide for easy expansion and bus operation and are LPTTL compatible.

## **Features**

- 50 kΩ maximum switch on resistance
- On or off chip clock
- On-chip row pull-up devices
- 2 key roll-over
- Keybounce elimination with single capacitor
- Last key register at outputs
- TRI-STATE outpust LPTTL compatible
- Wide supply range
- Low power consumption





20 V<sub>cc</sub>

19 DATA OUT A

18 DATA OUT B

17 DATA OUT C

16 DATA OUT D

15 DATA OUT E

12 COLUMN X1

11 COLUMN X2

14 OUTPUT ENABLE

13 DATA AVAILABLE

TL/F/6037-2

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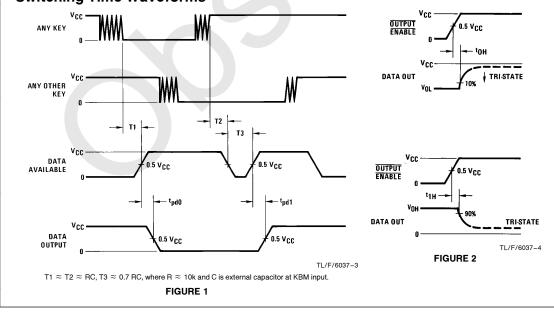
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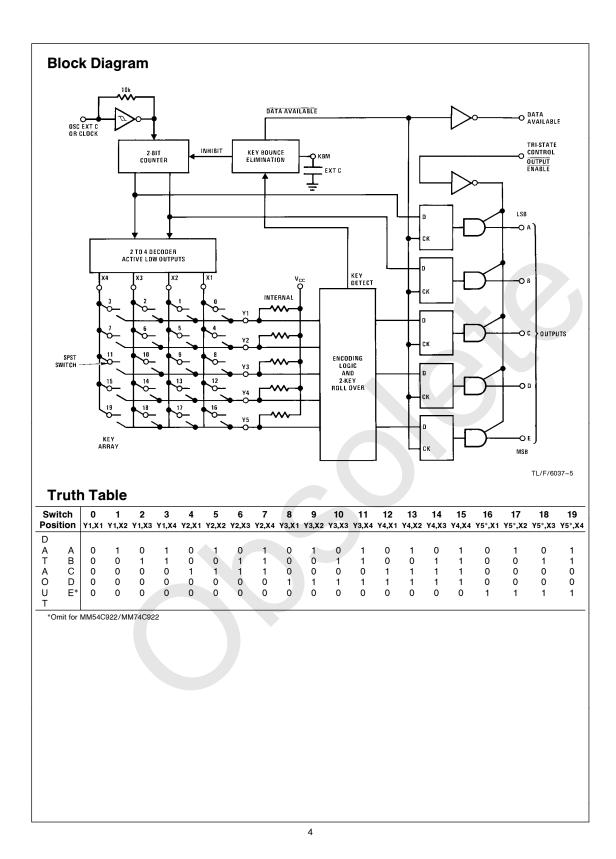
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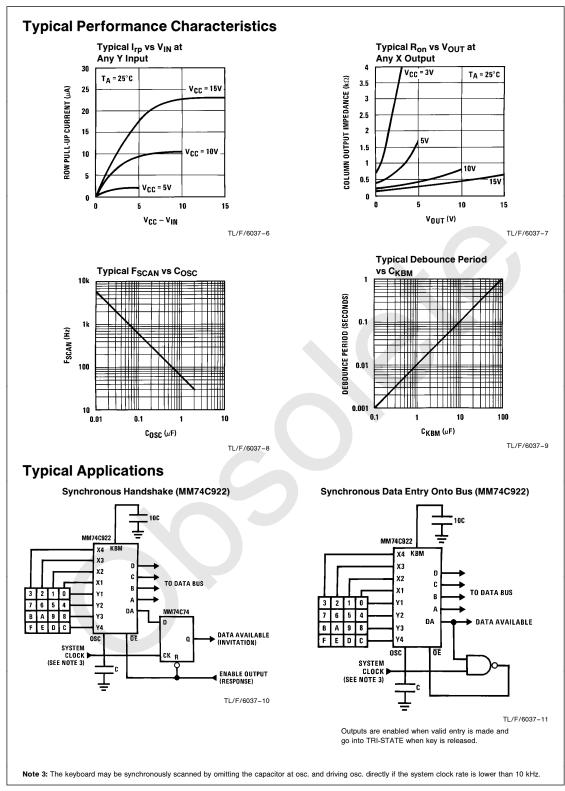
please d	//Aerospace specified devices are contact the National Semiconduct stributors for availability and specifi	or Sales	Storage Temp Power Dissipa Dual-In-Ling		-	-65°C to -	+ 150°C 700 mW	
Voltage at	• •		Small Outli				500 mW	
Operating Temperature Range			Operating V <sub>CC</sub> Range			3V to 15V		
1 0		o +125°C	+125°C V <sub>CC</sub>			18V		
MM74C	922, MM74C923 -40°C	to +85°C						
DC Ele	ectrical Characteristics	Min/Max limits	(Soldering,	10 seconds)	unless otherv	vise specil	260°C fied	
Symbol	Parameter		litions	Min	Тур	Max	Units	
смоѕ то	CMOS							
V <sub>T+</sub>	Positive-Going Threshold Voltage	$V_{CC} = 5V, I_{I}$		3.0	3.6	4.3	V	
	at Osc and KBM Inputs	$V_{\rm CC} = 10V,$	$I_{IN} \ge 1.4 \text{ mA}$	6.0	6.8	8.6	V	
		$V_{\rm CC} = 15V,$	$I_{IN} \ge 2.1 \text{ mA}$	9.0	10	12.9	V	
V <sub>T</sub> -	Negative-Going Threshold Voltage	$V_{CC} = 5V, I_{I}$		0.7	1.4	2.0	V	
	at Osc and KBM Inputs		$I_{IN} \ge 1.4 \text{ mA}$	1.4	3.2	4.0	V	
		$V_{\rm CC} = 15V,$	$I_{IN} \ge 2.1 \text{ mA}$	2.1	5	6.0	V	
V <sub>IN(1)</sub>	Logical "1" Input Voltage,	$V_{CC} = 5V$		3.5	4.5		V	
	Except Osc and KBM Inputs	$V_{\rm CC} = 10V$		8.0	9		V	
		$V_{CC} = 15V$		12.5	13.5		V	
V <sub>IN(0)</sub>	Logical "0" Input Voltage,	$V_{CC} = 5V$			0.5	1.5	V	
	Except Osc and KBM Inputs	$V_{\rm CC} = 10V$			1	2		
		$V_{\rm CC} = 15V$			1.5	2.5	-	
I <sub>rp</sub>	Row Pull-Up Current at Y1, Y2,		$V_{\rm IN} = 0.1  V_{\rm CC}$		-2	-5	μΑ	
	Y3, Y4 and Y5 Inputs	$V_{CC} = 10V$ $V_{CC} = 15V$			-10 -22	-20 -45	μΑ μΑ	
			10. 1	4.5	-22	-45		
V <sub>OUT(1)</sub>	Logical "1" Output Voltage		<sub>O</sub> = −10 μA I <sub>O</sub> = −10 μA	4.5 9				
			$I_0 = -10 \mu A$ $I_0 = -10 \mu A$	9 13.5			V V	
Vaumus	Logical "0" Output Voltage	$V_{\rm CC} = 5V, I_{\rm C}$		10.0		0.5	v	
V <sub>OUT(0)</sub>	Logical o Output Voltage	$V_{CC} = 10V,$				1	l v	
		$V_{\rm CC} = 15V,$				1.5	v v	
Ron	Column "ON" Resistance at	$V_{CC} = 5V, V$			500	1400	Ω	
on	X1, X2, X3 and X4 Outputs	$V_{\rm CC} = 10V,$	•		300	700	Ω	
	· · · · · · · · · · · · · · · · · · ·	$V_{CC} = 15V,$			200	500	Ω	
Icc	Supply Current	$V_{CC} = 5V$			0.55	1.1	mA	
00	Osc at 0V, (one Y low)	$V_{CC} = 10V$			1.1	1.9	mA	
		$V_{CC} = 15V$			1.7	2.6	mA	
l <sub>IN(1)</sub>	Logical "1" Input Current at Output Enable	$V_{CC} = 15V,$	$V_{IN} = 15V$		0.005	1.0	μA	
I <sub>IN(0)</sub>	Logical "0" Input Current at Output Enable	$V_{\rm CC} = 15V,$	$V_{IN} = 0V$	-1.0	-0.005		μΑ	
	TTL INTERFACE			11			L	
	Logical "1" Input Voltage,	54C, V <sub>CC</sub> =	4 5V	V <sub>CC</sub> - 1.5			v	
	Except Osc and KBM Inputs	74C, V <sub>CC</sub> =	4.75V	V <sub>CC</sub> - 1.5 V <sub>CC</sub> - 1.5			V	
V <sub>IN(0)</sub>	Logical "0" Input Voltage, Except Osc and KBM Inputs	54C, V <sub>CC</sub> = 74C, V <sub>CC</sub> =				0.8 0.8	V V	
V <sub>OUT(1)</sub>	Logical "1" Output Voltage	54C, V <sub>CC</sub> =		2.4			v v	
			360 μA				.	
		74C, V <sub>CC</sub> = I <sub>O</sub> = -		2.4			V	
V <sub>OUT(0)</sub>	Logical "0" Output Voltage	54C, V <sub>CC</sub> =	4.5V			0.4	v	
(-)	-	$I_0 = -$	360 μA			0.4	v	
		74C, $V_{CC} = I_0 = -$				0.4	v	

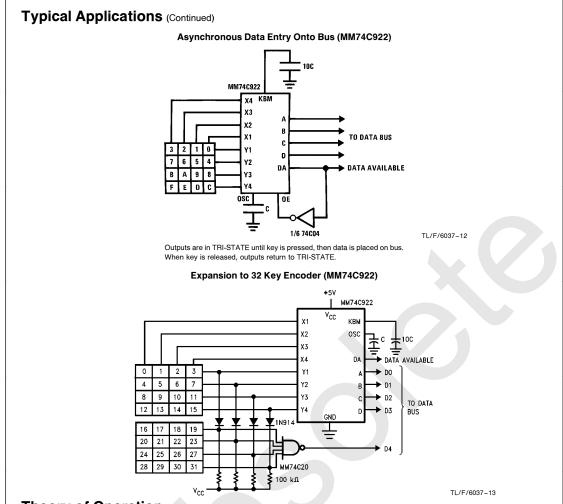
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Symbol	Parameter	Conditions	Min	Ту	/p	Max	Units
OUTPUT D	RIVE (See 54C/74C Family Cha	aracteristics Data Sheet) (Shor	t Circuit Cu	rrent)			
ISOURCE	Output Source Current (P-Channel)	$V_{CC} = 5V, V_{OUT} = 0V,$ $T_A = 25^{\circ}C$	-1.75	-3.3			mA
ISOURCE	Output Source Current (P-Channel)	$V_{CC} = 10V, V_{OUT} = 0V,$ $T_A = 25^{\circ}C$		_	15		mA
I <sub>SINK</sub>	Output Sink Current (N-Channel)	$V_{CC} = 5V, V_{OUT} = V_{CC},$ $T_A = 25^{\circ}C$		3.	.6		mA
I <sub>SINK</sub>	Output Sink Current (N-Channel)	$V_{CC} = 10V, V_{OUT} = V_{CC},$ $T_A = 25^{\circ}C$		1	6		mA
Symbol	Parameter	Conditions		Min	Тур	Max	Unit
		$CS^* T_A = 25^{\circ}C, C_L = 50 \text{ pF, u}$ Conditions $C_1 = 50 \text{ pF} (Figure 1)$	Inless otherv			Max	Unit
	Logical "0" or Logical "1" from D.A.	$V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$			60 35 25	150 80 60	ns ns ns
t <sub>0H</sub> , t <sub>1H</sub>	Propagation Delay Time from Logical "0" or Logical "1" into High Impedance State	$V_{CC} = 5V, R_{L} = 10k$	$V_{CC} = 10V, \bar{C}_{L} = 10  \text{pF}$		80 65 50	200 150 110	ns ns ns
t <sub>HO</sub> , t <sub>H1</sub>	Propagation Delay Time from High Impedance State to a Logical "0" or Logical "1"	$ \begin{array}{c} {\sf R}_L = 10{\sf k}, {\sf C}_L = 50 \; {\sf pF} \; (\textit{Figure 2}) \\ {\sf V}_{CC} = 5{\sf V}, {\sf R}_L = 10{\sf k} \\ {\sf V}_{CC} = 10{\sf V}, {\sf C}_L = 50 \; {\sf pF} \\ {\sf V}_{CC} = 15{\sf V} \end{array} $			100 55 40	250 125 90	ns ns ns
C <sub>IN</sub>	Input Capacitance	Any Input (Note 2)			5	7.5	pF
C <sub>OUT</sub>	TRI-STATE Output Capacitan	ce Any Output (Note 2)			10		pF
Note 1: "Absol they are not m operation.		g. beyond which the safety of the device car operated at these limits. The table of "					









#### Theory of Operation

The MM74C922/MM74C923 Keyboard Encoders implement all the logic necessary to interface a 16 or 20 SPST key switch matrix to a digital system. The encoder will convert a key switch closer to a 4(MM74C922) or 5(MM74C923) bit nibble. The designer can control both the keyboard scan rate and the key debounce period by altering the oscillator capacitor,  $C_{OSE}$ , and the key bounce mask capacitor,  $C_{MSK}$ . Thus, the MM74C922/MM74C923's performance can be optimized for many keyboards.

The keyboard encoders connect to a switch matrix that is 4 rows by 4 columns (MM74C922) or 5 rows by 4 columns (MM74C923). When no keys are depressed, the row inputs are pulled high by internal pull-ups and the column outputs sequentially output a logic "0". These outputs are open drain and are therefore low for 25% of the time and otherwise off. The column scan rate is controlled by the oscillator input, which consists of a Schmitt trigger oscillator, a 2-bit counter, and a 2-4-bit decoder.

When a key is depressed, key 0, for example, nothing will happen when the X1 input is off, since Y1 will remain high. When the X1 column is scanned, X1 goes low and Y1 will go low. This disables the counter and keeps X1 low. Y1 going

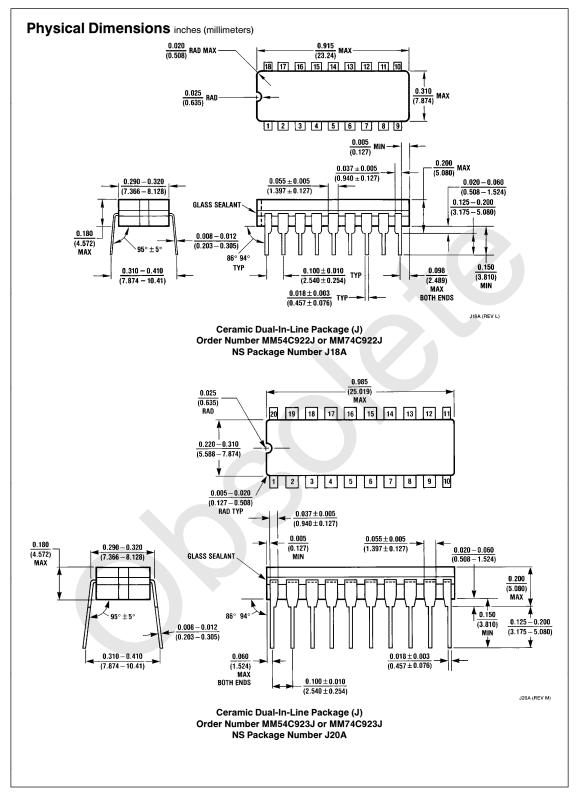
low also initiates the key bounce circuit timing and locks out the other Y inputs. The key code to be output is a combination of the frozen counter value and the decoded Y inputs. Once the key bounce circuit times out, the data is latched, and the Data Available (DAV) output goes high.

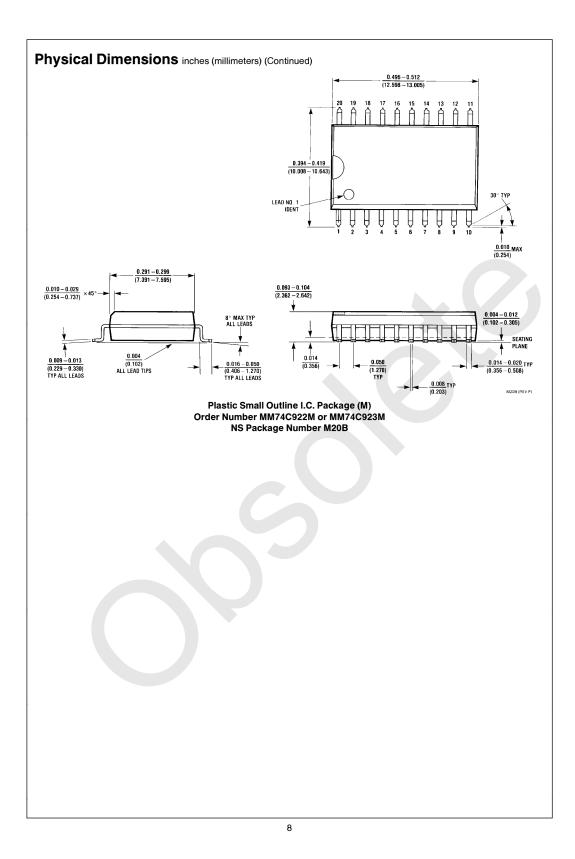
If, during the key closure the switch bounces, Y1 input will go high again, restarting the scan and resetting the key bounce circuitry. The key may bounce several times, but as soon as the switch stays low for a debounce period, the closure is assumed valid and the data is latched.

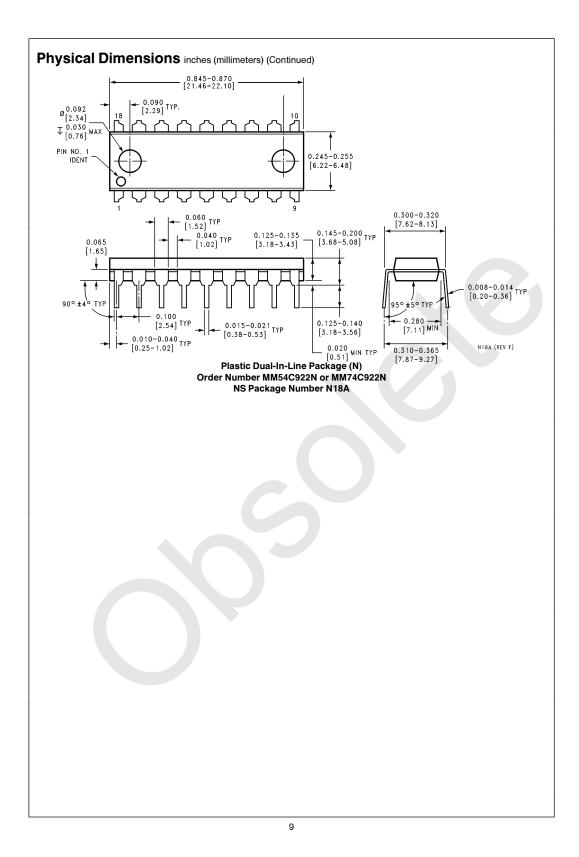
A key may also bounce when it is released. To ensure that the encoder does not recognize this bounce as another key closure, the debounce circuit must time out before another closure is recognized.

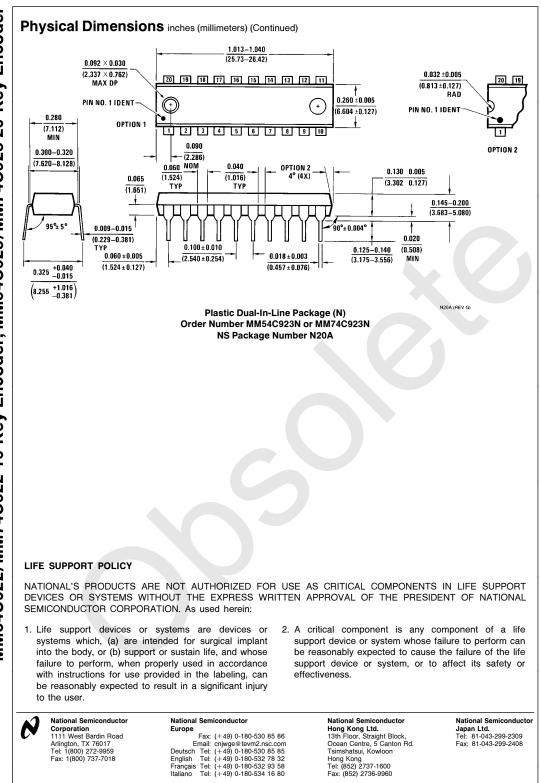
The two-key roll-over feature can be illustrated by assuming a key is depressed, and then a second key is depressed. Since all scanning has stopped, and all other Y inputs are disabled, the second key is not recognized until the first key is lifted and the key bounce circuitry has reset.

The output latches feed TRI-STATE, which is enabled when the Output Enable  $(\overline{\text{OE}})$  input is taken low.









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