

54FCT377

54FCT377 Octal D-Type Flip-Flop with Clock Enable



Literature Number: SNOS423

54FCT377

Octal D-Type Flip-Flop with Clock Enable

General Description

The 'FCT377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable (\overline{CE}) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The \overline{CE} input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

Features

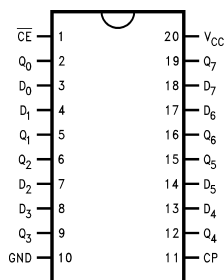
- Clock enable for address and data synchronization applications
- Eight edge-triggered D flip-flops
- Buffered common clock
- See 'FCT273 for master reset version
- See 'FCT373 for transparent latch version
- See 'FCT374 for TRI-STATE® version
- TTL input and output level compatible
- CMOS power consumption
- Output sink capability of 32 mA, source capability of 12 mA
- Standard Microcircuit Drawing (SMD) 5962-8762701

Ordering Code

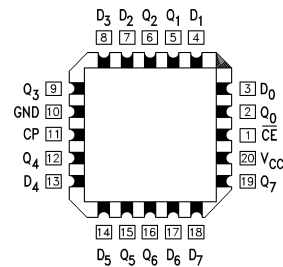
| Military | Package Number | Package Description |
|--------------|----------------|---|
| 54FCT377DMQB | J20A | 20-Lead Ceramic Dual-In-Line |
| 54FCT377FMQB | W20A | 20-Lead Cerpack |
| 54FCT377LMQB | E20A | 20-Lead Ceramic Leadless Chip Carrier, Type C |

Connection Diagram

Pin Assignment for
DIP and Cerpack



Pin Assignment for LCC



| Pin Names | Description |
|--------------------------------|---------------------------|
| D ₀ -D ₇ | Data Inputs |
| \overline{CE} | Clock Enable (Active LOW) |
| CP | Clock Pulse Input |
| Q ₀ -Q ₇ | Data Outputs |

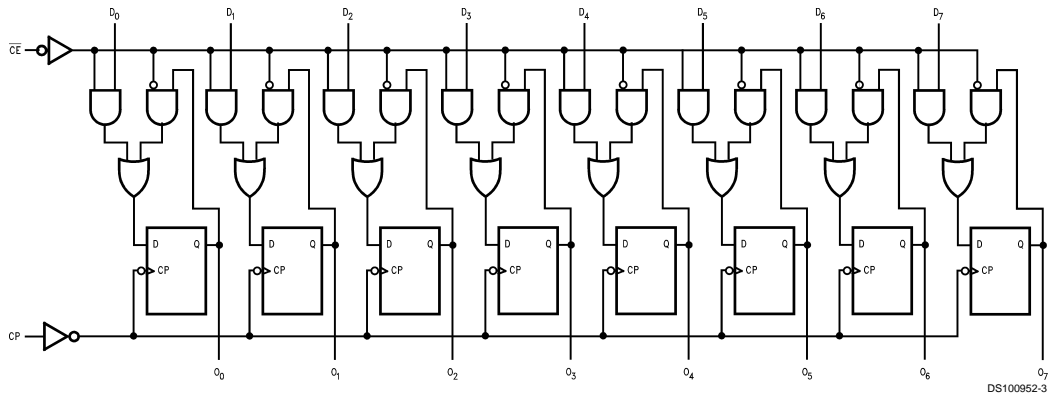
Truth Table

Mode Select-Function Table

| Operating Mode | Inputs | | | Output |
|----------------------|--------|-----------------|-------|-----------|
| | CP | \overline{CE} | D_n | Q_n |
| Load "1" | | l | h | H |
| Load "0" | | l | l | L |
| Hold (Do Nothing) | | h | X | No Change |
| | X | H | X | No Change |

H = HIGH Voltage Level
 h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
 L = LOW Voltage Level
 l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
 X = Immaterial
 = LOW-to-HIGH Clock Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DS100952-3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|--------------------------|
| Storage Temperature | -65°C to +150°C |
| Ambient Temperature under Bias | -55°C to +125°C |
| Junction Temperature under Bias | |
| Ceramic | -55°C to +175°C |
| V _{CC} Pin Potential to Ground Pin | -0.5V to +7.0V |
| Input Voltage (Note 2) | -0.5V to +7.0V |
| Input Current (Note 2) | -30 mA to +5.0 mA |
| Voltage Applied to Any Output in the Disabled or Power-Off State | -0.5V to +4.75V |
| in the HIGH State | -0.5V to V _{CC} |

| | |
|---|--------------------------------------|
| Current Applied to Output in LOW State (Max) | Twice the rated I _{OL} (mA) |
| DC Latchup Source Current (Across Comm Operating Range) | -500 mA |

Recommended Operating Conditions

| | |
|------------------------------|-----------------|
| Free Air Ambient Temperature | |
| Military | -55°C to +125°C |
| Supply Voltage | |
| Military | +4.5V to +5.5V |
| Minimum Input Edge Rate | (ΔV/Δt) |
| Data Input | 50 mV/ns |
| Enable Input | 20 mV/ns |

DC Electrical Characteristics

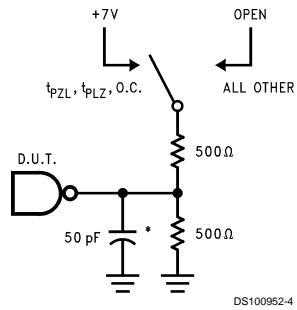
| Symbol | Parameter | FCT377 | | | Units | V _{CC} | Conditions |
|------------------|--------------------------------|--------------|-----|------------|------------|-----------------|---|
| | | Min | Typ | Max | | | |
| V _{IH} | Input HIGH Voltage | 2.0 | | | V | | Recognized HIGH Signal |
| V _{IL} | Input LOW Voltage | | | 0.8 | V | | Recognized LOW Signal |
| V _{CD} | Input Clamp Diode Voltage | | | -1.2 | V | Min | I _{IN} = -18 mA |
| V _{OH} | Output HIGH Voltage | 54FCT 4.3 | | | V | Min | I _{OH} = -300 uA I _{OH} = -12 mA |
| V _{OL} | Output LOW Voltage | 54FCT 2.4 | | 0.2 0.5 | V | Min | I _{OL} = 300 uA I _{OL} = 32mA |
| I _{IH} | Input HIGH Current | | | 5 | μA | Max | V _{IN} = V _{CC} |
| I _{IL} | Input LOW Current | | | -5 | μA | Max | V _{IN} = 0.5V |
| I _{OS} | Output Short-Circuit Current | | | -60 | mA | Max | V _{OUT} = 0.0V |
| I _{CCQ} | Quiescent Power Supply Current | | | 1.5 | mA | Max | V _I = 0.2V or V _I = 5.3V, V _{CC} = 5.5V |
| ΔI _{CC} | Maximum I _{CC} /Input | | | 2.0 | mA | Max | V _I = V _{CC} - 2.1V Data Input V _I = V _{CC} - 2.1V All Others at V _{CC} or GND |
| I _{CCD} | Dynamic I _{CC} | | | 0.4 | mA/ MHz | Max | Outputs Open One bit Toggling, 50% Duty Cycle |
| I _{CC} | Total Power Supply Current | | | 6.0 | mA | Max | V _{CC} = 5.5V, Outputs Open, f _{CP} = 10MHz, 50% Duty Cycle, One bit Toggling at f _I = 5 MHz, 50% Duty Cycle |

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

| AC Electrical Characteristics | | | | | |
|---|------------------------------|--|-------|--|----------|
| Symbol | Parameter | 54FCT | | Units | Fig. No. |
| | | $T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 50\text{ pF}$ | | | |
| | | Min | Max | | |
| t_{PLH} | Propagation Delay | 2.0 | 15.0 | ns | Figure 4 |
| t_{PHL} | CP to O_n | 2.0 | 8.3 | | |
| AC Operating Requirements | | | | | |
| Symbol | Parameter | 54FCT | | Units | Fig. No. |
| | | $T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 50\text{ pF}$ | | | |
| | | Min | Max | | |
| $t_s(H)$ | Setup Time, HIGH | 4.0 | | ns | Figure 6 |
| $t_s(L)$ | or LOW D_n to CP | 4.0 | | | |
| $t_h(H)$ | Hold Time, HIGH | 2.5 | | ns | Figure 6 |
| $t_h(L)$ | or LOW D_n to CP | 2.5 | | | |
| $t_s(H)$ | Setup Time, HIGH | 4.5 | | ns | Figure 6 |
| $t_s(L)$ | or LOW \overline{CE} to CP | 4.5 | | | |
| $t_h(H)$ | Hold Time, HIGH | 2.0 | | ns | Figure 6 |
| $t_h(L)$ | or LOW \overline{CE} to CP | 2.0 | | | |
| $t_w(H)$ | Pulse Width, CP, | 7.0 | | ns | Figure 5 |
| $t_w(L)$ | HIGH or LOW | 7.0 | | | |
| Capacitance | | | | | |
| Symbol | Parameter | Max | Units | Conditions | |
| C_{IN} | Input Capacitance | 10 | pF | $V_{CC} = 0\text{V}, T_A = 25^\circ\text{C}$ | |
| C_{OUT} (Note 3) | Output Capacitance | 12 | pF | $V_{CC} = 5.0\text{V}$ | |
| Note 3: C_{OUT} is measured at frequency $f = 1\text{ MHz}$, per MIL-STD-883B, Method 3012. | | | | | |

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

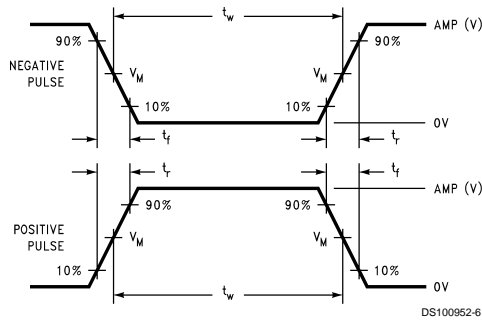


FIGURE 2. $V_M = 1.5V$

Input Pulse Requirements

| Amplitude | Rep. Rate | t_w | t_r | t_f |
|-----------|-----------|--------|--------|--------|
| 3.0V | 1 MHz | 500 ns | 2.5 ns | 2.5 ns |

FIGURE 3. Test Input Signal Requirements

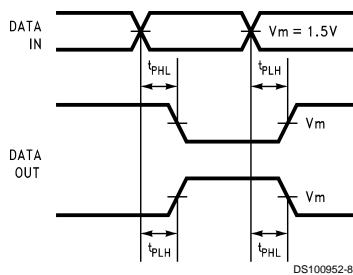


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

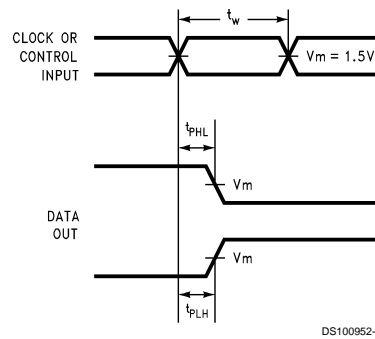


FIGURE 5. Propagation Delay, Pulse Width Waveforms

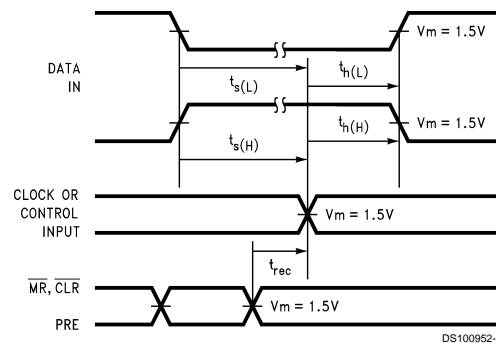
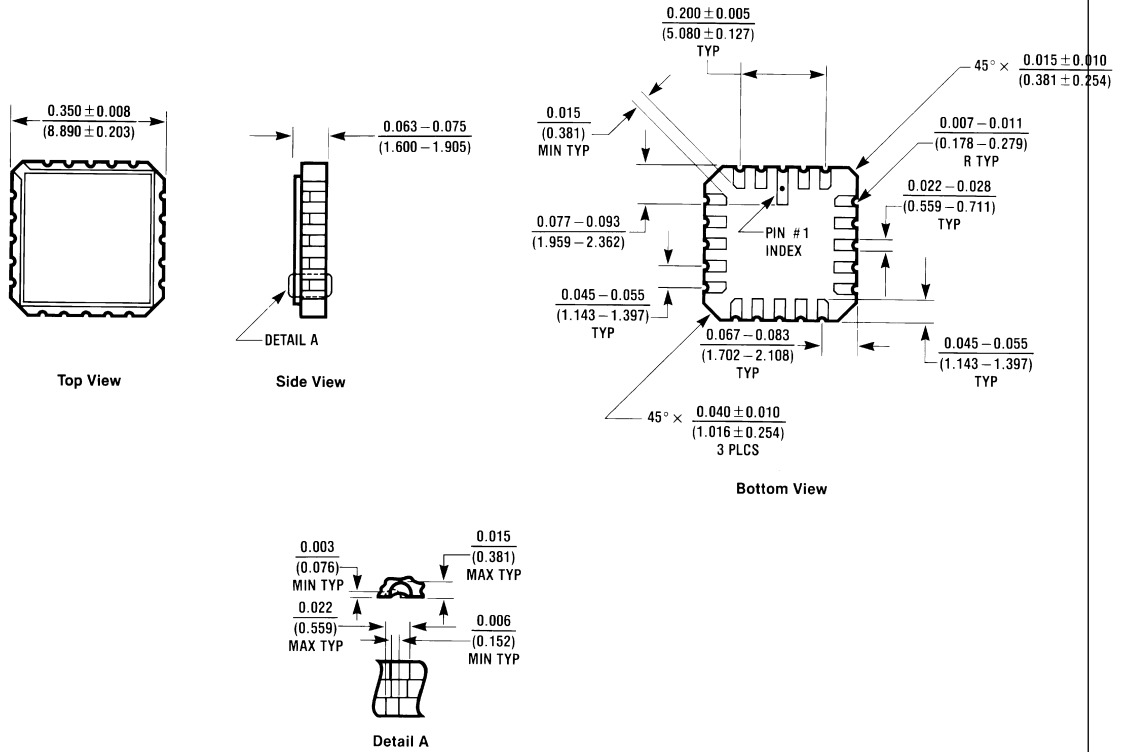


FIGURE 6. Setup Time, Hold Time and Recovery Time Waveforms

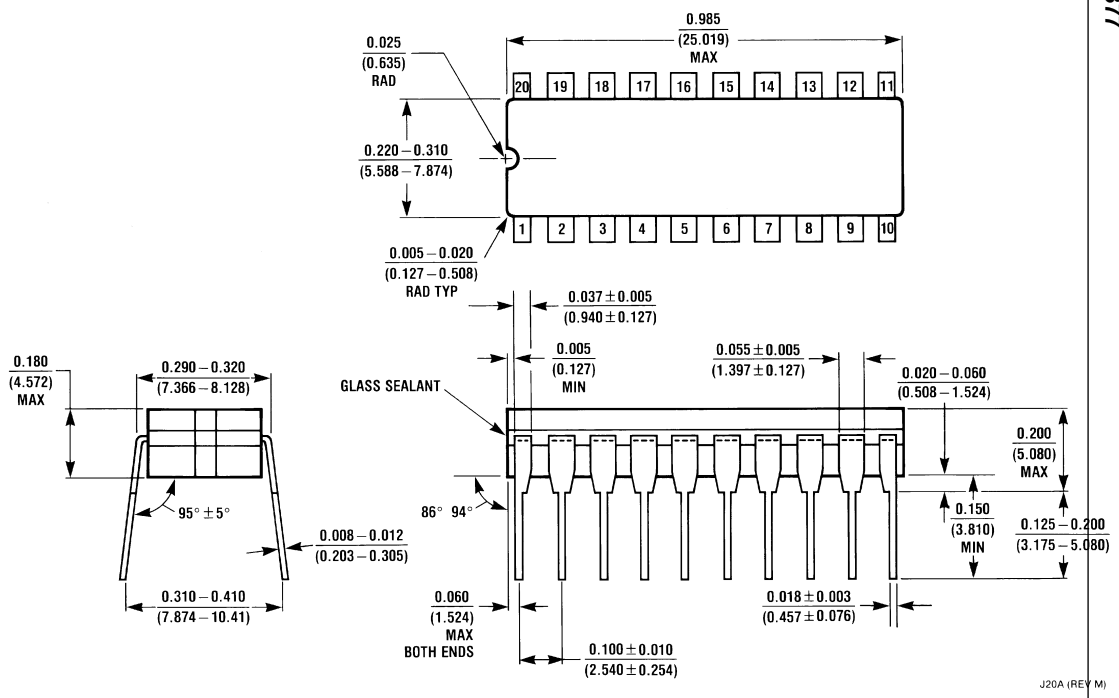
Physical Dimensions inches (millimeters) unless otherwise noted



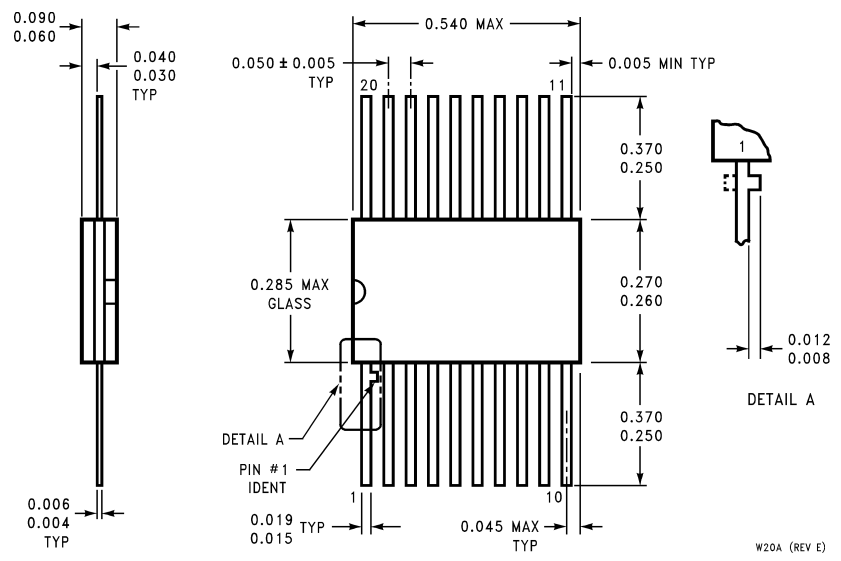
**20-Lead Ceramic Chip Carrier
NS Package Number E20A**

E20A (REV D)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Ceramic Dual-In-Line Package
NS Package Number J20A



20-Lead Ceramic Flatpack
NS Package Number W20A

Notes

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