

100371

100371 Low Power Triple 4-Input Multiplexer with Enable



Literature Number: SNOS433

100371 Low Power Triple 4-Input Multiplexer with Enable

General Description

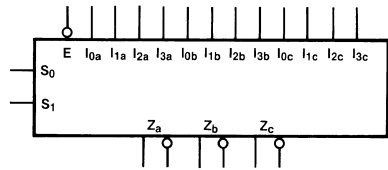
The 100371 contains three 4-input multiplexers which share a common decoder (inputs S_0 and S_1). Output buffer gates provide true and complement outputs. A HIGH on the Enable input (\bar{E}) forces all true outputs LOW (see Truth Table). All inputs have 50 k Ω pull-down resistors.

- 2000V ESD protection
- Pin/function compatible with 100171
- Voltage compensated operating range = -4.2V to -5.7V
- Available to MIL-STD-883

Features

- 35% power reduction of the 100171

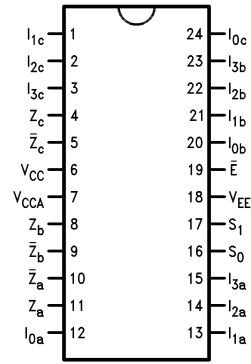
Logic Symbol



Pin Names	Description
$I_{0x}-I_{3x}$	Data Inputs
S_0, S_1	Select Inputs
\bar{E}	Enable Input (Active LOW)
Z_a-Z_c	Data Outputs
$\bar{Z}_a-\bar{Z}_c$	Complementary Data Outputs

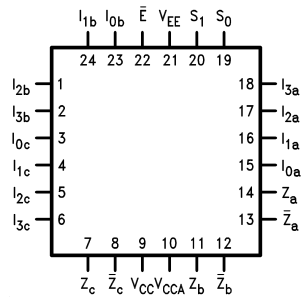
Connection Diagrams

24-Pin DIP



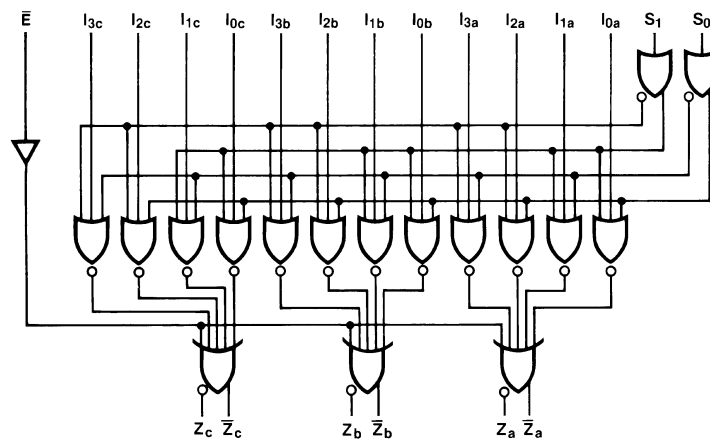
DS100975-2

24-Pin Quad Cerpak



DS100975-3

Logic Diagram



DS100975-5

Truth Table

Inputs			Outputs
\bar{E}	S_0	S_1	Z_n
L	L	L	I_{0x}
L	H	L	I_{1x}
L	L	H	I_{2x}
L	H	H	I_{3x}
H	X	X	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	-65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
V_{EE} Pin Potential to Ground Pin	-7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output current (DC Output HIGH)	-50 mA
ESD (Note 2)	≥2000V

Military Version DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55^\circ C$ to $+125^\circ C$

Recommended Operating Conditions

Case Temperature (T_C)	
Military	-55°C to +125°C
Supply Voltage (V_{EE})	-5.7V to -4.2V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Symbol	Parameter	Min	Max	Units	T_C	Conditions	Notes	
V_{OH}	Output HIGH Voltage	-1025	-870	mV	0°C to +125°C	$V_{IN} = V$ (Max) or V_{IL} (Min)	Loading with 50Ω to -2.0V	(Notes 3, 4, 5)
		-1085	-870	mV	-55°C			
V_{OL}	Output LOW Voltage	-1830	-1620	mV	0°C to +125°C			
		-1830	-1555	mV	-55°C			
V_{OHC}	Output HIGH Voltage	-1035		mV	0°C to +125°C	$V_{IN} = V_{IH}$ (Min) or V_{IL} (Max)	Loading with 50Ω to -2.0V	(Notes 3, 4, 5)
		-1085		mV	-55°C			
V_{OLC}	Output LOW Voltage		-1610	mV	0°C to +125°C			
			-1555	mV	-55°C			
V_{IH}	Input HIGH Voltage	-1165	-870	mV	-55°C to +125°C	Guaranteed HIGH Signal for All Inputs	(Notes 3, 4, 5, 6)	
V_{IL}	Input LOW Voltage	-1830	-1475	mV	-55°C to +125°C	Guaranteed LOW Signal for All Inputs	(Notes 3, 4, 5, 6)	
I_{IL}	Input LOW Current	0.50		μA	-55°C to +125°C	$V_{EE} = -4.2V$ $V_{IN} = V_{IL}$ (Min)	(Notes 3, 4, 5)	
I_{IH}	Input HIGH Current $I_{0X}-I_{3X}$ S_0, S_1, \bar{E}		340	μA	0°C to +125°C	$V_{EE} = -5.7V$ $V_{IN} = V_{IH}$ (Max)	(Notes 3, 4, 5)	
			490	μA	-55°C			
I_{EE}	Power Supply Current	-80	-30	mA	-55°C to +125°C	Inputs Open	(Notes 3, 4, 5)	

Note 3: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals -55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 4: Screen tested 100% on each device at -55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 5: Sample tested (Method 5005, Table I) on each manufactured lot at -55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 6: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

Military Version AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH}	Propagation Delay	0.10	1.90	0.20	1.70	0.20	2.00	ns	Figures 1, 2	(Notes 7, 8, 9, 11)
t_{PHL}	$I_{0x}-I_{3x}$ to Output									
t_{PLH}	Propagation Delay	0.40	2.70	0.60	2.40	0.50	2.90	ns		
t_{PHL}	S_0, S_1 to Output									
t_{PLH}	Propagation Delay	0.50	2.70	0.60	2.40	0.50	2.90	ns		
t_{PHL}	\bar{E} to Output									
t_{TLH}	Transition Time	0.20	1.60	0.30	1.50	0.20	1.60	ns		(Note 10)
t_{THL}	20% to 80%, 80% to 20%									

Note 7: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

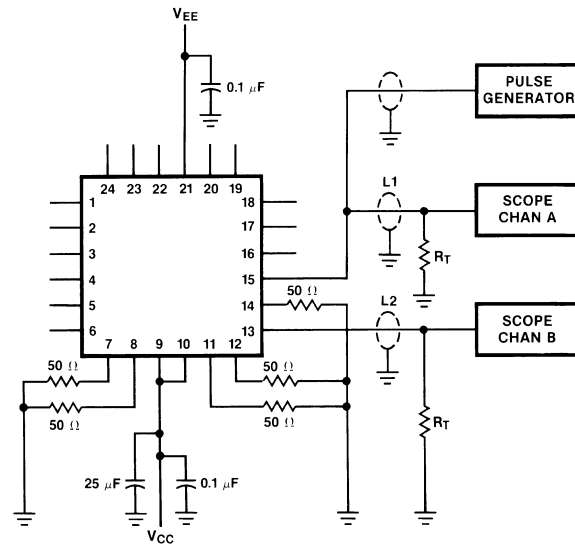
Note 8: Screen tested 100% on each device at $+25^\circ C$ temperature only, Subgroup A9.

Note 9: Sample tested (Method 5005, Table I) on each mfg. lot at $+25^\circ C$, Subgroup A9, and at $+125^\circ C$ and $-55^\circ C$ temperatures, Subgroups A10 and A11.

Note 10: Not tested at $+25^\circ C$, $+125^\circ C$ and $-55^\circ C$ temperature (design characterization data).

Note 11: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Test Circuitry



DS100975-6

Notes:

$V_{CC}, V_{CCA} = +2V$, $V_{EE} = -2.5V$

L1 and L2 = equal length 50Ω impedance lines

$R_T = 50\Omega$ terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

$C_L =$ Fixture and stray capacitance ≤ 3 pF

Pin numbers shown are for flatpak; for DIP see logic symbol

FIGURE 1. AC Test Circuit

Switching Waveforms

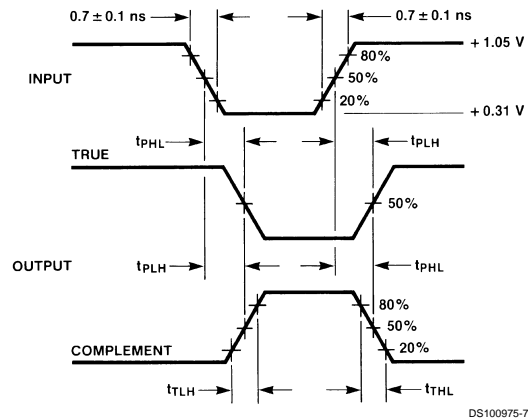


FIGURE 2. Propagation Delay and Transition Times

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