54LCX16373

54LCX16373 Low Voltage 16-Bit Transparent Latch with 5V Tolerant Inputs and Outputs

Literature Number: SNOS490A

National Semiconductor

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54LCX16373
Low Voltage 16-Bit Transparent Latch with 5V Tolerant Inputs and Outputs

General Description

The LCX16373 contains sixteen non-inverting latches with TRI-STATE® outputs and is intended for bus oriented applications. The device is byte controlled. The flip-flops appear transparent to the data when the Latch Enable (LE) is HIGH. When LE is low, the data that meets the setup time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When OE is HIGH, the outputs are in TRI-STATE.

The LCX16373 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX16373 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

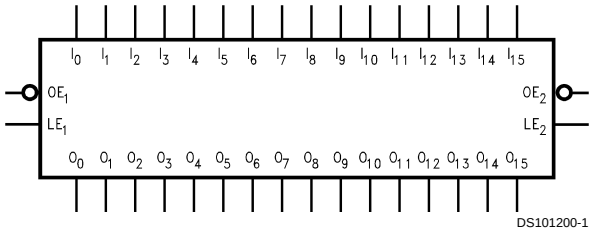
Features

- 5V tolerant inputs and outputs
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V_{CC} supply operation
- ±24 mA output drive
- Implements patented noise/EMI reduction circuitry
- Functionally compatible with the 54 series 16373
- ESD performance:
  Human body model > 2000V
  Machine model > 200V
- Standard Microcircuit Drawing (SMD) 5962-9953401

Ordering Code

Order Number	Package Number	Package Description
54LCX16373W-QML	WA48A	48-Lead Ceramic Flatpack

Logic Symbol



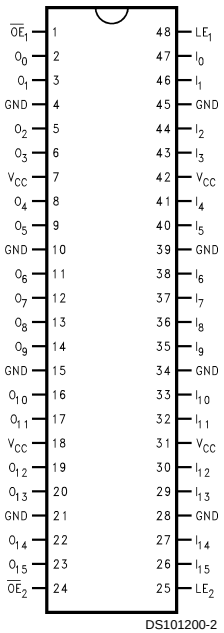
DS101200-1

Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
LE_n	Latch Enable Input
I_0–I_{15}	Inputs
O_0–O_{15}	Outputs

Connection Diagram

Pin Assignment for Cerpack



DS101200-2

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Functional Description

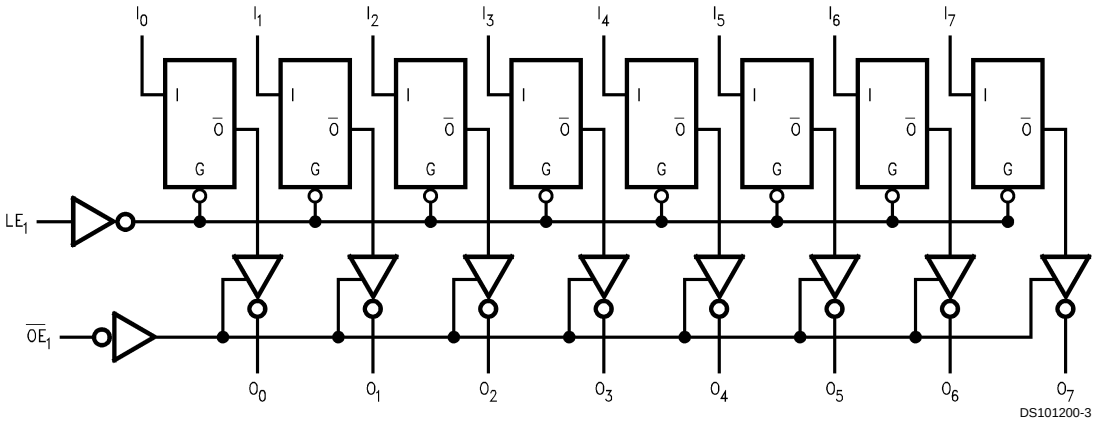
The LCX16373 contains sixteen D-type latches with TRI-STATE standard outputs. The device is byte controlled with each byte functioning identically, but independent of the other. Control pins can be shorted together to obtain full 16-bit operation. The following description applies to each byte. When the Latch Enable (LE_n) input is HIGH, data on the I_n enters the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its I input changes. When LE_n is LOW, the latches store information that was present on the I inputs a setup time preceding the HIGH-to-LOW transition of LE_n. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{OE}_n$) input. When $\overline{OE}_n$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}_n$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

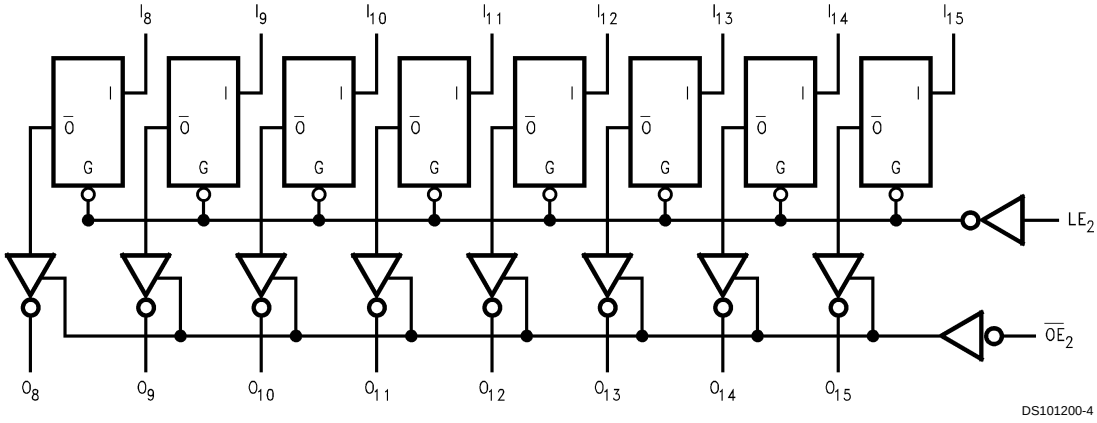
Inputs			Outputs
LE_1	$\overline{OE}_1$	I_0–I_7	O_0–O_7
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

Inputs			Outputs
LE_2	$\overline{OE}_2$	I_8–I_{15}	O_8–O_{15}
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance
O_0 = Previous O_0 before HIGH to LOW transition of Latch Enable

Logic Diagrams





Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_I)	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I < GND	−50 mA
DC Output Diode Current (I_{OK})	
V_O < GND	−50mA
$V_O \geq V_{CC}$	+50mA
DC Output Voltage (V_O) (Note 2)	
Output in High or Low State	-0.5V to V_{CC} + 0.5V
Output in TRI-STATE	-0.5V to 7.0V
DC Output Source or Sink Current (I_O)	±50mA
DC V_{CC} or Ground Current	±400mA
Storage Temperature Range (T_{STG})	−65˚C to +150˚C
Power Dissapation	750mW
Junction Temperature (T_J)	175˚C

Recommended Operating Conditions (Note 3)

Supply Voltage (V_{CC})	
Operating	2.7V to 3.6V
Data Retention	1.5V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	
High or Low State	0V to V_{CC}
TRI-STATE	0V to 5.5V
Operating Temperature (T_A)	−55˚C to +125˚C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
V_{IN} from 0.8V to 2.0V, V_{CC} = 3.0V	0ns/V to 10ns/V

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Note 3: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −55˚C to +125˚C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.7–3.6	2.0		V
V_{IL}	LOW Level Input Voltage		2.7–3.6		0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 µA	2.7–3.6	V_{CC} − 0.2		V
		I_{OH} = −12 mA	2.7	2.2		V
		I_{OH} = −12 mA	3.0	2.4		V
		I_{OH} = −24 mA	3.0	2.2		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 µA	2.7–3.6		0.2	V
		I_{OL} = 12 mA	2.7		0.4	V
		I_{OL} = 24 mA	3.0		0.55	V
I_I	Input Leakage Current	$0 \leq V_I \leq 5.5V$	2.7–3.6		±5.0	µA
I_{OZ}	TRI-STATE Output Leakage	$0 \leq V_O \leq 5.5V$ $V_I = V_{IH}$ or V_{IL}	2.7–3.6		±5.0	µA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	µA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.7–3.6		20	µA
		$3.6V \leq V_I, V_O \leq 5.5V$	2.7–3.6		±20	µA
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC}$ −0.6V	2.7–3.6		500	µA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -55^\circ C$ to $+125^\circ C$, $C_L = 50pF$, $R_L = 500\Omega$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PHL}	Propagation Delay	1.0	6.0	1.5	6.5	ns
t_{PLH}	I_n to O_n	1.0	6.0	1.5	6.5	
t_{PHL}	Propagation Delay	1.0	6.5	1.5	7.0	ns
t_{PLH}	LE to O_n	1.0	6.5	1.5	7.0	
t_{PZL}	Output Enable Time	1.0	6.5	1.5	7.0	ns
t_{PZH}		1.0	6.5	1.5	7.0	
t_{PLZ}	Output Disable Time	1.0	6.5	1.5	7.0	ns
t_{PHZ}		1.0	6.5	1.5	7.0	
t_S	Setup Time, I_n to LE	2.5		2.5		ns
t_H	Hold Time, I_n to LE	2.0		2.0		ns
t_W	LE Pulse Width	3.5		3.5		ns
t_{OSHL}	Output to Output Skew (Note 4)		1.0		1.0	ns
t_{OSLH}			1.0		1.0	

Note 4: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

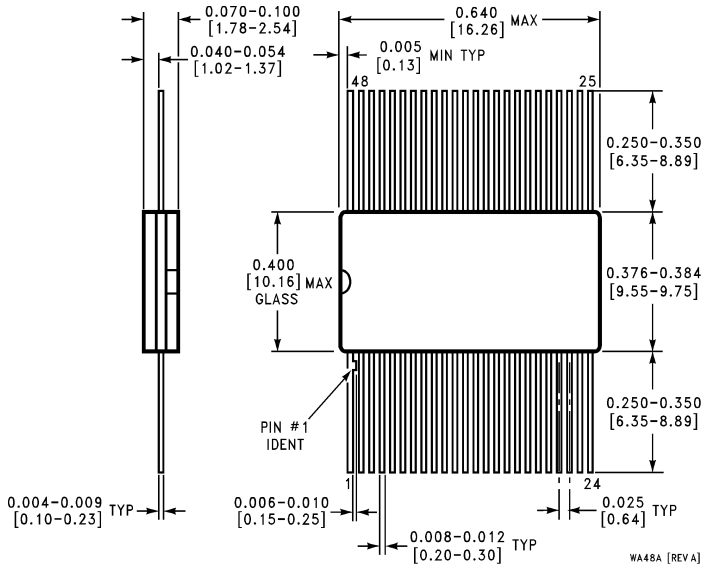
Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25^\circ C$	Units
				Max	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	1.2	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	-1.1	V

Capacitance

Symbol	Parameter	Conditions	Max	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	10	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	12	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, f = 10 MHz	40	pF

Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead Ceramic Flatpack
Package Number WA48A

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