# LP2985LV-N Micropower 150 mA Low-Noise Low-Dropout Regulator in SOT-23 and DSBGA packages for Applications with Output Voltages ≤ 2.0V

## *Designed for Use with Very Low ESR Output Capacitors*

**Check for Samples: LP2985LV-N**

## FEATURES

- **Ensured 150 mA Output Current**
- **Smallest Possible Size (DSBGA)**
- **Requires Minimum External Components**
- **Stable With Low-ESR Output Capacitor**
- **<1 µA Quiescent Current When Shut Down**
- **Low Ground Pin Current at all Loads**
- **Output Voltage Accuracy 1% (A Grade)**
- **High Peak Current Capability**
- **Wide Supply Voltage Range (16V Max)**
- **Low $Z_{OUT}$: 0.3Ω Typical (10 Hz to 1 MHz)**
- **Overtemperature/Overcurrent Protection**
- **−40°C to +125°C Junction Temperature Range**
- **Custom Voltages Available**

## APPLICATIONS

- **Cellular Phone**
- **Palmtop/Laptop Computer**
- **Personal Digital Assistant (PDA)**
- **Camcorder, Personal Stereo, Camera**

## DESCRIPTION

The LP2985LV-N is a 150 mA, fixed-output voltage regulator designed to provide high performance and low noise in applications requiring output voltages ≤ 2.0V.

Using an optimized VIP (Vertically Integrated PNP) process, the LP2985LV-N delivers unequaled performance in all specifications critical to battery-powered designs:

**Ground Pin Current:** Typically 825 µA @ 150 mA load, and 75 µA @ 1 mA load.

**Enhanced Stability:** The LP2985LV-N is stable with output capacitor ESR as low as 5 mΩ, which allows the use of ceramic capacitors on the output.

**Sleep Mode:** Less than 1 µA quiescent current when ON/OFF pin is pulled low.

**Smallest Possible Size:** DSBGA package uses absolute minimum board space.

**Precision Output:** 1% tolerance output voltages available (A grade).

**Low Noise:** By adding a 10 nF bypass capacitor, output noise can be reduced to 30 µV (typical).

### Block Diagram

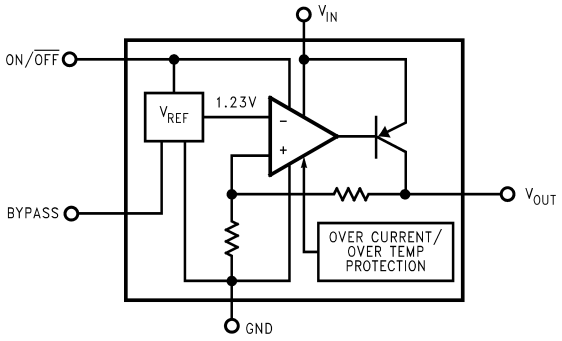
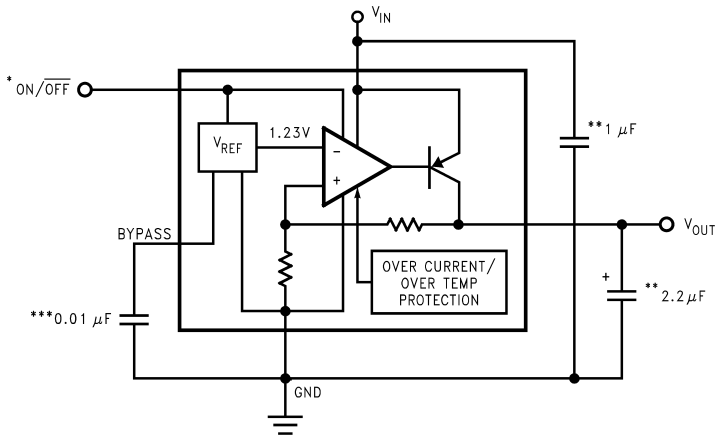



**Figure 1.**

## Basic Application Circuit




*ON/OFF input must be actively terminated. Tie to $V_{IN}$ if this function is not to be used.
**Minimum capacitance is shown to ensure stability (may be increased without limit). Ceramic capacitor required for output (see APPLICATION HINTS).
***Reduces output noise (may be omitted if application is not noise critical). Use ceramic or film type with very low leakage current (see APPLICATION HINTS).

**Figure 2.**

## Connection Diagram

**Note:** The actual physical placement of the package marking will vary from part to part. Package marking contains date code and lot traceability information, and will vary considerably. Package marking does not correlate to device type.

**Top View**

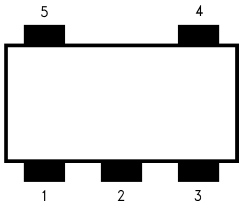



**Figure 3. 5-Lead SOT-23 Package**
**See Package Number DBV0005A**

**Top View**

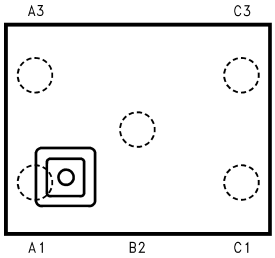



**Figure 4. 5 Bump DSBGA Package**
**See Package Number YPB0005**

### PIN DESCRIPTIONS

| Name | Pin Number | | Function |
|---|---|---|---|
| | SOT-23 | DSBGA | |
| $V_{IN}$ | 1 | C3 | Input Voltage |
| GND | 2 | A1 | Common Ground (device substrate) |
| ON/OFF | 3 | A3 | Logic high enable input |
| BYPASS | 4 | B2 | Bypass capacitor for low noise operation |
| $V_{OUT}$ | 5 | C1 | Regulated output voltage |

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS(1)(2)

| | |
|---|---|
| Storage Temperature Range | −65°C to +150°C |
| Operating Junction Temperature Range | −40°C to +125°C |
| Lead Temp. (Soldering, 5 sec.) | 260°C |
| ESD Rating(3) | 2 kV |
| Power Dissipation(4) | Internally Limited |
| Input Supply Voltage (Survival) | −0.3V to +16V |
| Input Supply Voltage (Operating) | 2.2V to +16V |
| Shutdown Input Voltage (Survival) | −0.3V to +16V |
| Output Voltage (Survival(5)) | −0.3V to +9V |
| $I_{OUT}$ (Survival) | Short Circuit Protected |
| Input-Output Voltage (Survival(6)) | −0.3V to +16V |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The ESD rating of pins 3 and 4 for the SOT-23 package, or pins 5 and 2 for the DSBGA package, is 1 kV.
(4) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_J(MAX)$, the junction-to-ambient thermal resistance, $\theta_{J-A}$, and the ambient temperature, $T_A$. The maximum allowable power dissipation at any ambient temperture is calculated using:

$$P(MAX) = \frac{T_J(MAX) - T_A}{\theta_{J-A}}$$

Where the value of $\theta_{J-A}$ for the SOT-23 package is 220°C/W in a typical PC board mounting. Exceeding the maximum allowable dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.
(5) If used in a dual-supply system where the regulator load is returned to a negative supply, the LP2985LV-N output must be diode-clamped to ground.
(6) The output PNP structure contains a diode between the $V_{IN}$ to $V_{OUT}$ terminals that is normally reverse-biased. Reversing the polarity from $V_{IN}$ to $V_{OUT}$ will turn on this diode, and possibly damage the device (See APPLICATION HINTS).

## ELECTRICAL CHARACTERISTICS[1]

Limits in standard typeface are for $T_J$ = 25°C. and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: $V_{IN} = V_{O(NOM)} + 1V$, $I_L$ = 1 mA, $C_{IN}$ = 1 µF, $C_{OUT}$ = 4.7 µF, $V_{ON/OFF}$ = 2V.

| Symbol | Parameter | Conditions | Typ | LP2985AI-X.X[2] | | LP2985I-X.X[2] | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $\Delta V_O$ | Output Voltage Tolerance | $I_L$ = 1 mA | | −1.0 | 1.0 | −1.5 | 1.5 | %$V_{NOM}$ |
| | | 1 mA ≤ $I_L$ ≤ 50 mA | | −1.5<br>**−2.5** | 1.5<br>**2.5** | −2.5<br>**−3.5** | 2.5<br>**3.5** | |
| | | 1 mA ≤ $I_L$ ≤ 150 mA | | −2.5<br>**−3.5** | 2.5<br>**3.5** | −3.0<br>**−4.0** | 3.0<br>**4.0** | |
| $\frac{\Delta V_O}{\Delta V_{IN}}$ | Output Voltage Line Regulation | $V_O$(NOM)+1V ≤ $V_{IN}$ ≤ 16V | 0.007 | | 0.014<br>**0.032** | | 0.014<br>**0.032** | %/V |
| $I_{GND}$ | Ground Pin Current | $I_L$ = 0 | 65 | | 95<br>**125** | | 95<br>**125** | µA |
| | | $I_L$ = 1 mA | 75 | | 110<br>**170** | | 110<br>**170** | |
| | | $I_L$ = 10 mA | 120 | | 220<br>**400** | | 220<br>**400** | |
| | | $I_L$ = 50 mA | 300 | | 500<br>**900** | | 500<br>**900** | |
| | | $I_L$ = 150 mA | 825 | | 1200<br>**2000** | | 1200<br>**2000** | |
| | | $V_{ON/OFF}$ < 0.3V | 0.01 | | 0.8 | | 0.8 | |
| | | $V_{ON/OFF}$ < 0.15V | **0.05** | | **2** | | **2** | |
| $V_{IN}$(min) | Minimum Input Voltage Required To maintain Output Regulation[3] | | 2.05 | | **2.20** | | **2.20** | V |
| $V_{IN}$ - $V_{OUT}$ | Dropout Voltage[3] | IL = 50mA | 120 | | 150<br>**250** | | 150<br>**250** | mV |
| | | IL = 150mA | 280 | | 350<br>**600** | | 350<br>**600** | |
| $V_{ON/OFF}$ | ON/OFF Input Voltage[4] | High = O/P ON | 1.4 | **1.6** | | **1.6** | | V |
| | | Low = O/P OFF | 0.55 | | **0.15** | | **0.15** | |
| $I_{ON/OFF}$ | ON/OFF Input Current | $V_{ON/OFF}$ = 0 | 0.01 | | **−2** | | **−2** | µA |
| | | $V_{ON/OFF}$ = 5V | 5 | | **15** | | **15** | |
| $e_n$ | Output Noise Voltage (RMS) | BW = 300 Hz to 50 kHz,<br>$C_{OUT}$ = 10 µF<br>$C_{BYPASS}$ = 10 nF<br>$V_{OUT}$ = 1.8V | 30 | | | | | µV |
| $\frac{\Delta V_{OUT}}{\Delta V_{IN}}$ | Ripple Rejection | f = 1 kHz, $C_{BYPASS}$ = 10 nF<br>$C_{OUT}$ = 10 µF | 45 | | | | | dB |
| $I_O$(SC) | Short Circuit Current | $R_L$ = 0 (Steady State)[5] | 400 | | | | | mA |
| $I_O$(PK) | Peak Output Current | $V_{OUT}$ ≥ $V_o$(NOM) −5% | 350 | | | | | mA |

(1) Exposing the DSBGA device to direct sunlight will cause misoperation. See APPLICATION HINTS for additional information.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate Average Outgoing Quality Level (AOQL).
(3) $V_{IN}$ must be the greater of 2.2V or $V_{OUT(NOM)}$ + Dropout Voltage to maintain output regulation. Dropout Voltage is defined as the input to output differential at which the output voltage drops 2% below ther value measured with a 1V differential.
(4) The ON/OFF input must be properly driven to prevent possible misoperation. For details, refer to APPLICATION HINTS.
(5) The LP2985LV-N has foldback current limiting which allows a high peak current when $V_{OUT}$ > 0.5V, and then reduces the maximum output current as $V_{OUT}$ is forced to ground (see TYPICAL PERFORMANCE CHARACTERISTICS curves).

## TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified: $C_{IN}$ = 1µF, $C_{OUT}$ = 4.7µF, $V_{IN}$ = $V_{OUT}$(NOM) +1, $V_{OUT}$ = 1.8V, $T_A$ = 25°C, ON/OFF pin is tied to $V_{IN}$

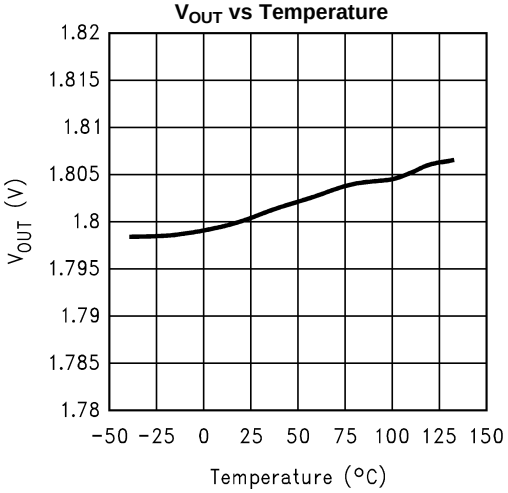



**Figure 5.**

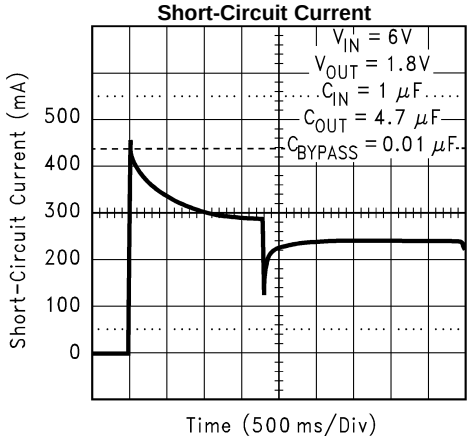



**Figure 6.**

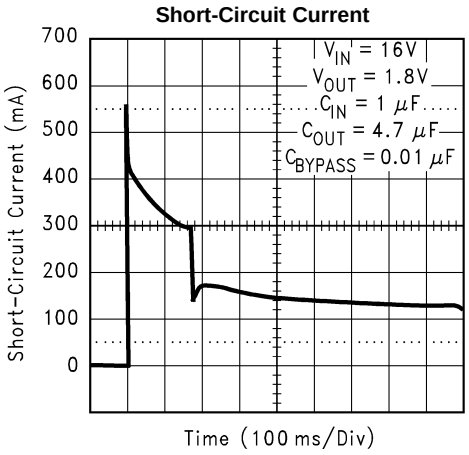



**Figure 7.**

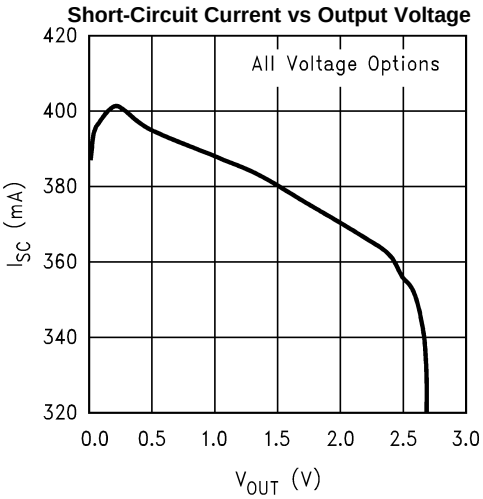



**Figure 8.**

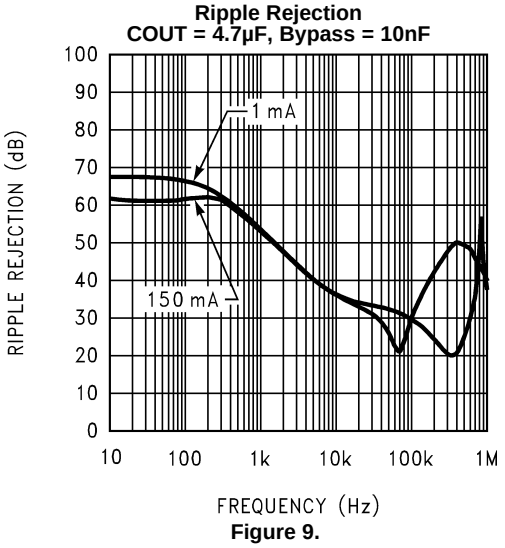



**Figure 9.**

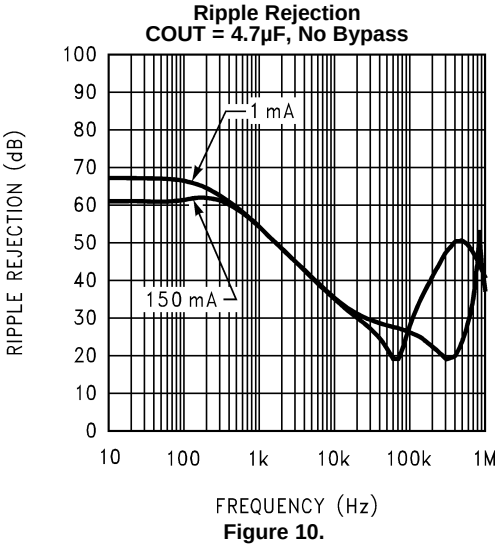



**Figure 10.**

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: $C_{IN}$ = 1µF, $C_{OUT}$ = 4.7µF, $V_{IN}$ = $V_{OUT}$(NOM) +1, $V_{OUT}$ = 1.8V, $T_A$ = 25°C, ON/OFF pin is tied to $V_{IN}$

**Output Impedance vs Frequency**

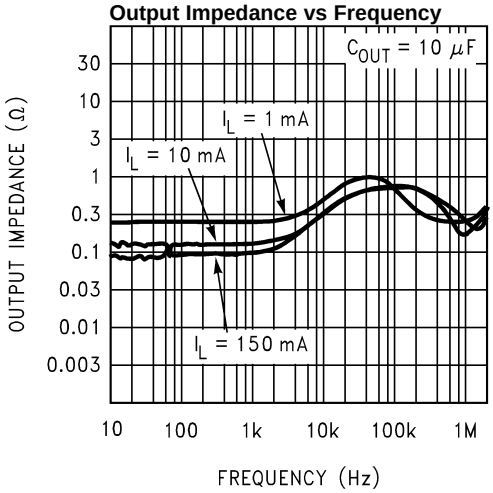



**Figure 11.**

**Output Impedance vs Frequency**

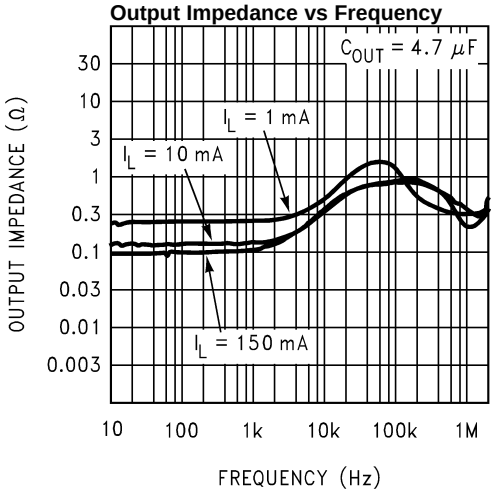



**Figure 12.**

**Noise Density**

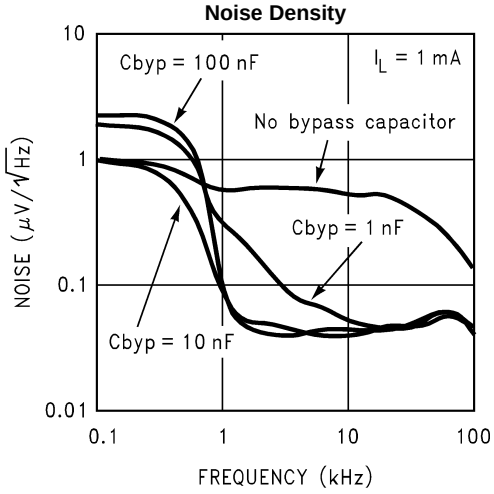



**Figure 13.**

**Noise Density**

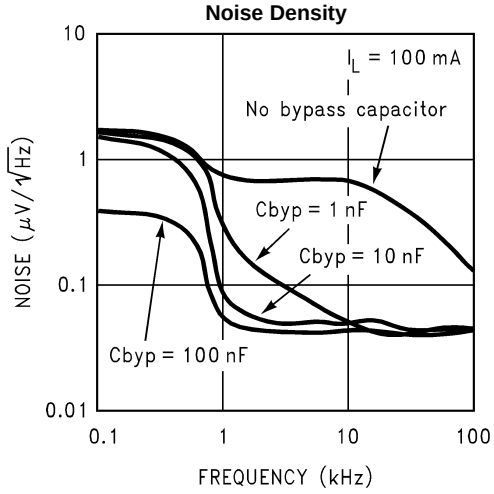



**Figure 14.**

**Ground Pin vs Load Current**

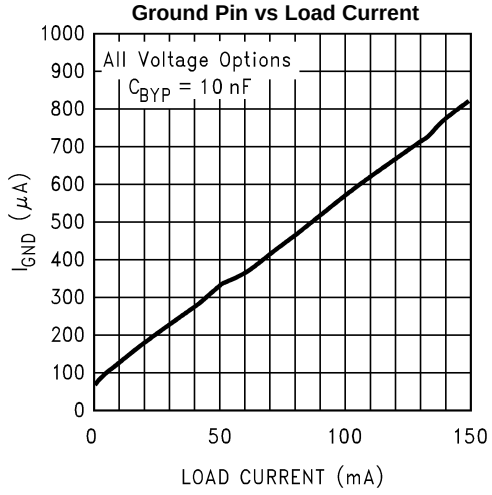



**Figure 15.**

**Minimum Input Voltage vs Temperature**

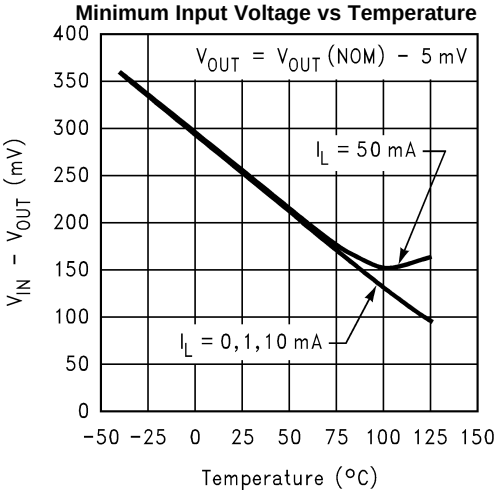



**Figure 16.**

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: $C_{IN}$ = 1µF, $C_{OUT}$ = 4.7µF, $V_{IN}$ = $V_{OUT}$(NOM) +1, $V_{OUT}$ = 1.8V, $T_A$ = 25°C, ON/OFF pin is tied to $V_{IN}$

**Minimum Input Voltage vs Temperature**

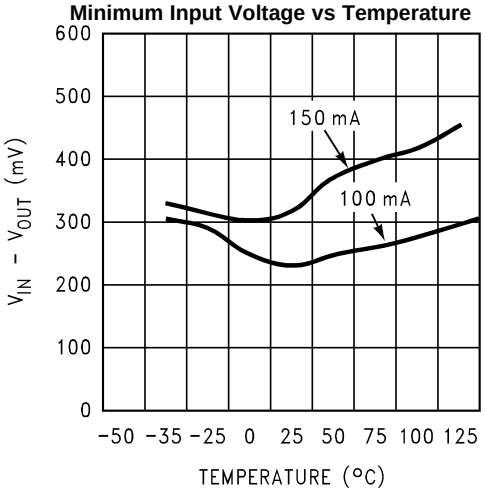



**Figure 17.**

**Input Current vs $V_{IN}$**

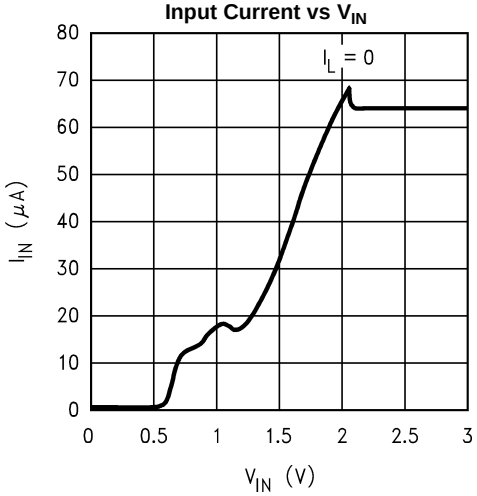



**Figure 18.**

**Input Current vs $V_{IN}$**

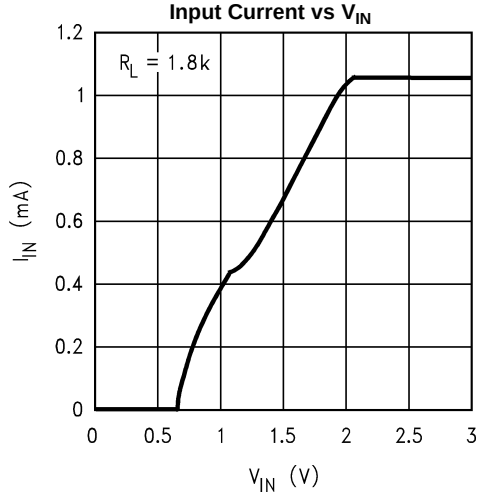



**Figure 19.**

**Input Current vs $V_{IN}$**

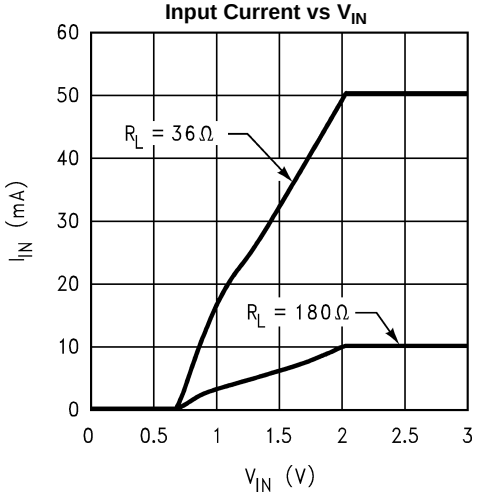



**Figure 20.**

**Ground Pin Current vs Temperature**

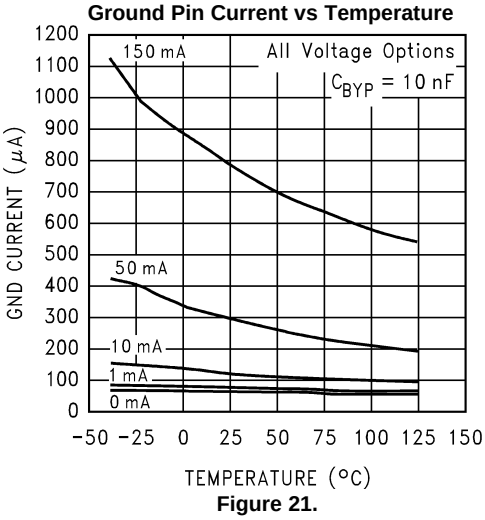



**Figure 21.**

**Instantaneous Short Circuit Current**

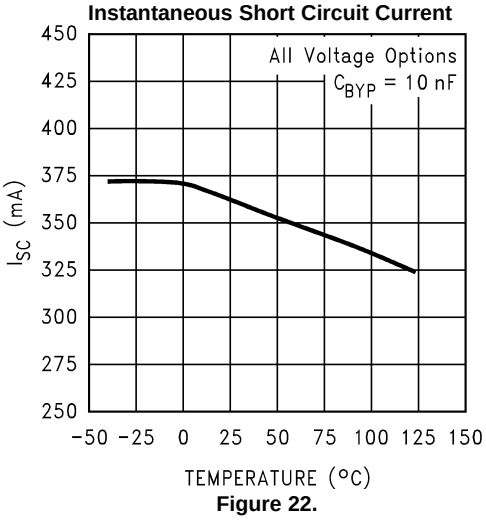



**Figure 22.**

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: $C_{IN}$ = 1µF, $C_{OUT}$ = 4.7µF, $V_{IN}$ = $V_{OUT}$(NOM) +1, $V_{OUT}$ = 1.8V, $T_A$ = 25°C, ON/OFF pin is tied to $V_{IN}$

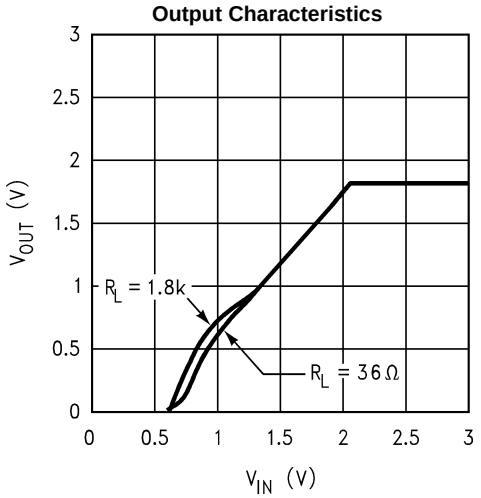



**Figure 23.**

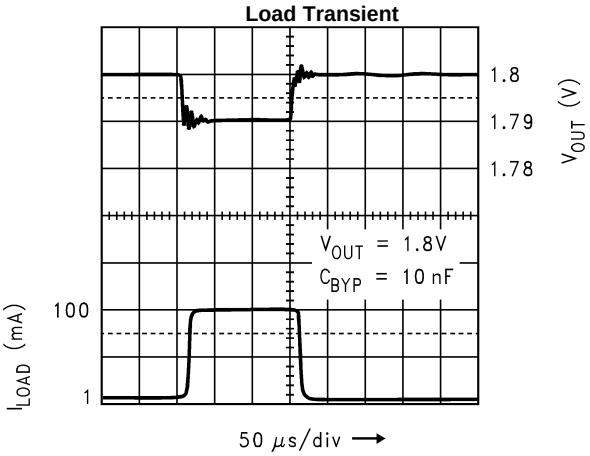



**Figure 24.**

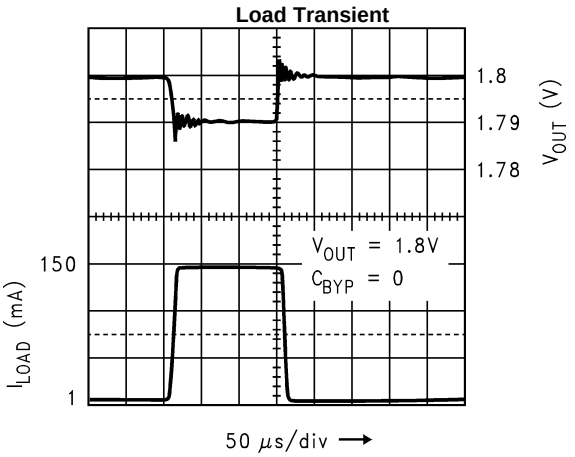



**Figure 25.**

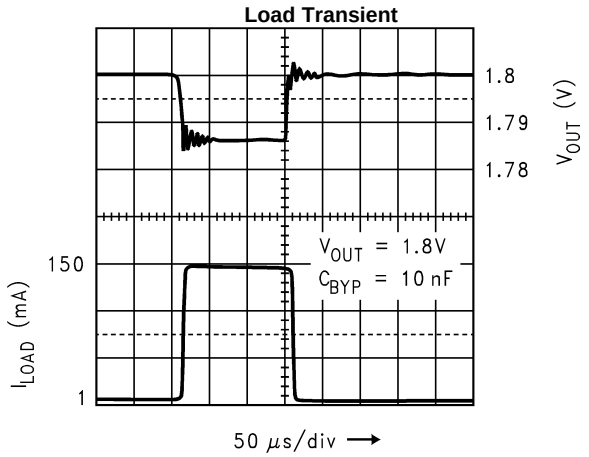



**Figure 26.**

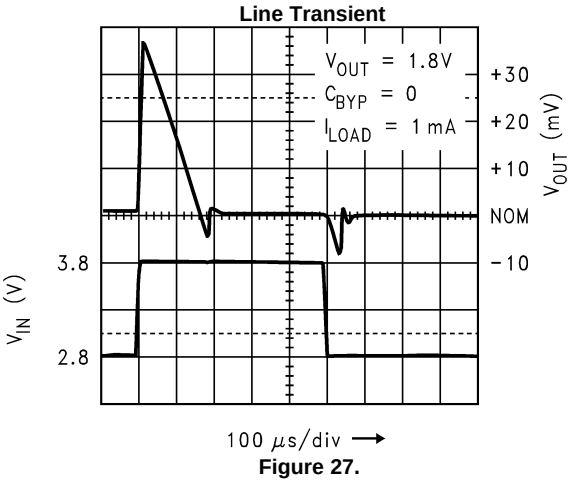



**Figure 27.**

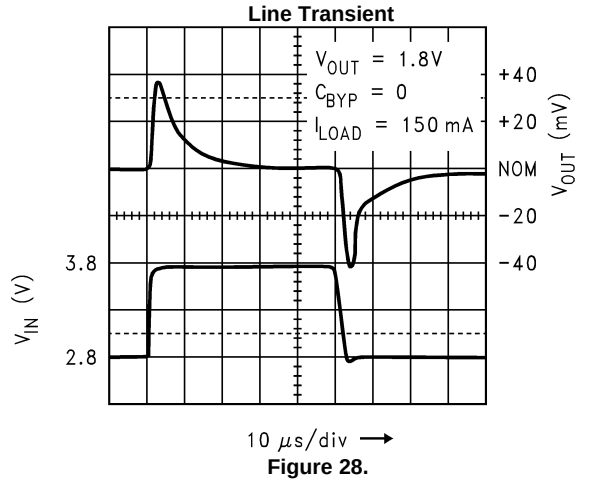



**Figure 28.**

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: $C_{IN}$ = 1µF, $C_{OUT}$ = 4.7µF, $V_{IN}$ = $V_{OUT}$(NOM) +1, $V_{OUT}$ = 1.8V, $T_A$ = 25°C, ON/OFF pin is tied to $V_{IN}$

**Line Transient**

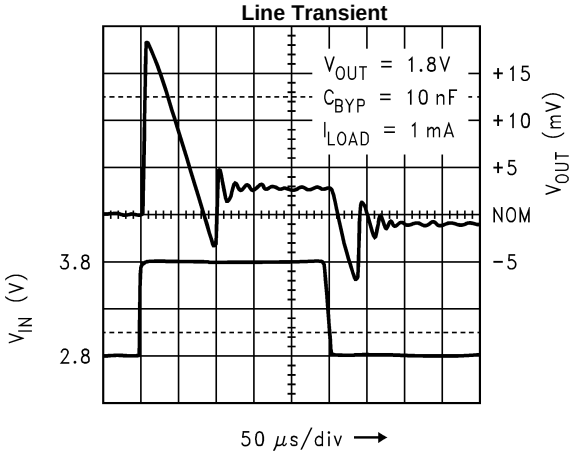



**Figure 29.**

**Line Transient**

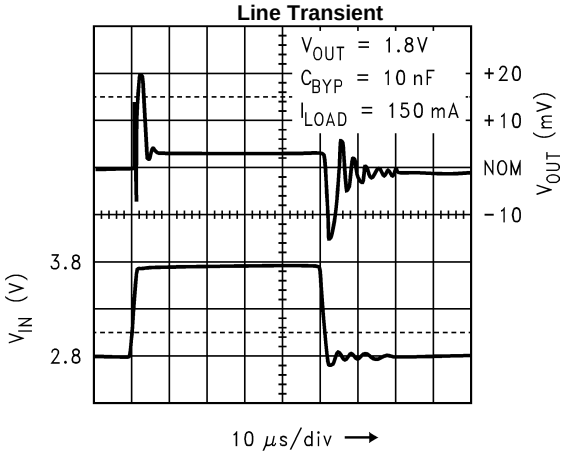



**Figure 30.**

**Turn-On Time**

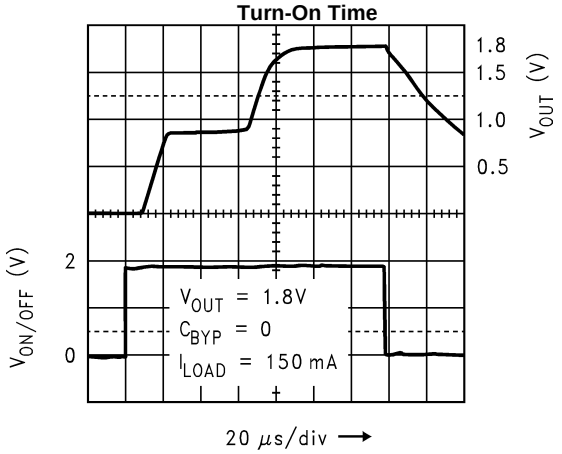



**Figure 31.**

**Turn-On Time**

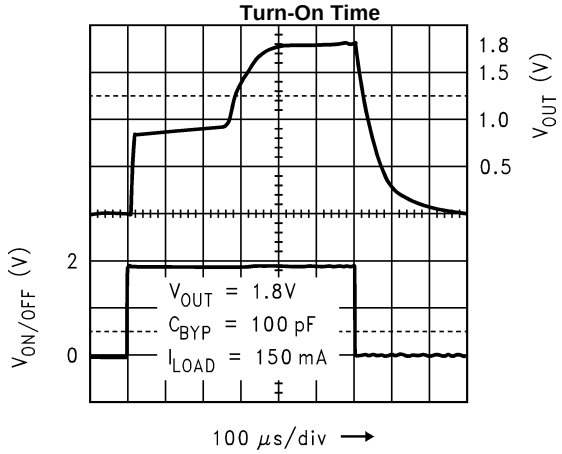



**Figure 32.**

**Turn-On Time**

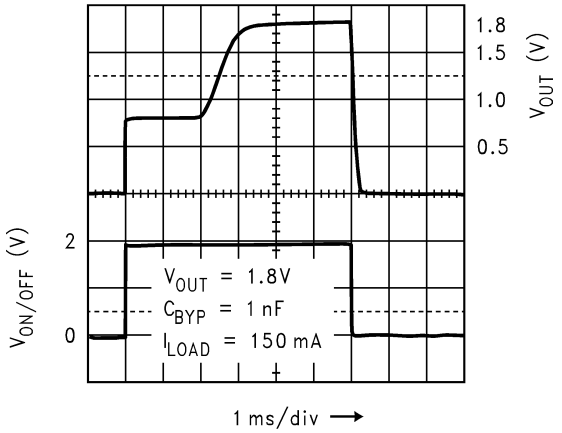



**Figure 33.**

**Turn-On Time**

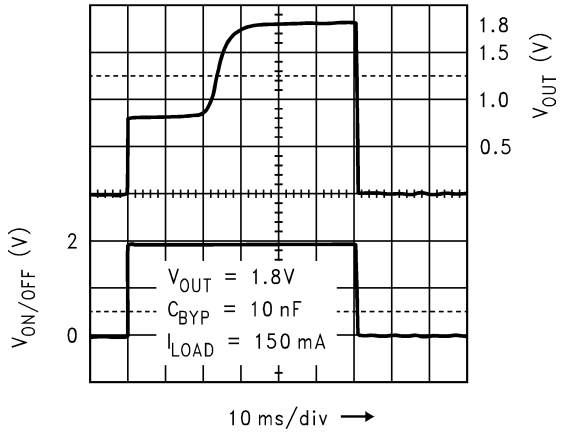



**Figure 34.**

## APPLICATION HINTS

### EXTERNAL CAPACITORS

Like any low-dropout regulator, the LP2985LV-N requires external capacitors for regulator stability. These capacitors must be correctly selected for good performance.

#### Input Capacitor

An input capacitor whose capacitance is ≥ 1 µF is required between the LP2985LV-N input and ground (the amount of capacitance may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

**Important:** Tantalum capacitors can suffer catastrophic failure due to surge current when connected to a low-impedance source of power (like a battery or very large capacitor). If a Tantalum capacitor is used at the input, it must be ensured by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for ESR on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will be ≥ 1 µF over the entire operating temperature range.

#### Output Capacitor

The LP2985LV-N is designed specifically to work with ceramic output capacitors, utilizing circuitry which allows the regulator to be stable across the entire range of output current with an output capacitor whose ESR is as low as 5 mΩ. It may also be possible to use Tantalum or film capacitors at the output, but these are not as attractive for reasons of size and cost (see CAPACITOR CHARACTERISTICS section).

The output capacitor must meet the requirement for minimum amount of capacitance and also have an ESR (equivalent series resistance) value which is within the stable range. Curves are provided which show the stable ESR range as a function of load current (see ESR graphs Figure 35 and Figure 36).

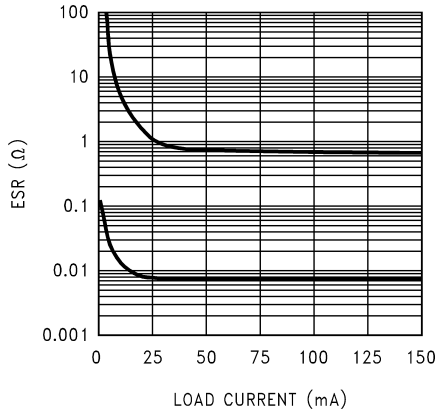



**Figure 35. LP2985LV-N 2.2µF Stable ESR Range**

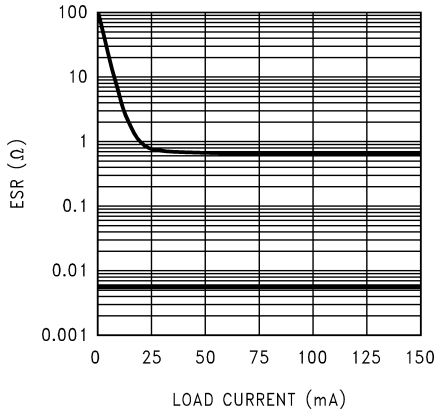



**Figure 36. LP2985LV-N 4.7µF Stable ESR Range**

**Important:** The output capacitor must maintain its ESR within the stable region over the full operating temperature range of the application to assure stability.

The LP2985LV-N requires a minimum of 2.2 µF on the output (output capacitor size can be increased without limit).

It is important to remember that capacitor tolerance and variation with temperature must be taken into consideration when selecting an output capacitor so that the minimum required amount of output capacitance is provided over the full operating temperature range. It should be noted that ceramic capacitors can exhibit large changes in capacitance with temperature (see CAPACITOR CHARACTERISTICS section).

The output capacitor must be located not more than 1 cm from the output pin and returned to a clean analog ground.

### Noise Bypass Capacitor

Connecting a 10 nF capacitor to the Bypass pin significantly reduces noise on the regulator output. It should be noted that the capacitor is connected directly to a high-impedance circuit in the bandgap reference.

Because this circuit has only a few microamperes flowing in it, any significant loading on this node will cause a change in the regulated output voltage. For this reason, DC leakage current through the noise bypass capacitor must never exceed 100 nA, and should be kept as low as possible for best output voltage accuracy.

The types of capacitors best suited for the noise bypass capacitor are ceramic and film. High-quality ceramic capacitors with either NPO or COG dielectric typically have very low leakage. 10 nF polypropolene and polycarbonate film capacitors are available in small surface-mount packages and typically have extremely low leakage current.

## CAPACITOR CHARACTERISTICS

The LP2985LV-N was designed to work with ceramic capacitors on the output to take advantage of the benefits they offer: for capacitance values in the 2.2 µF to 4.7 µF range, ceramics are the least expensive and also have the lowest ESR values (which makes them best for eliminating high-frequency noise). The ESR of a typical 2.2 µF ceramic capacitor is in the range of 10 mΩ to 20 mΩ, which easily meets the ESR limits required for stability by the LP2985LV-N.

One disadvantage of ceramic capacitors is that their capacitance can vary with temperature. Most large value ceramic capacitors (≥ 2.2 µF) are manufactured with the Z5U or Y5V temperature characteristic, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

This could cause problems if a 2.2 µF capacitor were used on the output since it will drop down to approximately 1 µF at high ambient temperatures (which could cause the LP2985LV-N to oscillate). If Z5U or Y5V capacitors are used on the output, a minimum capacitance value of 4.7 µF must be observed.

A better choice for temperature coefficient in ceramic capacitors is X7R, which holds the capacitance within ±15%. Unfortunately, the larger values of capacitance are not offered by all manufacturers in the X7R dielectric.

### Tantalum

Tantalum capacitors are less desirable than ceramics for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1 µF to 4.7 µF range.

Another important consideration is that Tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a Tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value.

It should also be noted that the ESR of a typical Tantalum will increase about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

### On/Off Input Operation

The LP2985LV-N is shut off by driving the ON/OFF input low, and turned on by pulling it high. If this feature is not to be used, the ON/OFF input should be tied to $V_{IN}$ to keep the regulator output on at all times.

To assure proper operation, the signal source used to drive the ON/OFF input must be able to swing above and below the specified turn-on/turn-off voltage thresholds listed in the ELECTRICAL CHARACTERISTICS(1) section under $V_{ON/OFF}$. To prevent mis-operation, the turn-on (and turn-off) voltage signals applied to the ON/OFF input must have a slew rate which is ≥ 40 mV/µs.

**CAUTION**

The regulator output voltage cannot be ensured if a slow-moving AC (or DC) signal is applied that is in the range between the specified turn-on and turn-off voltages listed under the electrical specification $V_{ON/OFF}$ (see Electrical Characteristics).

(1) Exposing the DSBGA device to direct sunlight will cause misoperation. See APPLICATION HINTS for additional information.

## REVERSE INPUT-OUTPUT VOLTAGE

The PNP power transistor used as the pass element in the LP2985LV-N has an inherent diode connected between the regulator output and input. During normal operation (where the input voltage is higher than the output) this diode is reverse-biased.

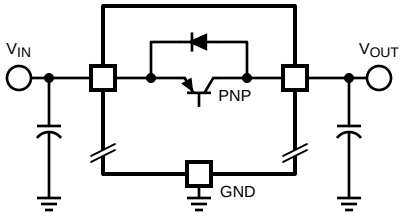



**Figure 37. Normal Operation**

However, if the output is pulled above the input, this diode will turn ON and current will flow into the regulator output. In such cases, a parasitic SCR can latch which will allow a high current to flow into $V_{IN}$ (and out the ground pin), which can damage the part.

In any application where the output may be pulled above the input, an external Schottky diode must be connected from $V_{IN}$ to $V_{OUT}$ (cathode on $V_{IN}$, anode on $V_{OUT}$), to limit the reverse voltage across the LP2985LV-N to 0.3V (see ABSOLUTE MAXIMUM RATINGS).

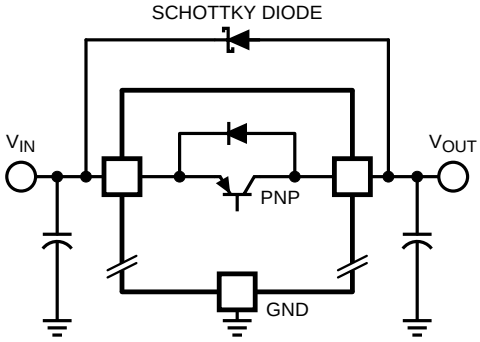



**Figure 38. Operation with Schottky Diode**

## DSBGA MOUNTING

The DSBGA package requires specific mounting techniques which are detailed in Texas Instruments Application Note AN-1112. Referring to the section Surface Mount Technology (SMT) Assembly Considerations, it should be noted that the pad style which must be used with the 5-pin package is the NSMD (non-solder mask defined) type.

For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the DSBGA device.

## DSBGA LIGHT SENSITIVITY

Exposing the DSBGA device to direct sunlight will cause misoperation of the device. Light sources such as Halogen lamps can also affect electrical performance if brought near to the device.

The wavelengths which have the most detrimental effect are reds and infra-reds, which means that the fluorescent lighting used inside most buildings has very little effect on performance. A DSBGA test board was brought to within 1 cm of a fluorescent desk lamp and the effect on the regulated output voltage was negligible, showing a deviation of less than 0.1% from nominal.

## REVISION HISTORY

| Changes from Revision O (April 2013) to Revision P | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 12 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LP2985AIM5-1.5 | ACTIVE | SOT-23 | DBV | 5 | 1000 | TBD | Call TI | Call TI | -40 to 125 | LCHA | Samples |
| LP2985AIM5-1.5/NOPB | ACTIVE | SOT-23 | DBV | 5 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LCHA | Samples |
| LP2985AIM5-1.8 | ACTIVE | SOT-23 | DBV | 5 | 1000 | TBD | Call TI | Call TI | -40 to 125 | LAYA | Samples |
| LP2985AIM5-1.8/NOPB | ACTIVE | SOT-23 | DBV | 5 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LAYA | Samples |
| LP2985AIM5-2.0 | ACTIVE | SOT-23 | DBV | 5 | 1000 | TBD | Call TI | Call TI | -40 to 125 | LCDA | Samples |
| LP2985AIM5-2.0/NOPB | ACTIVE | SOT-23 | DBV | 5 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LCDA | Samples |
| LP2985AIM5X-1.8 | ACTIVE | SOT-23 | DBV | 5 | 3000 | TBD | Call TI | Call TI | -40 to 125 | LAYA | Samples |
| LP2985AIM5X-1.8/NOPB | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LAYA | Samples |
| LP2985AIM5X-2.0 | ACTIVE | SOT-23 | DBV | 5 | 3000 | TBD | Call TI | Call TI | -40 to 125 | LCDA | Samples |
| LP2985AIM5X-2.0/NOPB | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LCDA | Samples |
| LP2985AITP-1.5/NOPB | ACTIVE | DSBGA | YPB | 5 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | 5 | Samples |
| LP2985AITP-1.8/NOPB | ACTIVE | DSBGA | YPB | 5 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | 5 | Samples |
| LP2985AITPX-1.5/NOPB | ACTIVE | DSBGA | YPB | 5 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | | 5 | Samples |
| LP2985AITPX-1.8/NOPB | ACTIVE | DSBGA | YPB | 5 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | 5 | Samples |
| LP2985IM5-1.8 | ACTIVE | SOT-23 | DBV | 5 | 1000 | TBD | Call TI | Call TI | -40 to 125 | LAYB | Samples |
| LP2985IM5-1.8/NOPB | ACTIVE | SOT-23 | DBV | 5 | 1000 | Green (RoHS & no Sb/Br) | SN | Level-1-260C-UNLIM | -40 to 125 | LAYB | Samples |
| LP2985IM5-2.0 | ACTIVE | SOT-23 | DBV | 5 | 1000 | TBD | Call TI | Call TI | -40 to 125 | LCDB | Samples |
| LP2985IM5-2.0/NOPB | ACTIVE | SOT-23 | DBV | 5 | 1000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LCDB | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LP2985IM5X-1.8 | ACTIVE | SOT-23 | DBV | 5 | 3000 | TBD | Call TI | Call TI | -40 to 125 | LAYB | Samples |
| LP2985IM5X-1.8/NOPB | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | SN | Level-1-260C-UNLIM | -40 to 125 | LAYB | Samples |
| LP2985IM5X-2.0 | ACTIVE | SOT-23 | DBV | 5 | 3000 | TBD | Call TI | Call TI | -40 to 125 | LCDB | Samples |
| LP2985IM5X-2.0/NOPB | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LCDB | Samples |
| LP2985ITP-1.5/NOPB | ACTIVE | DSBGA | YPB | 5 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | 5 | Samples |
| LP2985ITP-1.8/NOPB | ACTIVE | DSBGA | YPB | 5 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | 5 | Samples |
| LP2985ITPX-1.5/NOPB | ACTIVE | DSBGA | YPB | 5 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | | 5 | Samples |
| LP2985ITPX-1.8/NOPB | ACTIVE | DSBGA | YPB | 5 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | 5 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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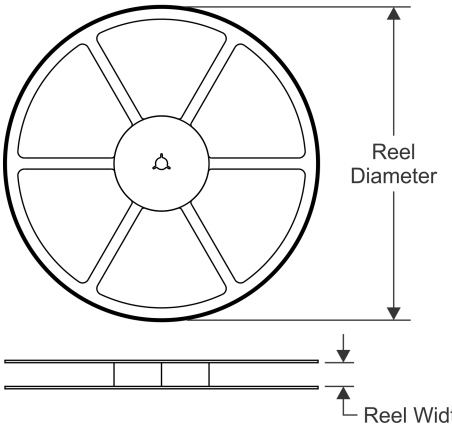
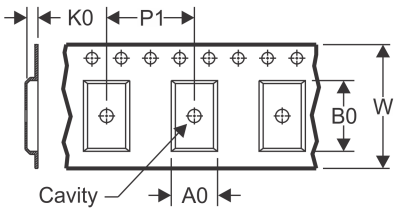
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

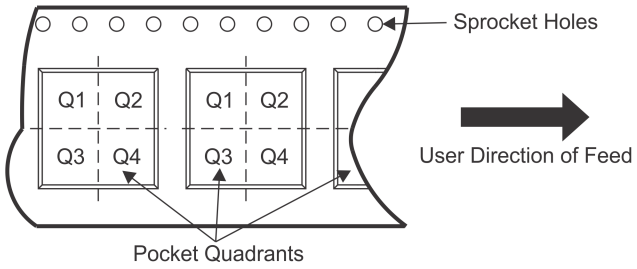



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

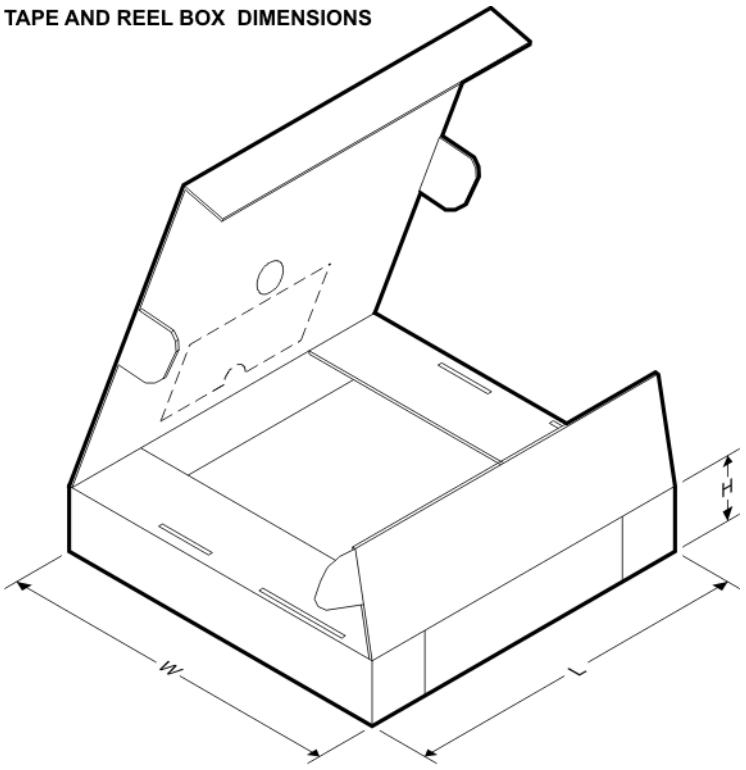



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LP2985AIM5-1.5 | SOT-23 | DBV | 5 | 1000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2985AIM5-1.5/NOPB | SOT-23 | DBV | 5 | 1000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2985AIM5-1.8 | SOT-23 | DBV | 5 | 1000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2985AIM5-1.8/NOPB | SOT-23 | DBV | 5 | 1000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2985AIM5-2.0 | SOT-23 | DBV | 5 | 1000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2985AIM5-2.0/NOPB | SOT-23 | DBV | 5 | 1000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2985AIM5X-1.8 | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2985AIM5X-1.8/NOPB | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2985AIM5X-2.0 | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2985AIM5X-2.0/NOPB | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2985AITP-1.5/NOPB | DSBGA | YPB | 5 | 250 | 178.0 | 8.4 | 1.02 | 1.19 | 0.66 | 4.0 | 8.0 | Q1 |
| LP2985AITP-1.8/NOPB | DSBGA | YPB | 5 | 250 | 178.0 | 8.4 | 1.02 | 1.19 | 0.66 | 4.0 | 8.0 | Q1 |
| LP2985AITPX-1.5/NOPB | DSBGA | YPB | 5 | 3000 | 178.0 | 8.4 | 1.02 | 1.19 | 0.66 | 4.0 | 8.0 | Q1 |
| LP2985AITPX-1.8/NOPB | DSBGA | YPB | 5 | 3000 | 178.0 | 8.4 | 1.02 | 1.19 | 0.66 | 4.0 | 8.0 | Q1 |
| LP2985IM5-1.8 | SOT-23 | DBV | 5 | 1000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2985IM5-1.8/NOPB | SOT-23 | DBV | 5 | 1000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2985IM5-2.0 | SOT-23 | DBV | 5 | 1000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2985IM5-2.0/NOPB | SOT-23 | DBV | 5 | 1000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LP2985IM5X-1.8 | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2985IM5X-1.8/NOPB | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2985IM5X-2.0 | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2985IM5X-2.0/NOPB | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LP2985ITP-1.5/NOPB | DSBGA | YPB | 5 | 250 | 178.0 | 8.4 | 1.02 | 1.19 | 0.66 | 4.0 | 8.0 | Q1 |
| LP2985ITP-1.8/NOPB | DSBGA | YPB | 5 | 250 | 178.0 | 8.4 | 1.02 | 1.19 | 0.66 | 4.0 | 8.0 | Q1 |
| LP2985ITPX-1.5/NOPB | DSBGA | YPB | 5 | 3000 | 178.0 | 8.4 | 1.02 | 1.19 | 0.66 | 4.0 | 8.0 | Q1 |
| LP2985ITPX-1.8/NOPB | DSBGA | YPB | 5 | 3000 | 178.0 | 8.4 | 1.02 | 1.19 | 0.66 | 4.0 | 8.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**

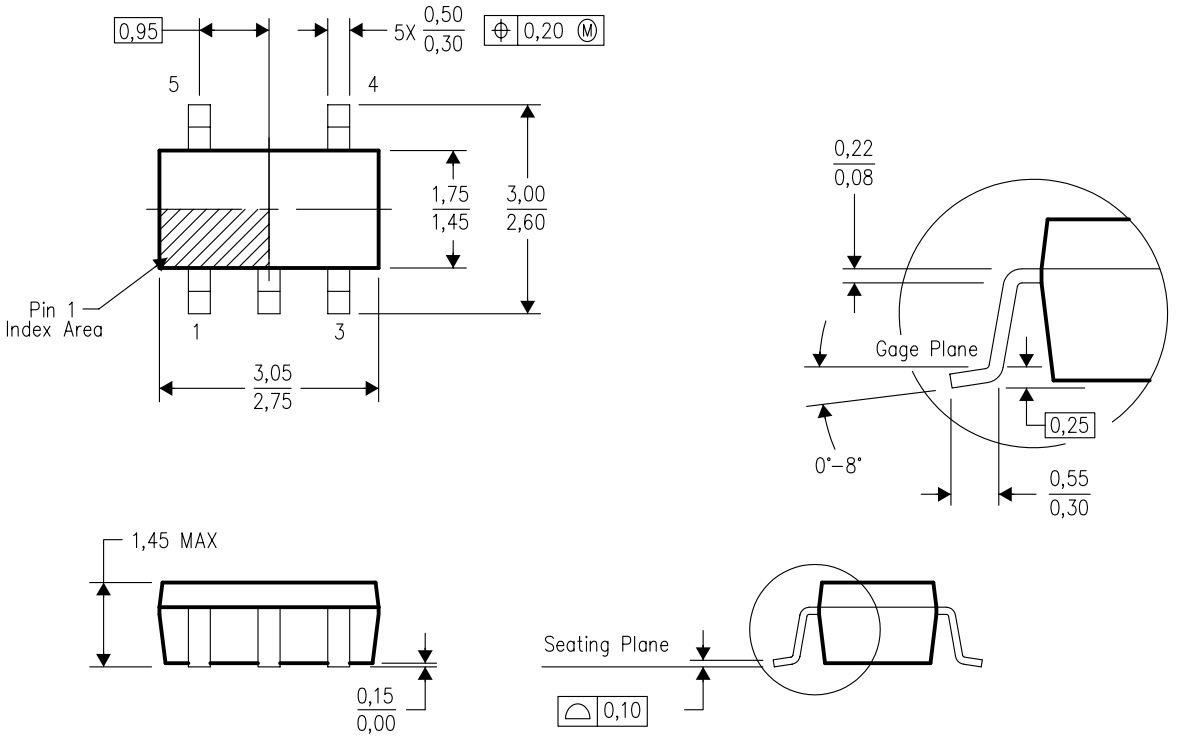



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LP2985AIM5-1.5 | SOT-23 | DBV | 5 | 1000 | 210.0 | 185.0 | 35.0 |
| LP2985AIM5-1.5/NOPB | SOT-23 | DBV | 5 | 1000 | 210.0 | 185.0 | 35.0 |
| LP2985AIM5-1.8 | SOT-23 | DBV | 5 | 1000 | 210.0 | 185.0 | 35.0 |
| LP2985AIM5-1.8/NOPB | SOT-23 | DBV | 5 | 1000 | 210.0 | 185.0 | 35.0 |
| LP2985AIM5-2.0 | SOT-23 | DBV | 5 | 1000 | 210.0 | 185.0 | 35.0 |
| LP2985AIM5-2.0/NOPB | SOT-23 | DBV | 5 | 1000 | 210.0 | 185.0 | 35.0 |
| LP2985AIM5X-1.8 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| LP2985AIM5X-1.8/NOPB | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| LP2985AIM5X-2.0 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LP2985AIM5X-2.0/NOPB | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| LP2985AITP-1.5/NOPB | DSBGA | YPB | 5 | 250 | 210.0 | 185.0 | 35.0 |
| LP2985AITP-1.8/NOPB | DSBGA | YPB | 5 | 250 | 210.0 | 185.0 | 35.0 |
| LP2985AITPX-1.5/NOPB | DSBGA | YPB | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| LP2985AITPX-1.8/NOPB | DSBGA | YPB | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| LP2985IM5-1.8 | SOT-23 | DBV | 5 | 1000 | 210.0 | 185.0 | 35.0 |
| LP2985IM5-1.8/NOPB | SOT-23 | DBV | 5 | 1000 | 210.0 | 185.0 | 35.0 |
| LP2985IM5-2.0 | SOT-23 | DBV | 5 | 1000 | 210.0 | 185.0 | 35.0 |
| LP2985IM5-2.0/NOPB | SOT-23 | DBV | 5 | 1000 | 210.0 | 185.0 | 35.0 |
| LP2985IM5X-1.8 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| LP2985IM5X-1.8/NOPB | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| LP2985IM5X-2.0 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| LP2985IM5X-2.0/NOPB | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| LP2985ITP-1.5/NOPB | DSBGA | YPB | 5 | 250 | 210.0 | 185.0 | 35.0 |
| LP2985ITP-1.8/NOPB | DSBGA | YPB | 5 | 250 | 210.0 | 185.0 | 35.0 |
| LP2985ITPX-1.5/NOPB | DSBGA | YPB | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| LP2985ITPX-1.8/NOPB | DSBGA | YPB | 5 | 3000 | 210.0 | 185.0 | 35.0 |

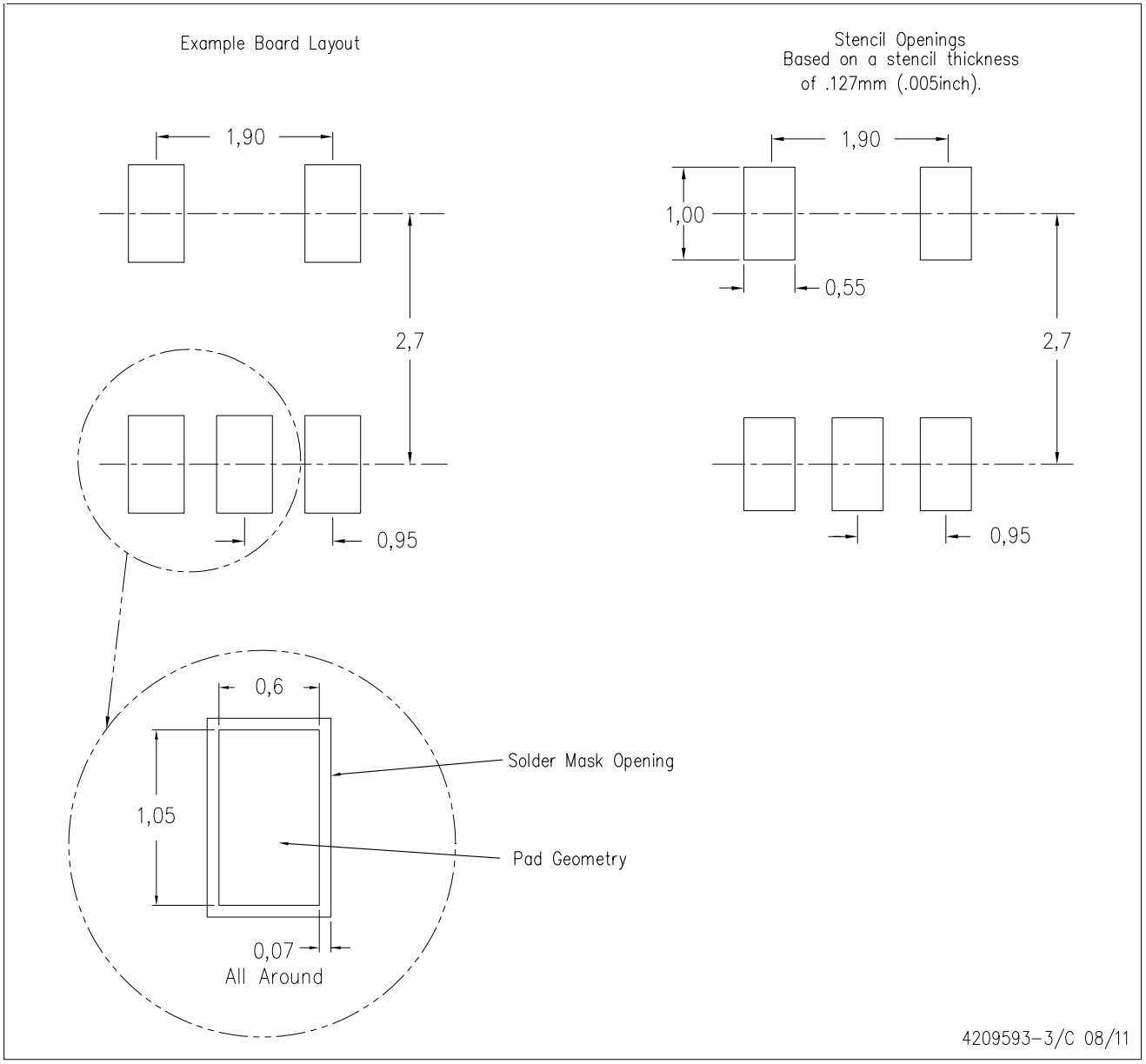
## DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE




4073253–4/K 03/2006

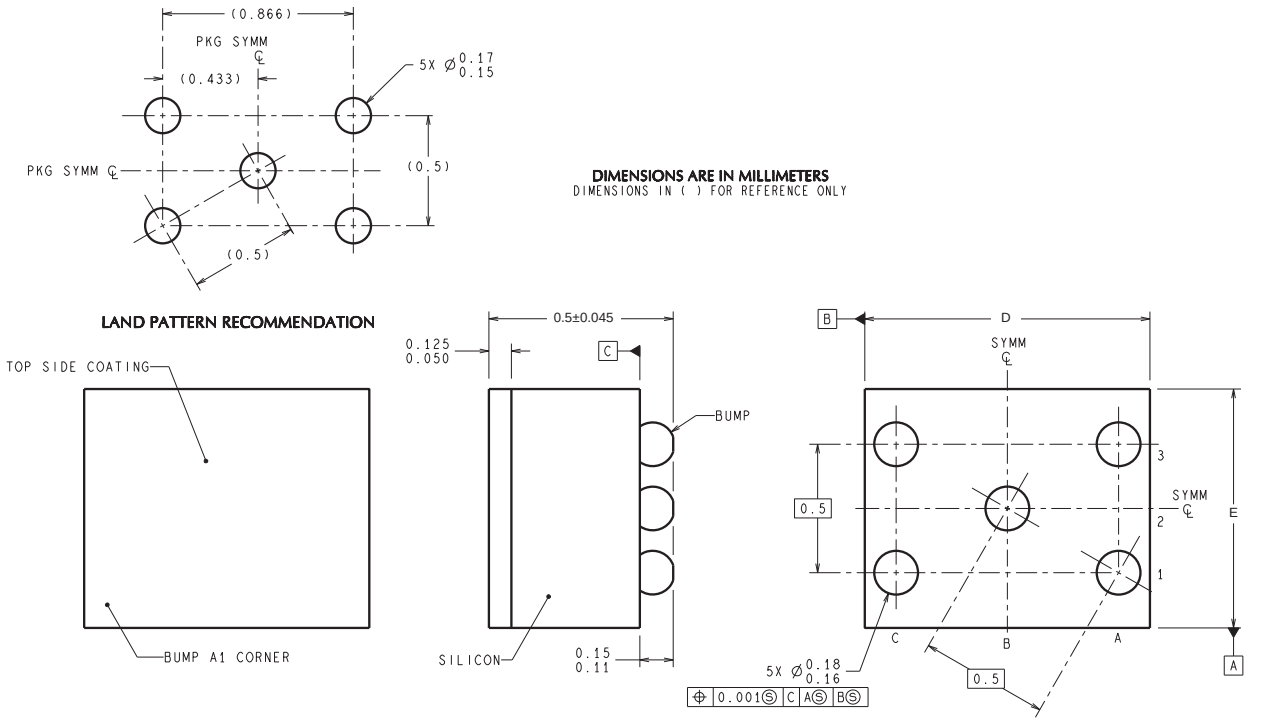
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

# YPB0005




D: Max = 1.159 mm, Min =1.098 mm

E: Max = 0.981 mm, Min = 0.92 mm

4215098/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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