CLC5802

CLC5802 Dual Low-Noise, Voltage Feedback Op Amp

Literature Number: SNOS524

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National Semiconductor

CLC5802
Dual Low-Noise, Voltage Feedback Op Amp

General Description

The CLC5802 is a dual op amp that offers a traditional voltage-feedback topology featuring unity-gain stability. Low noise and very low harmonic distortion combine to form a very wide dynamic-range op amp that operates within a power supply range of 5V to 12V.

Each of the CLC5802's closely matched channels provides a 140MHz unity-gain bandwidth with a very low input voltage noise density (4nV/$\sqrt{Hz}$). Low 2nd/3rd harmonic distortion (−69/−66dBc) as well as high channel-to-channel isolation (−61dB) make the CLC5802 a perfect wide dynamic-range amplifier for I/Q channels and other application which require low distortion and matching. With its fast and accurate settling (18ns to 0.1%), the CLC5802 is also a excellent choice for wide-dynamic range, anti-aliasing filters to buffer the inputs of hi-resolution analog-to-digital converters. Combining the CLC5802 two tightly-matched amplifiers in a single eight-pin SOIC reduces cost and board space for many composite amplifier applications such as active filters, differential line drivers/receivers, fast peak detectors and instrumentation amplifiers.

Features

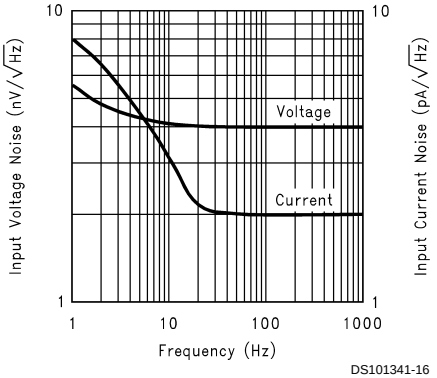
(T_A = 25°C, V_S = ±5V, R_L = 100Ω, Typical unless specified).

- Wide unity-gain bandwidth: 140MHz
- Ultra-low noise: 4nV/$\sqrt{Hz}$, 2pA/$\sqrt{Hz}$
- Low distortion: −69/−66dBc (5MHz)
- Settling time: 18ns to 0.1%
- High output current: ±70mA
- Supply voltage range: 5V to 12V

Applications

- General purpose dual op amp
- Low noise active filters
- Low noise integrators
- High-speed detectors
- Diff-in/diff-out instrumentation amp
- I/Q channel amplifiers
- Driver/receiver for transmission systems

Equivalent Input Noise



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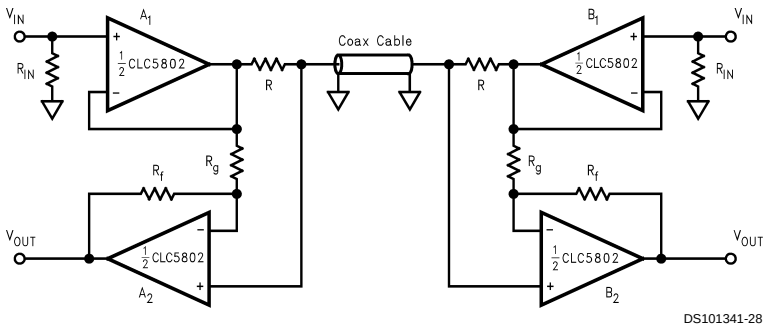
Typical Application

Full Duplex Transmission



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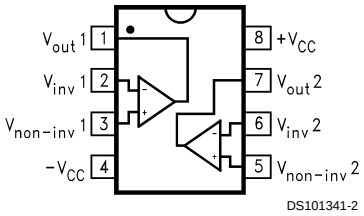
Connection Diagram

8-Pin SOIC



Top View

Ordering Information

Package	Part Number	Packaging Marking	Transport Media	NSC Drawing
8-pin SOIC	CLC5802IM	CLC5802IM	Rails	M08A
	CLC5802IMX	CLC5802IM	2.5k Tape and Reel	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	±7V
Short Circuit Current	(Note 3)
Common-Mode Input Voltage	$\pm V_{CC}$
Differential Input Voltage	±10V
Maximum Junction Temperature	+125˚C
Storage Temperature	−65˚C to +150˚C
Lead Temperature (soldering 10 sec)	+300˚C

Operating Rating (Note 1)

Thermal Resistance (θ_{JC})	40˚C/W
Thermal Resistance (θ_{JA})	115˚C/W
Temperature Range	−40˚C to +85˚C
Supply Voltage Range	5V to 12V

Electrical Characteristics

(T_A = +25˚C, V_{CC} = ±5V, A_V = +2V/V, R_f = 100Ω, R_g = 100Ω, R_L= 100Ω; unless specified).

Symbol	Parameter	Conditions	Typ	Min/Max Ratings (Note 2)			Units
			+25˚C	+25˚C	0˚C to +70˚C	−40˚C to +85˚C	
Frequency Domain Response							
GBW	Gain Bandwidth Product	$V_{OUT} < 0.5V_{PP}$	120	90			MHz
SSBW	−3dB Bandwidth (A_V = +1)	$V_{OUT} < 0.5V_{PP}$	140	110			
	−3dB Bandwidth (A_V = +2)	$V_{OUT} < 0.5V_{PP}$	75	50			
LSBW	−3dB Bandwidth	$V_{OUT} < 5.0V_{PP}$	40	25			
GFP	Gain Flatness Peaking	DC to 200MHz, $V_{OUT} < 0.5 V_{PP}$	0.0	0.6			dB
GFR	Gain Flatness Rolloff	DC to 20MHz, $V_{OUT} < 0.5 V_{PP}$	0.05	0.5			dB
LPD	Linear Phase Deviation	DC to 20MHz	0.2	1.0			Deg
Time Domain Response							
TRS	Rise and Fall Time	1V step	6	8			ns
TSS	Settling Time	2V step to 0.1%	18	22			ns
OS	Overshoot	1V step	1	5			%
SR	Slew Rate	5V step	450	275			V/µs
Distortion And Noise Response							
HD2	2nd Harmonic Distortion	$1V_{PP}$, 5MHz	−69	−57			dBc
HD3	3rd Harmonic Distortion	$1V_{PP}$, 5MHz	−66	−54			dBc
VN	Equivalent Input Noise Voltage	1MHz to 100MHz	4.0	4.5			nV/$\sqrt{Hz}$
ICN	Equivalent Input Noise Current	1MHz to 100MHz	2.0	3.0			pA/$\sqrt{Hz}$
CT	Crosstalk	Input referred, 10MHz	−61	−58			dB
Static, DC Performance							
AOL	Open-Loop Gain	DC	60	56	50	50	dB
VIO	Input Offset Voltage (Note 4)		±1.0	±2.0	±3.0	±3.5	mV
DVIO	Offset Voltage Average Drift		5	–	15	20	µV/˚C
IB	Input Bias Current (Note 4)		1.5	25	40	65	µA
DIB	Bias Current Average Drift		150	–	600	700	nA/˚C
IIO	Input Offset Current		0.3	3	5	5	µA
DIIO	Offset Current Average Drift		5	–	25	50	nA/˚C
PSRR	Power Supply Rejection Ratio	DC	63	57	55	55	dB
CMRR	Common Mode Rejection Ratio	DC	60	54	52	52	dB
ICC	Supply Current (Note 4)	Per Channel, R_L = ∞	11	12	13	15	mA

Electrical Characteristics (Continued)

(T_A = +25˚C, V_{CC} = ±5V, A_V = +2V/V, R_f = 100Ω, R_g = 100Ω, R_L= 100Ω; unless specified).

Symbol	Parameter	Conditions	Typ	Min/Max Ratings (Note 2)			Units
			+25˚C	+25˚C	0˚C to +70˚C	−40˚C to +85˚C	
Miscellaneous Performance							
RINC	Input Resistance	Common-Mode	500	250	125	125	kΩ
RIND		Differential-Mode	200	50	25	25	kΩ
CINC	Input Capacitance	Common-Mode	2.0	3.0	3.0	3.0	pF
CIND		Differential-Mode	2.0	3.0	3.0	3.0	pF
ROUT	Output Resistance	Closed Loop	0.05	0.1	0.2	0.2	Ω
VO	Output Voltage Range	R_L = ∞	±3.6	±3.5	±3.3	±3.3	V
VOL		R_L = 100Ω	±3.4	±3.2	±2.6	±1.3	V
CMIR	Input Voltage Range	Common-Mode	±3.7	±3.5	±3.3	±3.3	V
IO	Output Current		±70	±50	±40	±20	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed,

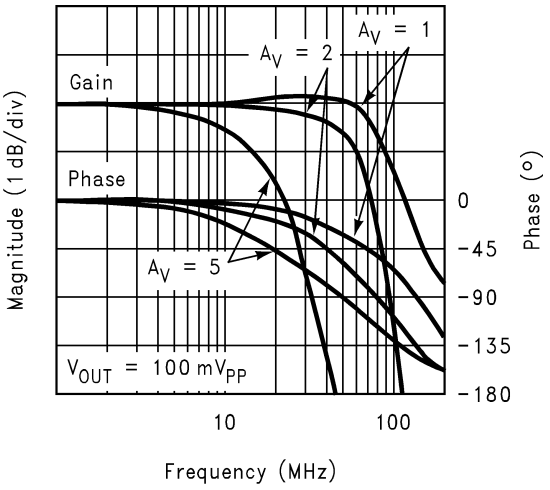
Note 2: Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Note 3: Output is short circuit protected to ground, however maximum reliability is obtained if output current does not exceed 160mA.

Note 4: 100% tested at +25˚C.

Typical Performance Characteristics (T_A = 25°C, V_{CC} = ±5V, R_g = 26.1Ω, R_f = 499Ω, R_L = 100Ω, unless otherwise specified).

Non-Inverting Frequency Response



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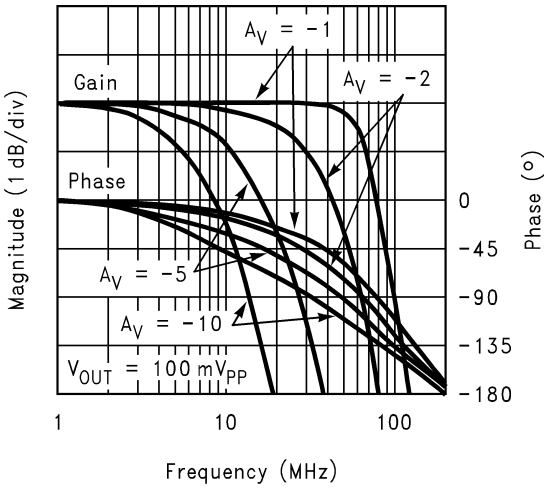
Inverting Frequency Response



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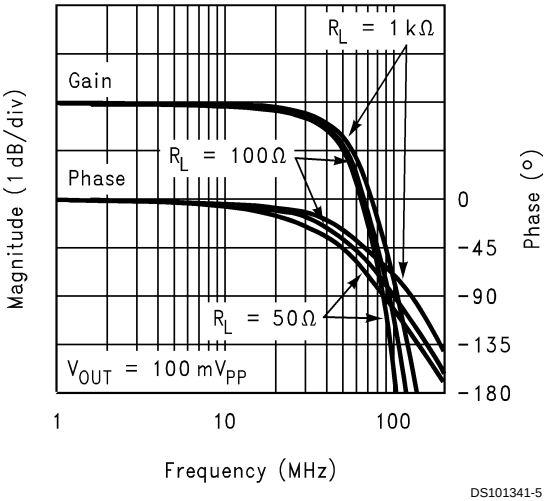
Frequency Response vs. Load Resistance



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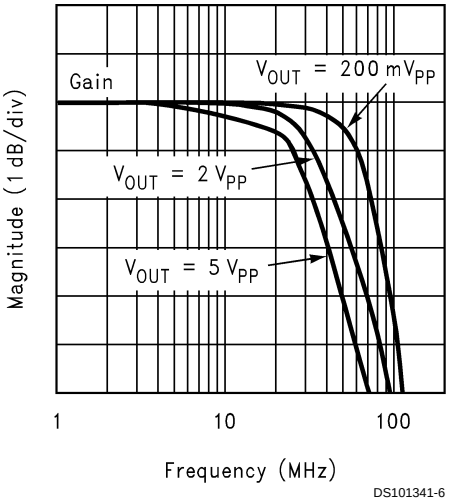
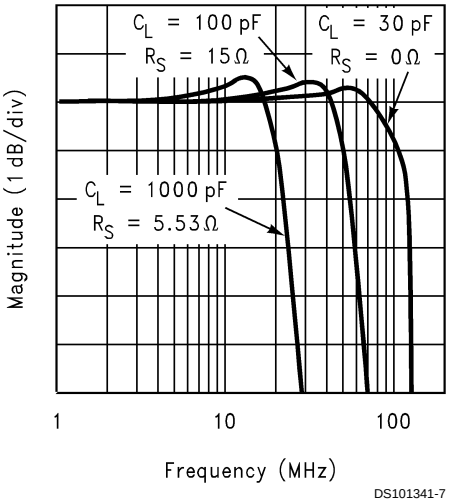
Frequency Response vs. Output Amplitude



DS101341-6

Frequency Response vs. Capacitive Load



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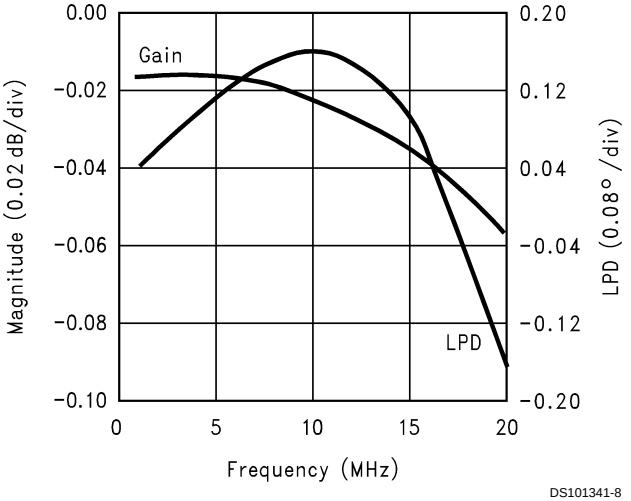
Gain Flatness & Linear Phase Deviation



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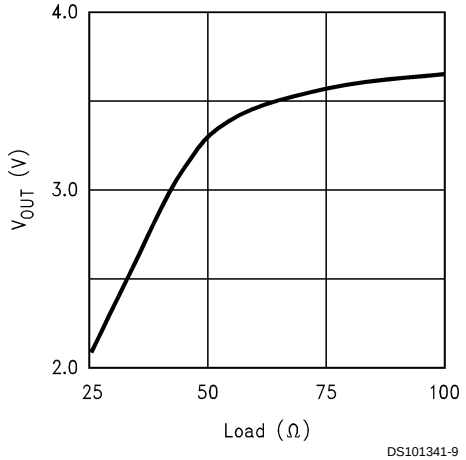
Typical Performance Characteristics (T_A = 25°C, V_{CC} = ±5V, R_g = 26.1Ω, R_f = 499Ω, R_L = 100Ω, unless otherwise specified).. (Continued)

Maximum Output Voltage vs. Load



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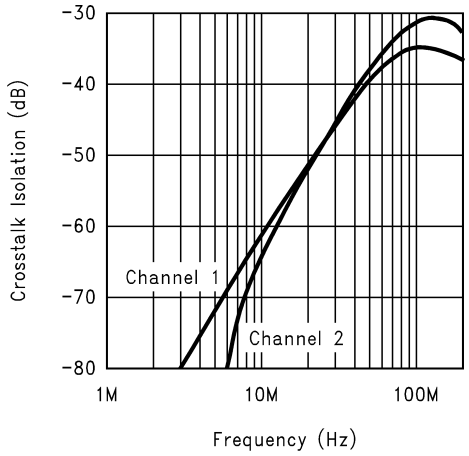
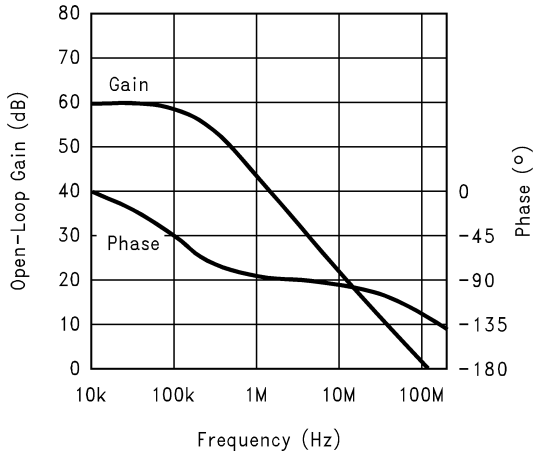
Channel-to-Channel Crosstalk



DS101341-10

Open-Loop Gain & Phase



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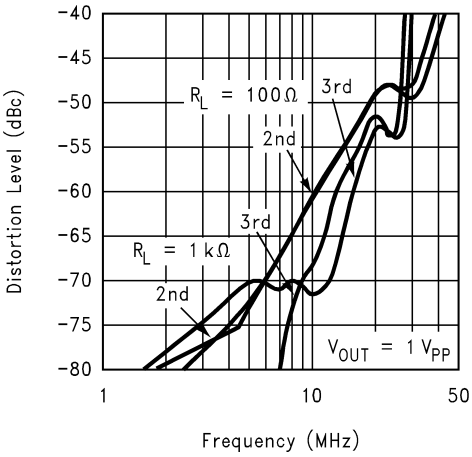
2nd and 3rd Harmonic Distortion



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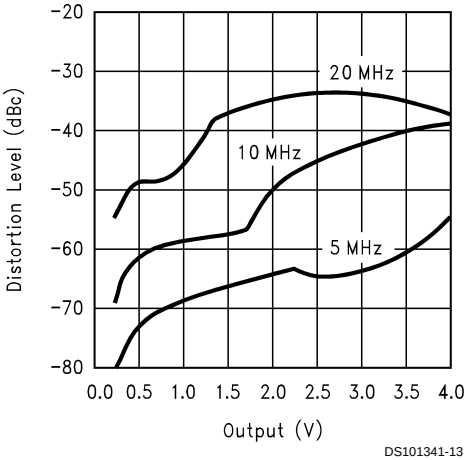
2nd Harmonic Distortion vs. Output Voltage



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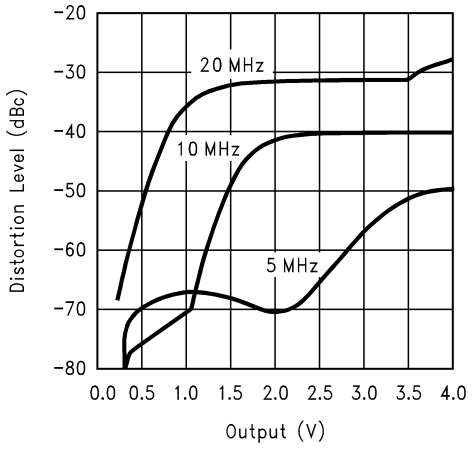
3rd Harmonic Distortion vs. Output Voltage



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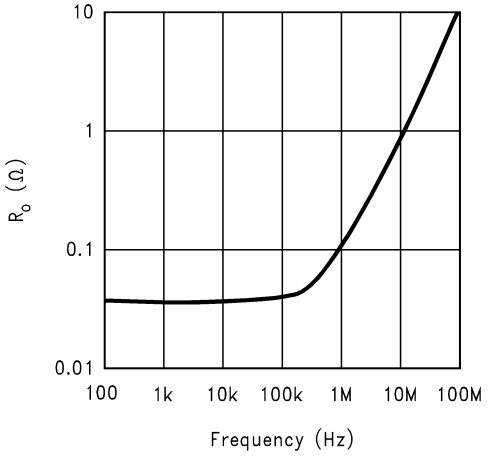
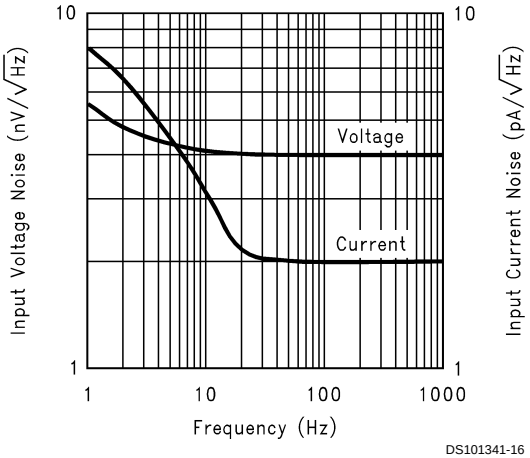
Typical Performance Characteristics (T_A = 25°C, V_{CC} = ±5V, R_g = 26.1Ω, R_f = 499Ω, R_L = 100Ω, unless otherwise specified).. (Continued)

Closed-Loop Output Resistance



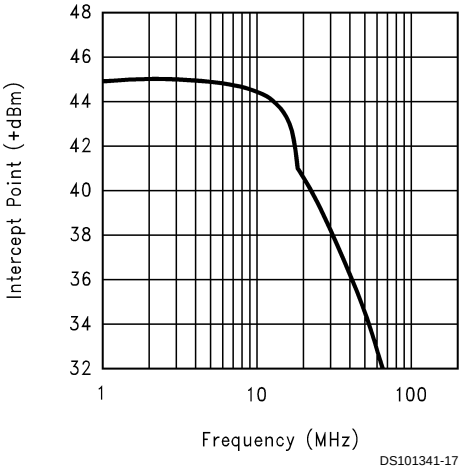
DS101341-15

Equivalent Input Noise



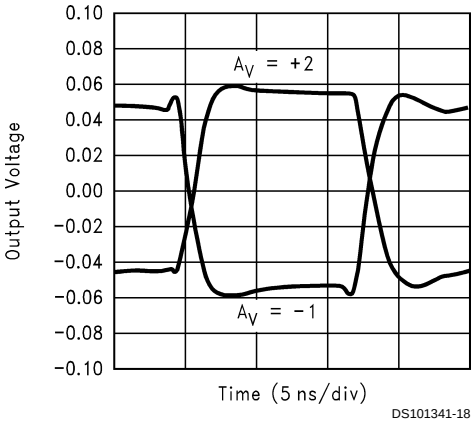
DS101341-16

2-Tone, 3rd order Intermodulation Intercept



DS101341-17

Pulse Response (V_{OUT} = 100mV)



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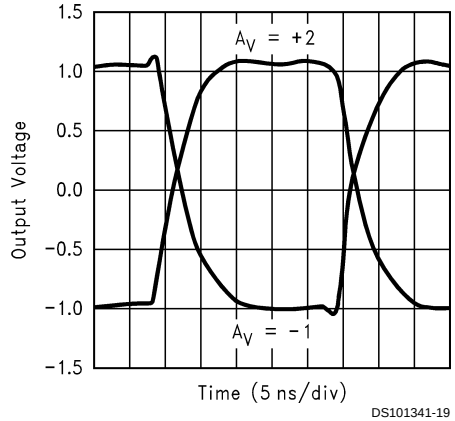
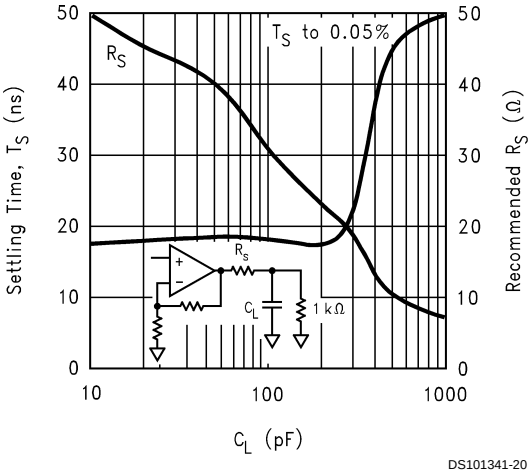
Pulse Response (V_{OUT} = 2V)



DS101341-19

Settling Time vs. Capacitive Load



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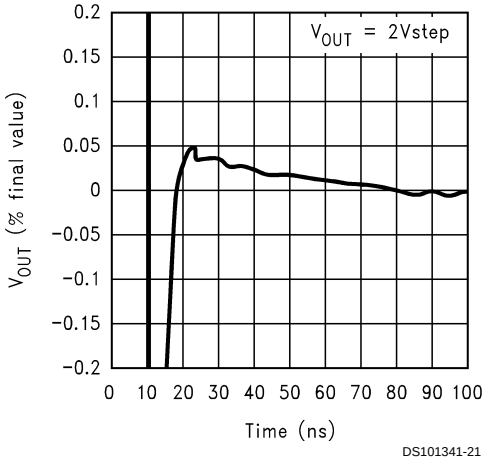
Typical Performance Characteristics (T_A = 25°C, V_{CC} = ±5V, R_g = 26.1Ω, R_f = 499Ω, R_L = 100Ω, unless otherwise specified).. (Continued)

Short-Term Settling Time



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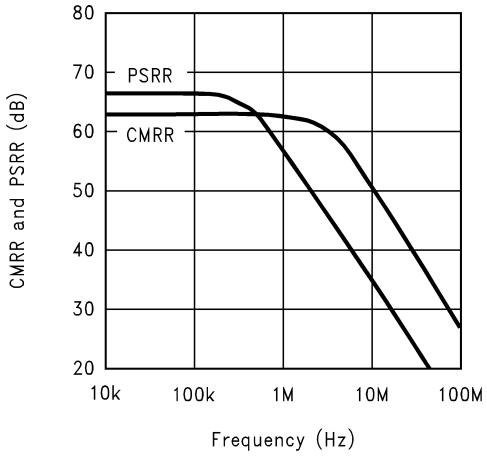
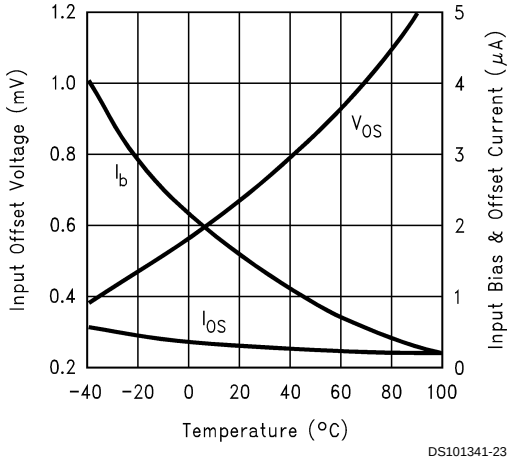
CMRR and PSRR



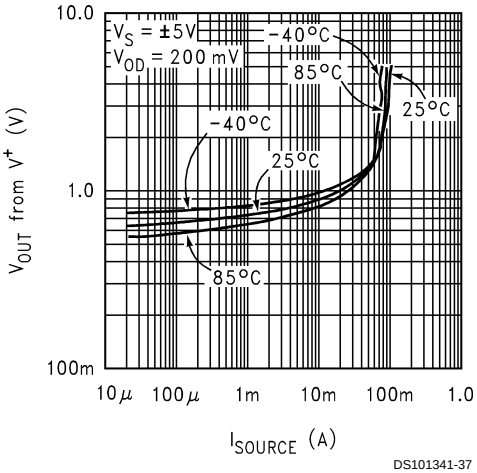
DS101341-22

Typical DC Errors vs. Temperature



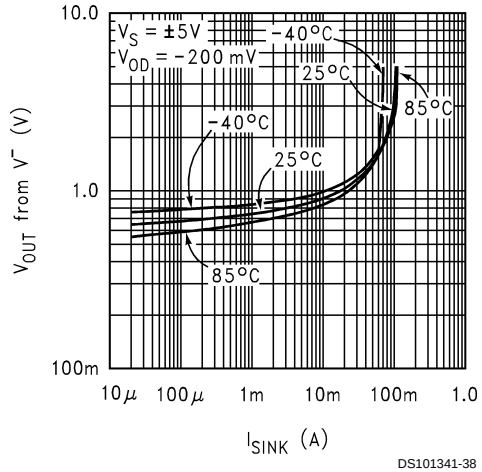
DS101341-23

Output Voltage vs. Output Sourcing Current



DS101341-37

Output Voltage vs. Output Sinking Current



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Application Information

Low Noise Design

Ultimate low noise performance from circuit designs using the CLC5802 requires the proper selection of external resistors. By selecting appropriate low-valued resistors for R_f and R_g, amplifier circuits using the CLC5802 can achieve output noise that is approximately the equivalent voltage input noise of $4nV/\sqrt{Hz}$ multiplied by the desired gain (A_V).

Each amplifier in the CLC5802 has an equivalent input noise resistance which is optimum for matching source impedances of approximately 2k. Using a transformer, any source can be matched to achieve the lowest noise design.

For even lower noise performance than the CLC5802, consider the CLC425, CLC426 or CLC5801 at 1.05, 1.6 and $2nV/\sqrt{Hz}$, respectively.

DC Bias Currents and Offset Voltages

Cancellation of the output offset voltage due to input bias currents is possible with the CLC5802. This is done by making the resistance seen from the inverting and non-inverting inputs equal. Once done, the residual output offset voltage will be the input offset voltage (V_{OS}) multiplied by the desired gain (A_V). Application Note OA-7 offers several solutions to further reduce the output offset.

Output and Supply Considerations

With ±5V supplies, the CLC5802 is capable of a typical output swing of ±3.6V under a no-load condition. Additional output swing is possible with slightly higher supply voltages. For loads of less than 50Ω, the output swing will be limited by the CLC5802's output current capability, typically 70mA.

Output settling time when driving capacitive loads can be improved by the use of a series output resistor. See the plot labeled "Settling Time vs. Capacitive Load" in the Typical Performance Characteristics section.

Layout

Proper power supply bypassing is critical to insure good high frequency performance and low noise. De-coupling capacitors of 0.1µF should be placed as close as possible to the power supply pins. The use of surface mounted capacitors is recommended due to their low series inductance.

A good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitance from these nodes to ground causes frequency response peaking and possible circuit oscillation. See OA-15 for more information. National suggests the CLC730038 (through-hole) or the CLC730036 (SOIC) dual op amp evaluation board as a guide for high frequency layout and as an aid in device evaluation.

Full Duplex Digital or Analog Transmission

Simultaneous transmission and reception of analog or digital signals over a single coaxial cable or twisted-pair line can reduce cabling requirements. The CLC5802's wide bandwidth and high common-mode rejection in a differential amplifier configuration allows full duplex transmission of video, telephone, control and audio signals.

In the circuit shown in *Figure 1*, one of the CLC5802's amps is used as a "driver" and the other as a difference "receiver" amplifier. The output impedance of the "driver" is essentially zero. The two R's are chosen to match the characteristic impedance of the transmission line. The "driver" op amp gain can be selected for unity or greater.

Receiver amplifier A_2 (B_2) is connected across R and forms a differential amplifier for the signals transmitted by driver A_1 (B_1). If the coax cable is lossless and R_f equals R_g, receiver A_2 (B_2) will then reject the signals from driver A_1 (B_1) and pass the signals from driver B_1 (A_1).

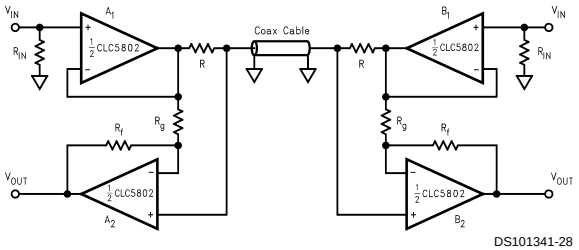


FIGURE 1.

The output of the receiver amplifier will be:

$$V_{OUT_{A(B)}} = \frac{1}{2} V_{IN_{A(B)}} \left(1 - \frac{R_f}{R_g}\right) + \frac{1}{2} V_{IN_{B(A)}} \left(1 + \frac{R_f}{R_g}\right) \quad (1)$$

Care must be given to layout and component placement to maintain a high frequency common-mode rejection. The plot of *Figure 2* show the simultaneous reception of signals transmitted at 1MHz and 10MHz.

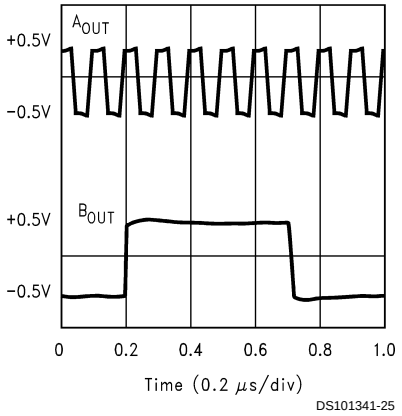


FIGURE 2.

Five Decade Integrator

A composite integrator, shown in *Figure 3*, uses the CLC5802 dual op amp to increase the circuits usable frequency range of operation. The transfer function of this circuit is:

$$V_O = \frac{1}{RC} \int V_{IN}\, dt \quad (2)$$

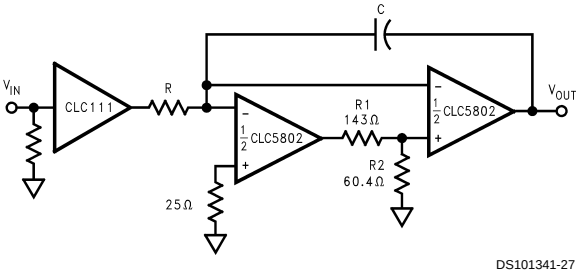


FIGURE 3.

Application Information (Continued)

A resistive divider made from the 143Ω and 60.4Ω resistors was chosen to reduce the loop-gain and stabilize the network. The CLC5802 composite integrator provides integration over five decades of operation. R and C set the integrator's gain. *Figure 4* shows the frequency and phase response of the circuit in *Figure 3* with R = 44.2Ω and C = 360pF.

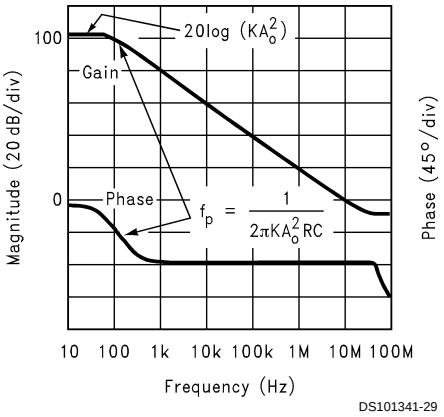


FIGURE 4.

K: R2/(R1 + R2)

A_0: Op amp low Frequency open loop gain

Positive Peak Detector

The CLC5802's dual amplifiers can be used to implement a unity-gain peak detector circuit as shown in *Figure 5*.

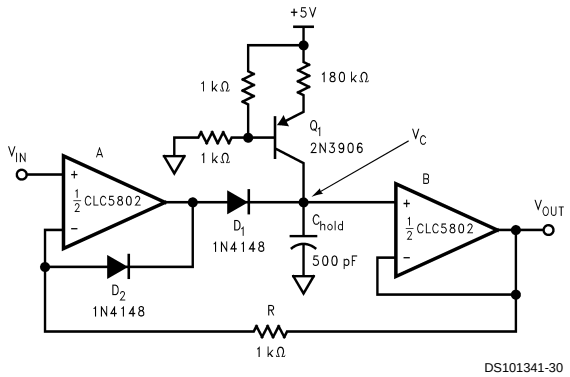


FIGURE 5.

The acquisition speed of this circuit is limited by the dynamic resistance of the diode when charging C_{hold}. A plot of the circuit's performance is shown in *Figure 6* with a 1MHz sinusoidal input.

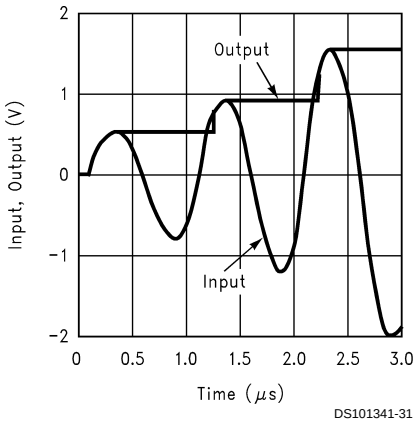


FIGURE 6.

A current source, built around Q1, provides the necessary bias current for the second amplifier and prevents saturation when power is applied. The resistor, R, closes the loop while diode D_2 prevents negative saturation when V_{IN} is less than V_C. A MOS-type switch (not shown) can be used to reset the capacitor's voltage.

The maximum speed of detection is limited by the delay of the op amp and the diodes. The use of Schottky diodes will provide faster response.

Adjustable or Bandpass Equalizer

A "boost" equalizer can be made with the CLC5802 by summing a bandpass response with the input signal, as shown in *Figure 7*.

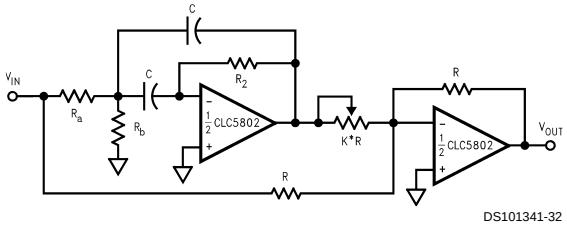


FIGURE 7.

The overall transfer function is shown in *Equation (3)*.

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{R_b}{K(R_a + R_b)}\right) \frac{s2Q\omega_o}{s^2 + s\frac{\omega_o}{Q} + \omega_o^2} - 1 \quad (3)$$

To build a boost circuit, use the design Equation 4 and 5.

$$\frac{R_2 C}{2} = \frac{Q}{\omega_o} \quad (4)$$

$$2C(R_a || R_b) = \frac{1}{Q\omega_o} \quad (5)$$

Select R_2 and C using *Equation (4)*. Use reasonable values for high frequency circuits - R_2 between 10Ω and 5kΩ, C between 10pF and 2000pF. Use *Equation (5)* to determine the parallel combination of R_a and R_b. Select R_a and R_b by either the 10Ω to 5kΩ criteria or by other requirements based on the impedance V_{IN} is capable of driving. Finish the design by determining the value of K from *Equation (6)*.

Application Information (Continued)

$$\text{Peak Gain} = \frac{V_{OUT}}{V_{IN}}(\omega_o) = \frac{R_2}{2KR_a} - 1 \quad (6)$$

Figure 8 shows an example of the response of the circuit of *Figure 7*, where f_O is 2.3MHz. The component values are as follows: R_a = 2.1kΩ, R_b = 68.5Ω, R_2 = 4.22kΩ, R = 500Ω, KR = 50Ω, C = 120pF.

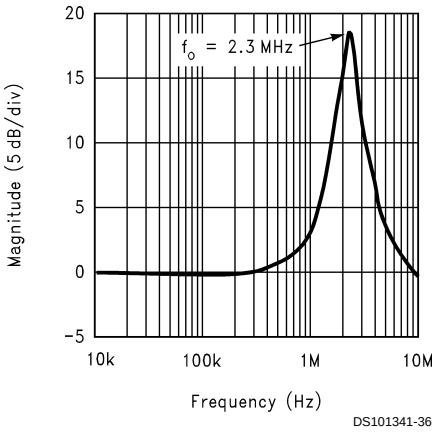
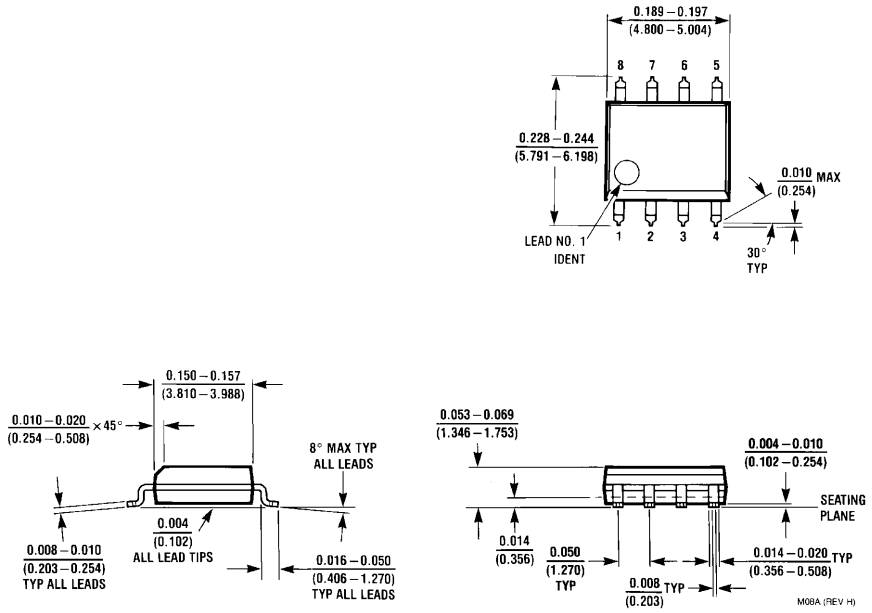


FIGURE 8.

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin SOIC
NS Package Number M08A

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