CGS74LCT2524 1 to 4 Minimum Skew (300 ps) 3V Clock Driver

Check for Samples: CGS74LCT2524

FEATURES

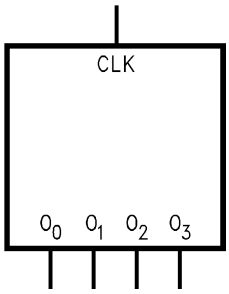
- **Ideal for Low Power/Low Noise High Speed Applications**
- **Ensured:**
  - **300 ps Pin-to-Pin Skew (t_{OSHL} and t_{OSLH})**
- **Implemented on Texas Instruments' FACT® Family Process**
- **1 Input to 4 Outputs Low Skew Clock Distribution**
- **Symmetric Output Current Drive: 12 mA I_{OH}/I_{OL}**
- **Industrial Temperature of −40°C to +85°C**
- **8-Pin SOIC Package**
- **Low Dynamic Power Consumption Above 20 MHz**
- **Ensured 2 kV ESD Protection**

DESCRIPTION

This minimum skew clock driver is a 3V option of the current CGS74CT2524 Minimum Skew Clock Driver and is designed for Clock Generation and Support (CGS) applications operating at low voltage, high frequencies. This device ensures minimum output skew across the outputs of a given device.

Skew parameters are also provided as a means to measure duty cycle requirements as those found in high speed clocking systems. This minimum skew clock driver with one input driving four outputs, is specifically designed for signal generation and clock distribution applications.

LOGIC SYMBOL



The output pins act as a single entity and will follow the state of the CLK when the clock distribution chip is selected.

PIN DESCRIPTION

Pin Names	Description
CLK	Clock Input
O_0–O_3	Outputs

TRUTH TABLE(1)

Inputs CLK	Outputs O_0–O_3
L	L
H	H

(1) L = Low Logic Level
H = High Logic Level

CONNECTION DIAGRAMS

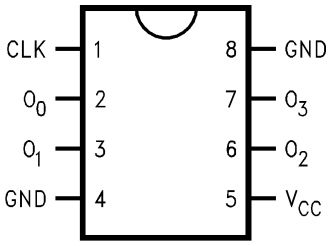


Figure 1. 8-Pin SOIC
See D Package

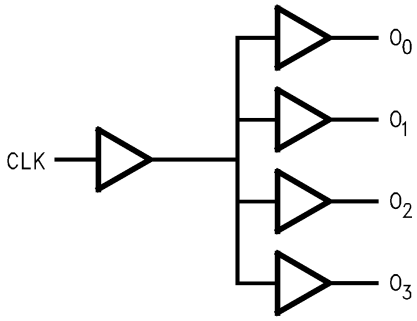


Figure 2.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Supply Voltage (V_{CC})				−0.5V to 7.0V
DC Input Voltage Diode Current (I_{IK})	V = −0.5V			−20 mA
	V = V_{CC} + 0.5V			+20 mA
DC Input Voltage (V_I)				−0.5V to V_{CC} +0.5V
DC Output Diode Current (I_O)	V = −0.5V			−20 mA
	V = V_{CC} + 0.5V			+20 mA
DC Output Voltage (V_O)				−0.5V to V_{CC} +0.5V
DC Output Source or Sink Current (I_O)				±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})				±50 mA
Storage Temperature (T_{STG})				−65°C to +150°C
Junction Temperature (θ_{JA})		**Min**	**Typ**	**Max**
	Airflow	0	225	500 LFM
	M	167	132	117 °C/W

(1) The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. The device should not be operated at these limits. The parametric values defined in the DC ELECTRICAL CHARACTERISTICS and AC ELECTRICAL CHARACTERISTICS tables are not ensured at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage (V_{CC})		3.0V to 3.6V
Input Voltage (V_{IN})		0V to V_{CC}
Output Voltage (V_O)		0V to V_{CC}
Operating Temperature (T_A)	Industrial	−40°C to +85°C
	Commercial	0°C to +70°C
Input Rise and Fall Times	(0.8V to 2.0V)	9.6 ns max

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions unless specified otherwise.

Symbol	Parameter	Conditions	V_{CC} (V)	CGS74LCT2524			Units
				T_A = +25°C	T_A = −40°C to +85°C		
				Typ	Ensured Limits		
V_{IH}	Minimum High Level Input Voltage	V_{OUT} = 0.1V or V_{CC}−0.1V	3.6	1.5	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage	V_{OUT} = 0.1V or V_{CC}−0.1V	3.6	1.5	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IL} or V_{IH}, I_{OUT} = −50 µA	3.0		2.9	2.9	V
		V_{IN} = V_{IL} or V_{IH}, I_{OH} = −12 mA	3.0		2.5	2.4	V
V_{OL}	Minimum Low Level Output Voltage	V_{IN} = V_{IL} or V_{IH}, I_{OUT} = 50 µA	3.0		0.1	0.1	V
		V_{IN} = V_{IL} or V_{IH}, I_{OL} = −12 mA	3.0		0.3	0.4	V
I_{IN}	Maximum Input Leakage Current	V_{IN} = V_{CC}, GND	3.6		±0.1	±1.0	µA
I_{CCT}	Maximum I_{CC}/Input	V_{IN} = 3.0V	3.6			100	µA
I_{OLD}	Minimum Dynamic Output Current	V_{OLD} = 0.8V (max)	3.6			36	mA
I_{OHD}		V_{OHD} = 2.0V (min)	3.6			−25	mA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	3.6		2.5	10	µA

AC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions unless specified otherwise. All typical values are measured at V_{CC} = 3.3V, T_A = 25°C

Symbol	Parameter	LCT2524			Units
		V_{CC} = 3.0V to 3.6V T_A = −40°C to +85°C C_L = 50 pF, R_L = 500Ω			
		Min	Typ	Max	
t_{PLH}	Low-to-High Propagation Delay CLK to O_n	6		15.0	ns
t_{PHL}	High-to-Low Propagation Delay CLK to O_n	6		15.0	ns

AC ELECTRICAL CHARACTERISTICS - EXTENDED

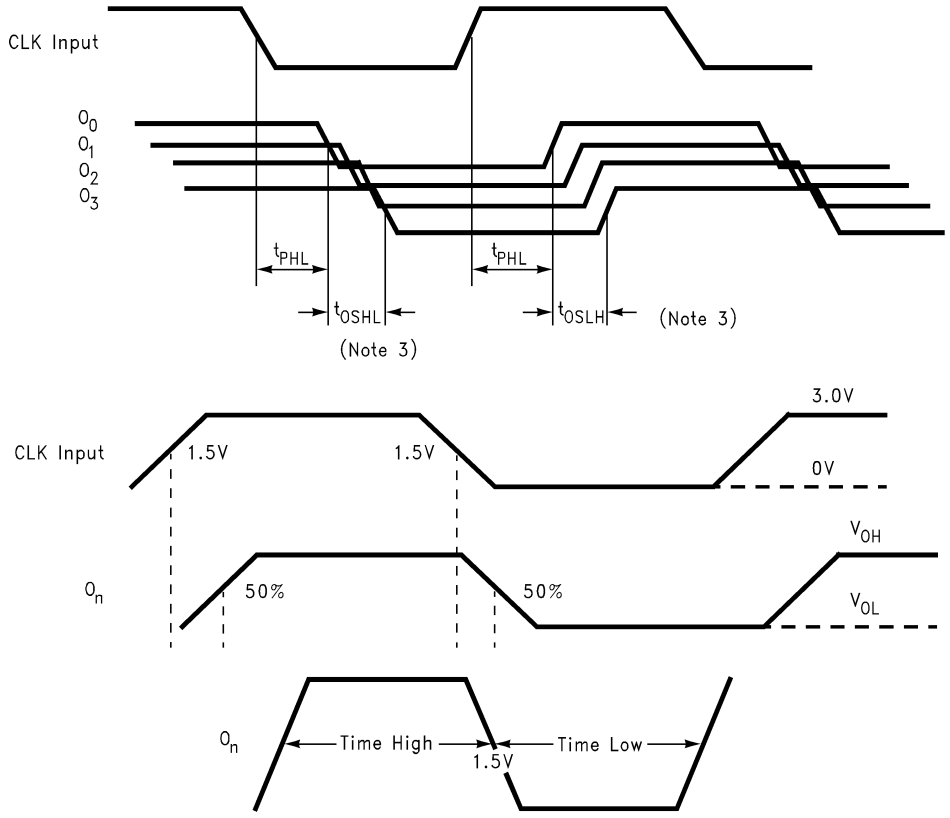
Over recommended operating conditions unless specified otherwise. All typical values are measured at V_{CC} = 3.3V, T_A = 25°C

Symbol	Parameter	LCT2524 V_{CC} = 3.0V to 3.6V T_A = −40°C to +85°C C_L = 50 pF, R_L = 500Ω			Units
		Min	Typ	Max	
f_{max}	Maximum Operating Frequency		75		MHz
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation(1)			300	ps
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation(1)			300	ps
t_{PS}	Maximum Skew Pin (Signal) Transition Variation(2)			2.5	ns
t_{RISE}/ t_{FALL}	Rise Time/Fall Time (from 0.8V to 2.0V/2.0V to 0.8V)			2.5	ns
T_{HIGH}	Time High	4			ns
T_{LOW}	Time Low	4			ns

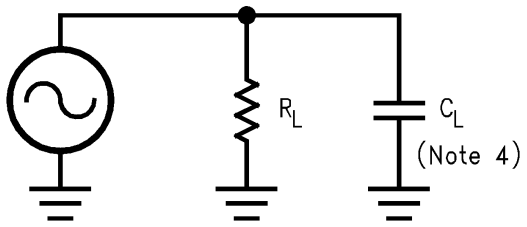
(1) Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}). Limits are characterized and ensured by design @ 66 MHz.

(2) Pin transition skew is the absolute difference between HIGH-to-LOW and LOW-to-HIGH propagation delay, measured at a given output pin.

TIMING DIAGRAMS



TEST CIRCUIT



R_L is 500Ω
C_L is 50 pF for all propagation delays and skew measurements.

REVISION HISTORY

Changes from Revision C (April 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	5

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