LVDS 18-Bit Color Flat Panel Display (FPD) Link

Check for Samples: DS90CF561, DS90CF562

FEATURES

- **Up to 105 Megabyte/sec Bandwidth**
- **Narrow Bus Reduces Cable Size and Cost**
- **290 mV Swing LVDS Devices for Low EMI**
- **Low Power CMOS Design**
- **Power Down Mode**
- **PLL Requires No External Components**
- **Low Profile 48-Lead TSSOP Package**
- **Falling Edge Data Strobe**
- **Compatible with TIA/EIA-644 LVDS Standard**

DESCRIPTION

The DS90CF561 transmitter converts 21 bits of CMOS/TTL data into three LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fourth LVDS link. Every cycle of the transmit clock 21 bits of input data are sampled and transmitted. The DS90CF562 receiver converts the LVDS data streams back into 21 bits of CMOS/TTL data. At a transmit clock frequency of 40 MHz, 18 bits of RGB data and 3 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY) are transmitted at a rate of 280 Mbps per LVDS data channel. Using a 40 MHz clock, the data throughput is 105 Megabytes per second. These devices are offered with falling edge data strobes for convenient interface with a variety of graphics and LCD panel controllers.

This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

Block Diagrams

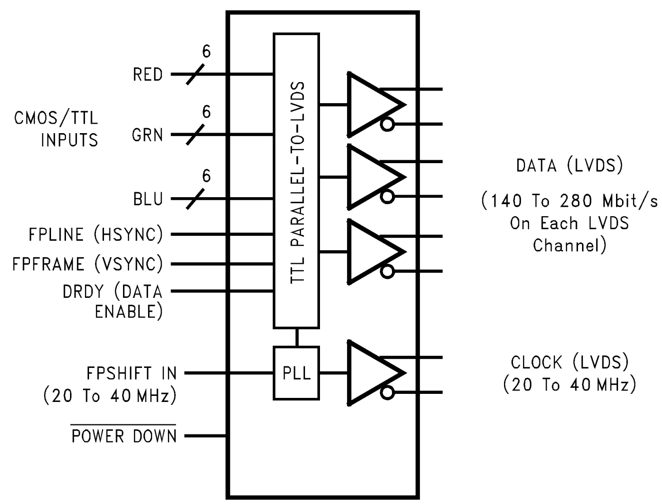

Figure 1. DS90CF561
See Package Number DGG0048A

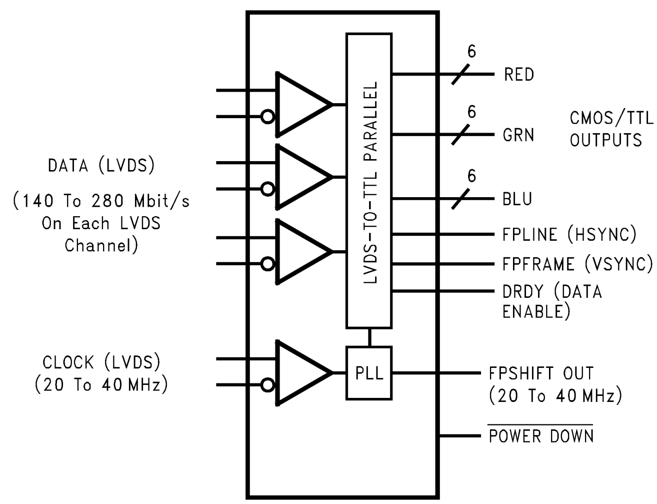

Figure 2. DS90CF562
See Package Number DGG0048A

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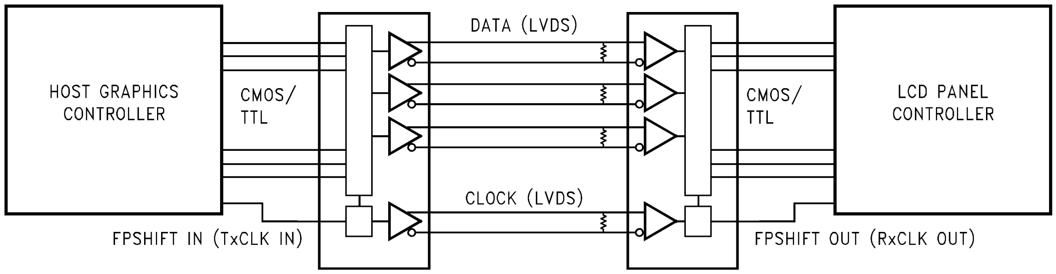


Figure 3. Application

Connection Diagrams

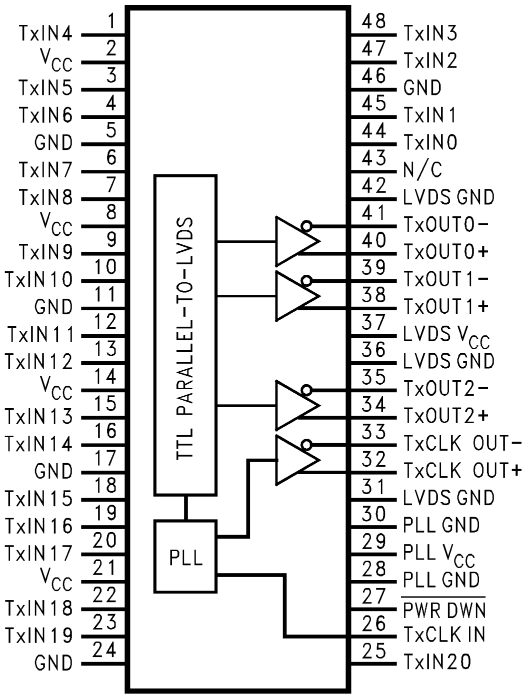


Figure 4. DS90CF561

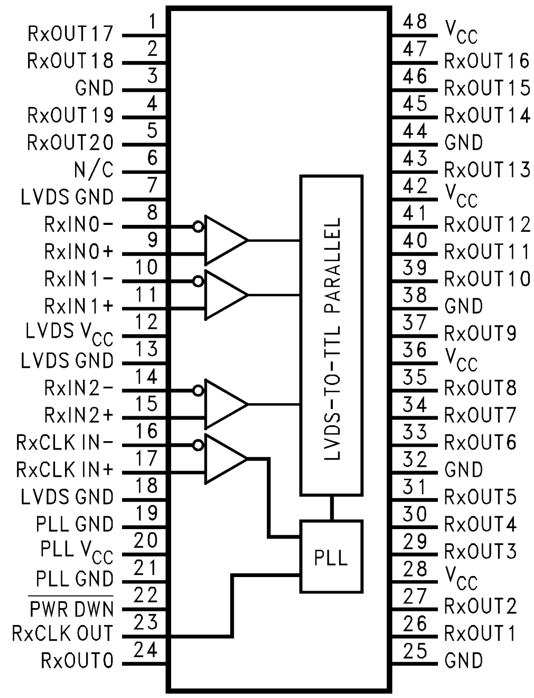


Figure 5. DS90CF562

Absolute Maximum Ratings [1][2][3]

	Value
Supply Voltage (V_{CC})	−0.3 to +6V
CMOS/TTL Input Voltage	−0.3 to (V_{CC} + 0.3V)
CMOS/TTL Ouput Voltage	−0.3 to (V_{CC} + 0.3V)
LVDS Receiver Input Voltage	−0.3 to (V_{CC} + 0.3V)
LVDS Driver Output Voltage	−0.3 to (V_{CC} + 0.3V)
LVDS Output Short Circuit Duration	continuous
Junction Temperature	+150°C
Storage Temperature Range	−65 to +150°C
Lead Temperature (Soldering, 4 sec.)	+260°C
Maximum Power Dissipation @ +25°C	
DGG0048A (TSSOP) Package:	
DS90CF561	1.98W
DS90CF562	1.89W
Package Derating:	
DS90CF561	16 mW/°C above +25°C
DS90CF562	15 mW/°C above +25°C
This device does not meet 2000V ESD rating [4].	

(1) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(2) “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be verified. They are not meant to imply that the device should be operated at these limits. The “Electrical Characteristics” specify conditions for device operation.
(3) Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).
(4) ESD Rating: HBM (1.5 kΩ, 100 pF) PLL V_{CC} ≥ 1000V All other pins ≥ 2000V EIAJ (0Ω, 200 pF) ≥ 150V

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Operating Free Air Temperature (T_A)	−10	+25	+70	°C
Receiver Input Range	0		2.4	V
Supply Noise Voltage (V_{CC})			100	mV_{P-P}

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Units
CMOS/TTL DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA	3.8	4.9		V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA		0.1	0.3	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA		−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = V_{CC}, GND, 2.5V or 0.4V		±5.1	±10	μA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V			−120	mA

(1) Typical values are given for V_{CC} = 5.0V and T_A = +25°C.

Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ[(1)]	Max	Units
LVDS DRIVER DC SPECIFICATIONS							
V_{OD}	Differential Output Voltage	$R_L = 100\Omega$		250	290	450	mV
ΔV_{OD}	Change in V_{OD} between					35	mV
	Complimentary Output States						
V_{CM}	Common Mode Voltage			1.1	1.25	1.375	V
ΔV_{CM}	Change in V_{CM} between					35	mV
	Complimentary Output States						
V_{OH}	High Level Output Voltage				1.3	1.6	V
V_{OL}	Low Level Output Voltage			0.9	1.01		V
I_{OS}	Output Short Circuit Current	$V_{OUT} = 0V$, $R_L = 100\Omega$			−2.9	−5	mA
I_{OZ}	Output TRI-STATE®™ Current	$\overline{\text{Power Down}} = 0V$, $V_{OUT} = 0V$ or V_{CC}			±1	±10	µA
LVDS RECEIVER DC SPECIFICATIONS							
V_{TH}	Differential Input High Threshold	$V_{CM} = +1.2V$				+100	mV
V_{TL}	Differential Input Low Threshold			−100			mV
I_{IN}	Input Current	$V_{IN} = +2.4V$	$V_{CC} = 5.5V$			±10	µA
		$V_{IN} = 0V$				±10	µA
TRANSMITTER SUPPLY CURRENT							
I_{CCTW}	Transmitter Supply Current, Worst Case	$R_L = 100\Omega$, $C_L = 5$ pF, Worst Case Pattern (See Figure 6, Figure 8)	f = 32.5 MHz		34	51	mA
			f = 37.5 MHz		36	53	mA
I_{CCTG}	Transmitter Supply Current, 16 Grayscale	$R_L = 100\Omega$, $C_L = 5$ pF, Grayscale Pattern (See Figure 7, Figure 8)	f = 32.5 MHz		27	47	mA
			f = 37.5 MHz		28	48	mA
I_{CCTZ}	Transmitter Supply Current, Power Down	$\overline{\text{Power Down}}$ = Low			1	25	µA
RECEIVER SUPPLY CURRENT							
I_{CCRW}	Receiver Supply Current, Worst Case	$C_L = 8$ pF, Worst Case Pattern (See Figure 6, Figure 9)	f = 32.5 MHz		55	75	mA
			f = 37.5 MHz		60	80	mA
I_{CCRG}	Receiver Supply Current, 16 Grayscale	$C_L = 8$ pF, 16 Grayscale Pattern See (Figure 7, Figure 9)	f = 32.5 MHz		35	55	mA
			f = 37.5 MHz		37	58	mA
I_{CCRZ}	Receiver Supply Current, Power Down	$\overline{\text{Power Down}}$ = Low			1	10	µA

Transmitter Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units
LLHT	LVDS Low-to-High Transition Time (Figure 8)		0.75	1.5	ns
LHLT	LVDS High-to-Low Transition Time (Figure 8)		0.75	1.5	ns
TCIT	TxCLK IN Transition Time (Figure 10)			8	ns
TCCS	TxOUT Channel-to-Channel Skew [(1)] (Figure 11)			350	ps

(1) This limit based on bench characterization.

Transmitter Switching Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
TPPos0	Transmitter Output Pulse Position for Bit 0 (Figure 22)	f = 20 MHz	−200	150	350	ps
TPPos1	Transmitter Output Pulse Position for Bit 1		6.3	7.2	7.5	ns
TPPos2	Transmitter Output Pulse Position for Bit 2		12.8	13.6	14.6	ns
TPPos3	Transmitter Output Pulse Position for Bit 3		20	20.8	21.5	ns
TPPos4	Transmitter Output Pulse Position for Bit 4		27.2	28	28.5	ns
TPPos5	Transmitter Output Pulse Position for Bit 5		34.5	35.2	35.6	ns
TPPos6	Transmitter Output Pulse Position for Bit 6		42.2	42.6	42.9	ns
TPPos0	Transmitter Output Pulse Position for Bit 0 (Figure 21)	f = 40 MHz	−100	100	300	ps
TPPos1	Transmitter Output Pulse Position for Bit 1		2.9	3.3	3.9	ns
TPPos2	Transmitter Output Pulse Position for Bit 2		6.1	6.6	7.1	ns
TPPos3	Transmitter Output Pulse Position for Bit 3		9.7	10.2	10.7	ns
TPPos4	Transmitter Output Pulse Position for Bit 4		13	13.5	14.1	ns
TPPos5	Transmitter Output Pulse Position for Bit 5		17	17.4	17.8	ns
TPPos6	Transmitter Output Pulse Position for Bit 6		20.3	20.8	21.4	ns
TCIP	TxCLK IN Period (Figure 12)		25	T	50	ns
TCIH	TxCLK IN High Time (Figure 12)		0.35T	0.5T	0.65T	ns
TCIL	TxCLK IN Low Time (Figure 12)		0.35T	0.5T	0.65T	ns
TSTC	TxIN Setup to TxCLK IN (Figure 12)	f = 20 MHz	14			ns
		f = 40 MHz	8			ns
THTC	TxIN Hold to TxCLK IN (Figure 12)		2.5	2		ns
TCCD	TxCLK IN to TxCLK OUT Delay @ 25°C, V_{CC} = 5.0V (Figure 14)		5		9.7	ns
TPLLS	Transmitter Phase Lock Loop Set (Figure 16)				10	ms
TPDD	Transmitter Powerdown Delay (Figure 20)				100	ns

Receiver Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
CLHT	CMOS/TTL Low-to-High Transition Time (Figure 9)			3.5	6.5	ns
CHLT	CMOS/TTL High-to-Low Transition Time (Figure 9)			2.7	6.5	ns
RCOP	RxCLK OUT Period (Figure 13)		25	T	50	ns
RSKM	Receiver Skew Margin (1). V_{CC} = 5V, T_A = 25°C (Figure 23)	f = 20 MHz	1.1			ns
		f = 40 MHz	700			ps
RCOH	RxCLK OUT High Time (Figure 13)	f = 20 MHz	21.5			ns
		f = 40 MHz	10.5			ns
RCOL	RxCLK OUT Low Time (Figure 13)	f = 20 MHz	19			ns
		f = 40 MHz	6			ns
RSRC	RxOUT Setup to RxCLK OUT (Figure 13)	f = 20 MHz	14			ns
		f = 40 MHz	4.5			ns
RHRC	RxOUT Hold to RxCLK OUT (Figure 13)	f = 20 MHz	16			ns
		f = 40 MHz	6.5			ns
RCCD	RxCLK IN to RxCLK OUT Delay @ 25°C, V_{CC} = 5.0V (Figure 15)		7.6		11.9	ns
RPLLS	Receiver Phase Lock Loop Set (Figure 17)				10	ms
RPDD	Receiver Powerdown Delay (Figure 21)				1	μs

(1) Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account for transmitter output skew(TCCS) and the setup and hold time (internal data sampling window), allowing LVDS cable skew dependent on type/length and source clock(TxCLK IN) jitter. RSKM ≥ cable skew (type, length) + source clock jitter (cycle to cycle).

AC Timing Diagrams

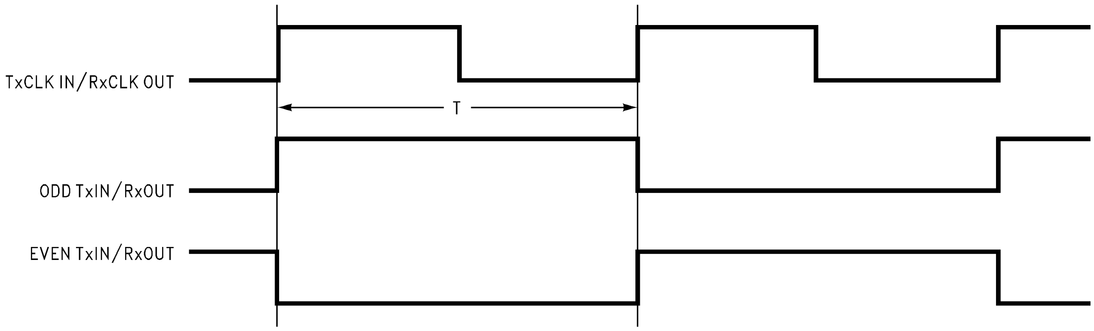
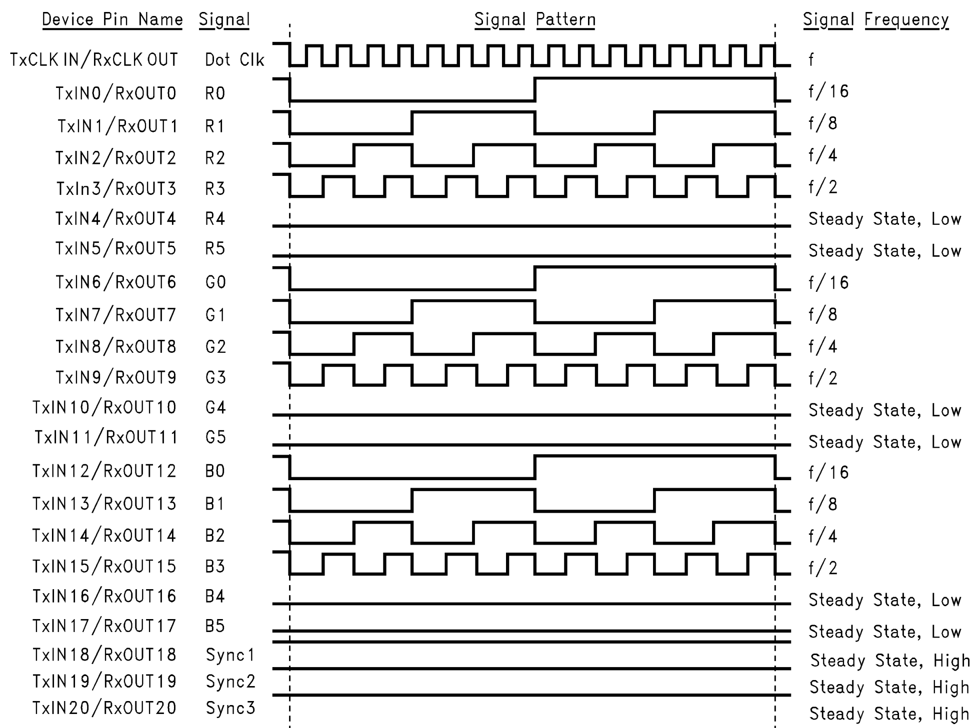


Figure 6. “Worst Case” Test Pattern



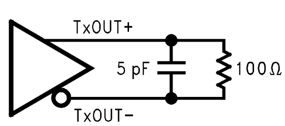
The worst case test pattern produces a maximum toggling of device digital circuitry, LVDS I/O and TTL I/O.

The 16 grayscale test pattern tests device power consumption for a “typical” LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

Figure 6 and Figure 7 show a falling edge data strobe (TxCLK IN/RxCLK OUT).

Recommended pin to signal mapping. Customer may choose to define differently.

Figure 7. “16 Grayscale” Test Pattern



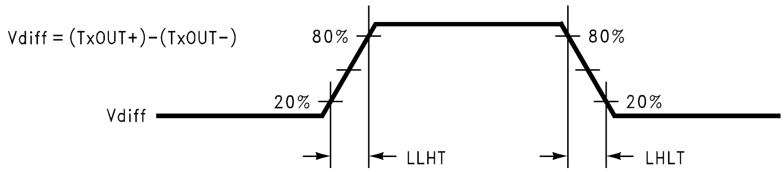


Figure 8. DS90CF561 (Transmitter) LVDS Output Load and Transition Timing

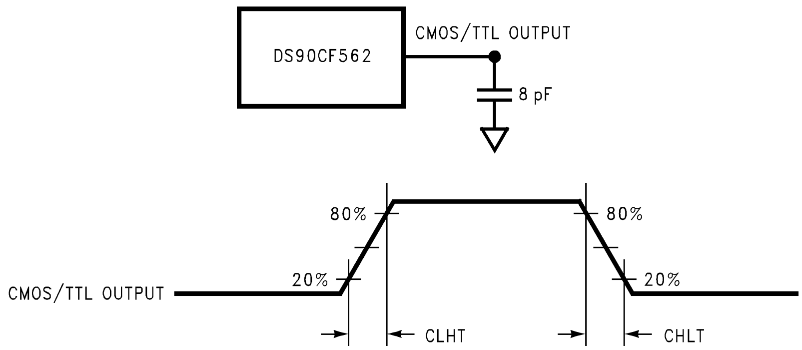


Figure 9. DS90CF562 (Receiver) CMOS/TTL Output Load and Transition Timing

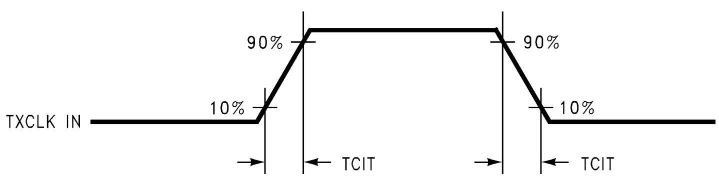
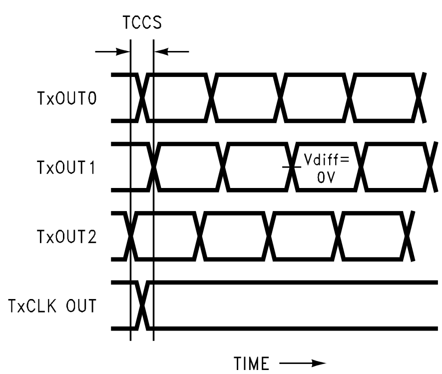


Figure 10. DS90CF561 (Transmitter) Input Clock Transition Time



Measurements at Vdiff = 0V
TCCS measured between earliest and latest initial LVDS edges.
TxCLK OUT Differential High→Low Edge for DS90CF561
TxCLK OUT Differential Low→High Edge for DS90CR561

Figure 11. DS90CF561 (Transmitter) Channel-to-Channel Skew and Pulse Width

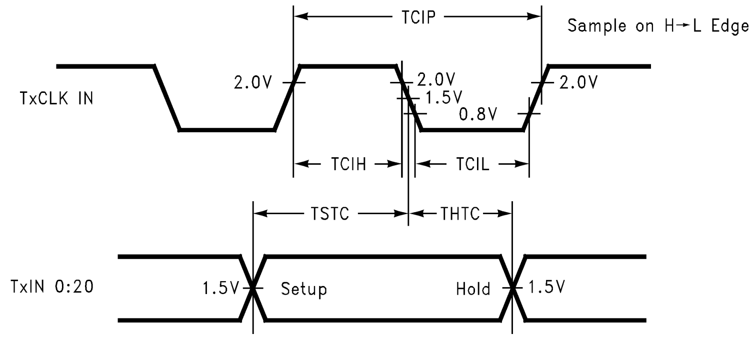


Figure 12. DS90CF561 (Transmitter) Setup/Hold and High/Low Times

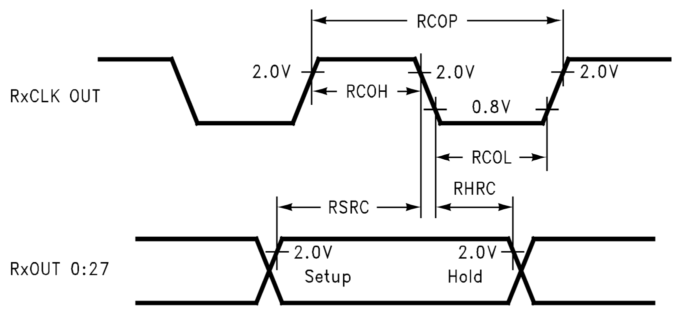


Figure 13. DS90CF562 (Receiver) Setup/Hold and High/Low Times

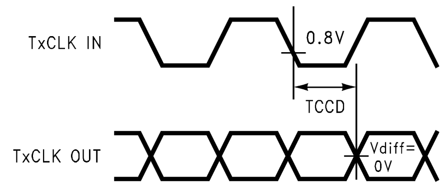


Figure 14. DS90CF561 (Transmitter) Clock In to Clock Out Delay

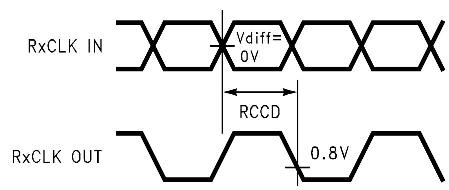


Figure 15. DS90CF562 (Receiver) Clock In to Clock Out Delay

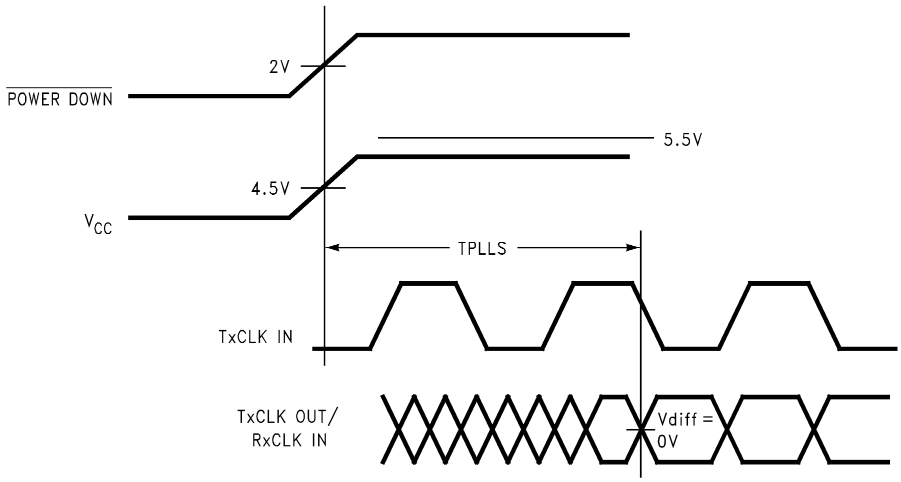


Figure 16. DS90CF561 (Transmitter) Phase Lock Loop Set Time

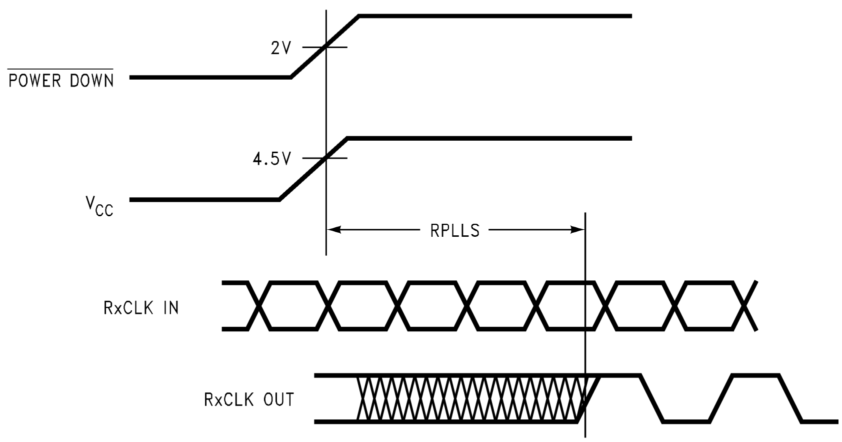


Figure 17. DS90CF562 (Receiver) Phase Lock Loop Set Time

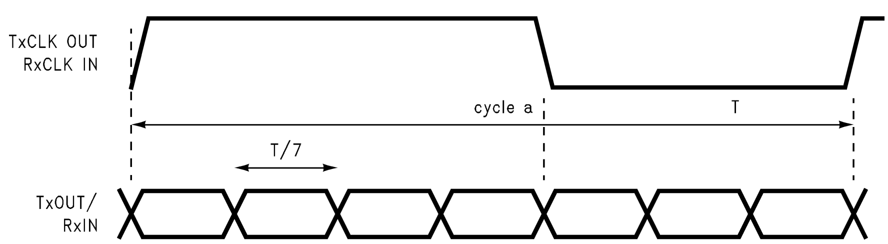


Figure 18. Seven Bits of LVDS in One Clock Cycle

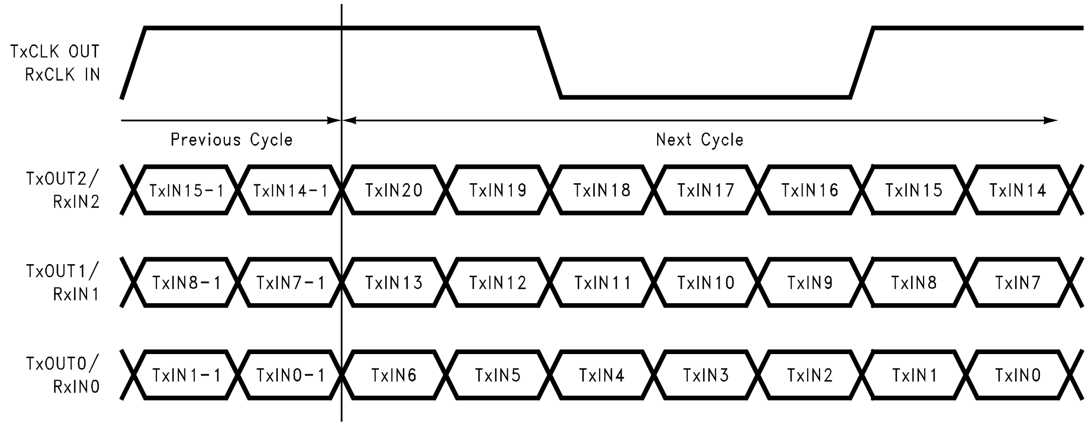


Figure 19. 21 Parallel TTL Data Inputs Mapped to LVDS Outputs (DS90CF561)

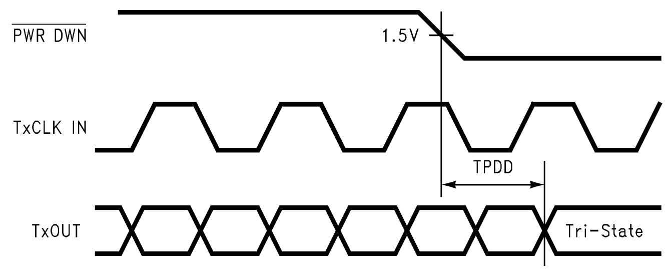


Figure 20. Transmitter Powerdown Delay

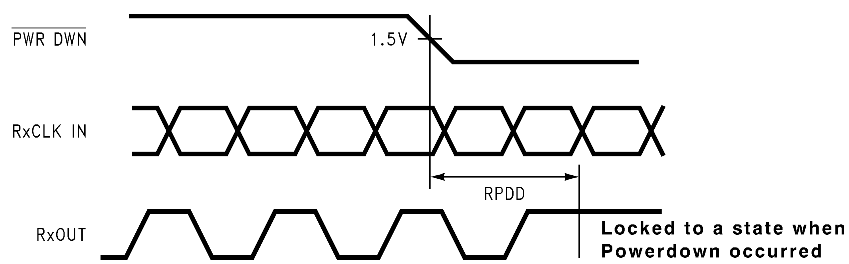


Figure 21. Receiver Powerdown Delay

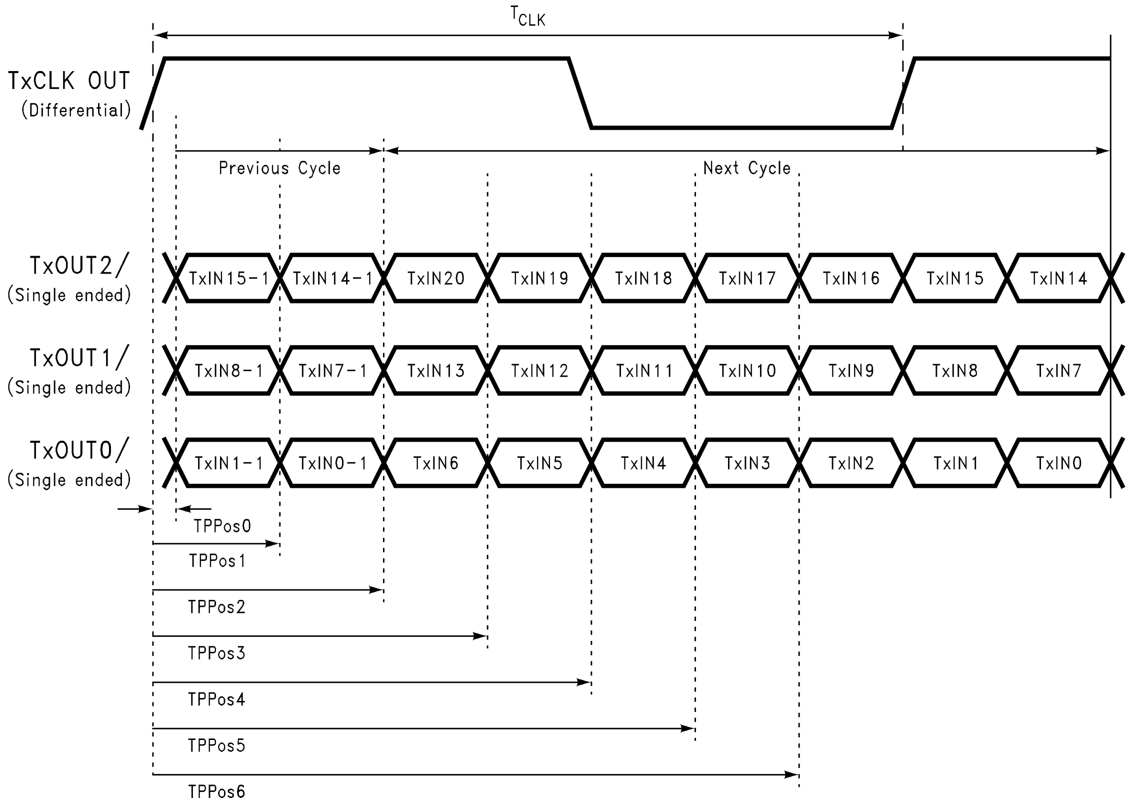
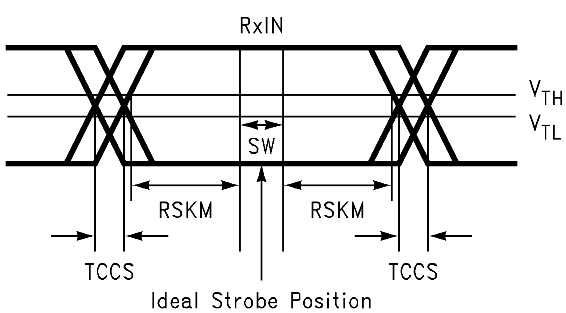


Figure 22. Transmitter LVDS Output Pulse Position Measurement



SW—Setup and Hold Time (Internal Data Sampling Window)
TCCS—Transmitter Output Skew
RSKM ≥ Cable Skew (Type, Length) + Source Clock Jitter (Cycle to Cycle)
Cable Skew—Typically 10 ps–40 ps per foot

Figure 23. Receiver LVDS Input Skew Margin

DS90CF561 PIN DESCRIPTION—FPD LINK TRANSMITTER

Pin Name	I/O	No.	Description
TxIN	I	21	TTL level input. This includes: 6 Red, 6 Green, 6 Blue, and 3 control lines (FPLINE, FPFRAME, DRDY). (Also referred to as HSYNC, VSYNC and DATA ENABLE.)
TxOUT+	O	3	Positive LVDS differential data output
TxOUT−	O	3	Negative LVDS differential data output
FPSHIFT IN	I	1	TTL level clock input. The falling edge acts as data strobe.
TxCLK OUT+	O	1	Positive LVDS differential clock output
TxCLK OUT−	O	1	Negative LVDS differential clock output

DS90CF561 PIN DESCRIPTION—FPD LINK TRANSMITTER (continued)

Pin Name	I/O	No.	Description
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down.
V_{CC}	I	4	Power supply pins for TTL inputs
GND	I	5	Ground pins for TTL inputs
PLL V_{CC}	I	1	Power supply pin for PLL
PLL GND	I	2	Ground pins for PLL
LVDS V_{CC}	I	1	Power supply pin for LVDS outputs
LVDS GND	I	3	Ground pins for LVDS outputs

DS90CF562 PIN DESCRIPTION—FPD LINK RECEIVER

Pin Name	I/O	No.	Description
RxIN+	I	3	Positive LVDS differential data inputs
RxIN−	I	3	Negative LVDS differential data inputs
RxOUT	O	21	TTL level data outputs. This includes: 6 Red, 6 Green, 6 Blue, and 3 control lines (FPLINE, FPFRAME, DRDY). (Also referred to as HSYNC, VSYNC and DATA ENABLE.)
RxCLK IN+	I	1	Positive LVDS differential clock input
RxCLK IN−	I	1	Negative LVDS differential clock input
FPSHIFT OUT	O	1	TTL level clock output. The falling edge acts as data strobe.
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) maintains the receiver outputs in the previous state
V_{CC}	I	4	Power supply pins for TTL outputs
GND	I	5	Ground pins for TTL outputs
PLL V_{CC}	I	1	Power supply for PLL
PLL GND	I	2	Ground pin for PLL
LVDS V_{CC}	I	1	Power supply pin for LVDS inputs
LVDS GND	I	3	Ground pins for LVDS inputs

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	12