CLC416

CLC416 Dual, Low Cost, Low Power, 120 MHz Op Amp

Literature Number: SNOS817

September 1998

National Semiconductor

CLC416
Dual Low-Power, 120MHz Op Amp

General Description

The CLC416 is a dual, wideband (120MHz) op amp. The CLC416 consumes only 39mW per channel and can source or sink an output current of 60mA. These features make the CLC416 a versatile, high-speed solution for demanding applications that are sensitive to both power and cost.

Utilizing National's proven architectures, this dual current feedback amplifier surpasses the performance of alternative solutions and sets new standards for low power. This power-conserving dual op amp achieves low distortion with -80dBc and -80dBc second and third harmonics respectively. Many high source impedance applications will benefit from the CLC416's 6MΩ input impedance. And finally, designers will have a bipolar part with an exceptionally low 100nA non-inverting bias current.

With 0.1dB flatness to 30MHz and low differential gain and phase errors, the CLC416 is an ideal part for professional video processing and distribution. The 120MHz -3dB bandwidth (A_v = +2) coupled with a 400V/μs slew rate also makes the CLC416 a perfect choice in cost-sensitive applications such as video monitors, fax machines, copiers, and CATV systems.

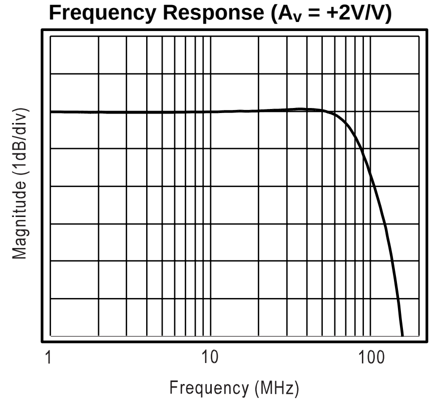
Features

- 0.01%, 0.03° D_G, Dϕ
- Very low input bias current: 100nA
- High input impedance: 6MΩ
- 120MHz -3dB bandwidth (A_v = +2)
- Low power
- High output current: 60mA
- Low-cost

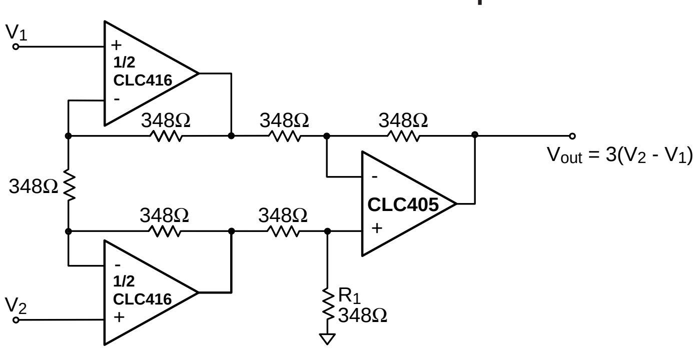
Applications

- Desktop video systems
- Video distribution
- Flash A/D driver
- High-speed driver
- High-source impedance applications
- Professional video processing
- High resolution monitors

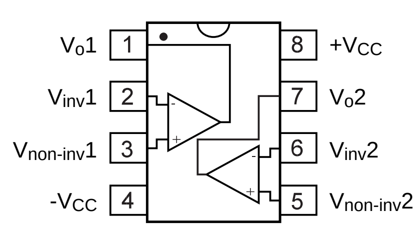
Frequency Response (A_v = +2V/V)



Typical Application Diagram
Instrumentation Amplifier



Pinout
DIP & SOIC



CLC416 Electrical Characteristics (A_V = +2, R_f = 348Ω: V_{cc} = ± 5V, R_L = 100Ω unless specified)

PARAMETERS	CONDITIONS	TYP	MIN/MAX RATINGS			UNITS	NOTES
Ambient Temperature	CLC416AJ	+25°C	+25°C	0 to 70°C	-40 to 85°C		
FREQUENCY DOMAIN RESPONSE							
-3dB bandwidth	V_{out} < 1.0V_{pp}	120	65	45	45	MHz	
	V_{out} < 5.0V_{pp}	52	40	36	35	MHz	1
±0.1dB bandwidth	V_{out} < 1.0V_{pp}	30	15			MHz	
gain flatness	V_{out} < 1.0V_{pp}						
peaking	DC to 200MHz	0.1	0.7	0.8	1.0	dB	
rolloff	<30MHz	0	0.3	0.6	0.6	dB	
linear phase deviation	<20MHz	0.3	0.6	0.7	0.7	deg	
differential gain	4.43MHz, R_L=150Ω	0.01	0.04	0.04	0.04	%	
differential phase	4.43MHz, R_L=150Ω	0.03	0.08	0.11	0.12	deg	
TIME DOMAIN RESPONSE							
rise and fall time	2V step	4.3	6.5	7.2	7.4	ns	
settling time to 0.05%	2V step	22	30	38	41	ns	
overshoot	2V step	3	12	12	12	%	
slew rate A_V = +2	2V step	400	300	260	250	V/µs	
A_V = -1	1V step	700				V/µs	
DISTORTION AND NOISE RESPONSE							
2nd harmonic distortion	2V_{pp}, 1MHz	-80				dBc	
3rd harmonic distortion	2V_{pp}, 1MHz	-80				dBc	
2nd harmonic distortion	2V_{pp}, 10MHz	-65	-55	-50	-47	dBc	
3rd harmonic distortion	2V_{pp}, 10MHz	-57	-50	-45	-45	dBc	
equivalent input noise							
voltage	>1MHz	5	6.3	6.6	6.7	nV/√Hz	
inverting current	>1MHz	12	15	16	17	pA/√Hz	
non-inverting current	>1MHz	3	3.8	4.0	4.2	pA/√Hz	
crosstalk, input referred	2V_{pp}, 10MHz	72	66	66	66	dB	
STATIC DC PERFORMANCE							
input offset voltage		1	5	7	8	mV	A
average drift		30		50	50	µV/°C	
input bias current	non-inverting	100	900	1600	2800	nA	A
average drift		3		8	11	nA/°C	
input bias current	inverting	1	5	6	8	µA	A
average drift		17		40	45	nA/°C	
power supply rejection ratio	DC	52	47	47	45	dB	
common-mode rejection ratio	DC	50	45	45	43	dB	
supply current per channel	R_L= ∞	3.9	4.5	4.6	4.9	mA	A
MISCELLANEOUS PERFORMANCE							
input resistance	non-inverting	6	3	2.4	1	MΩ	
input capacitance	non-inverting	1	2	2	2	pF	
common mode input range		±2.2	±1.8	±1.7	±1.5	V	
output voltage range	R_L = 100Ω	+3.5,-2.9	+3.1/-2.8	+2.9/-2.7	+2.4/-1.7	V	
output voltage range	R_L = ∞	+4.0,-3.4	+3.9/-3.3	+3.8/-3.2	+3.7/-2.8	V	
output current		60	44	38	20	mA	
output resistance, closed loop		0.06	0.2	0.25	0.4	Ω	

Recommended gain range ±1 to ±40V/V

Transistor count = 110

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

supply voltage	±7V
I_{out} is short circuit protected to ground	
common-mode input voltage	±Vcc
maximum junction temperature	+175°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+300°C
ESD rating (human body model)	1000V

Notes

1) At temps < 0°C, spec is guaranteed for R_L = 500Ω.
A) J-level: spec is 100% tested at +25°C.

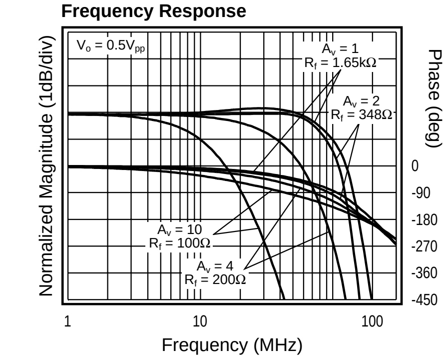
Ordering Information

Model	Temperature Range	Description
CLC416AJP	-40°C to +85°C	8-pin PDIP
CLC416AJE	-40°C to +85°C	8-pin SOIC

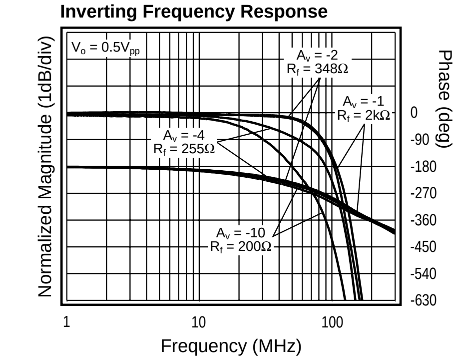
Package Thermal Resistance

Package	θ_{JC}	θ_{JA}
Plastic (AJP)	80°C/W	95°C/W
Surface Mount (AJE)	95°C/W	115°C/W

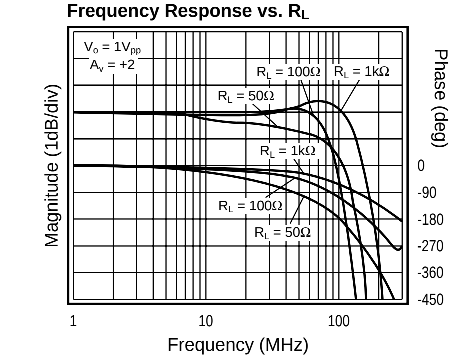
Frequency Response



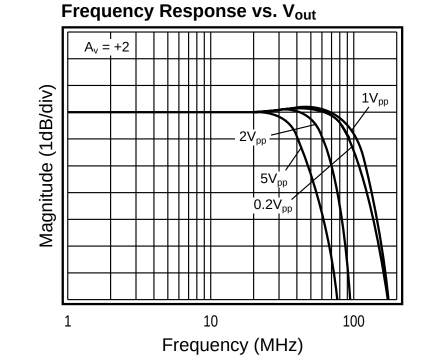
Inverting Frequency Response



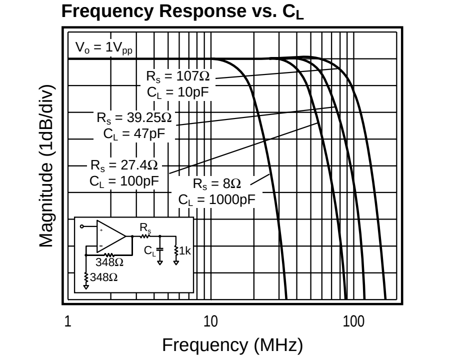
Frequency Response vs. R_L



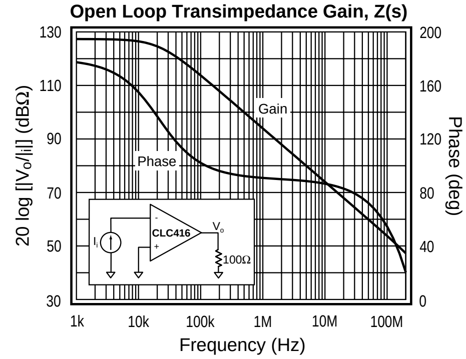
Frequency Response vs. V_{out}



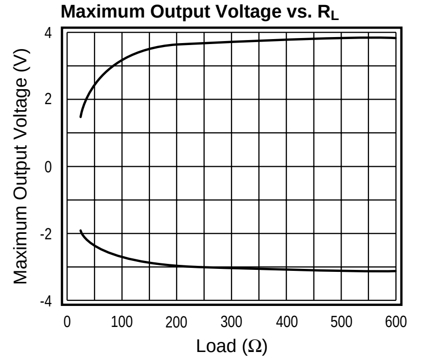
Frequency Response vs. C_L



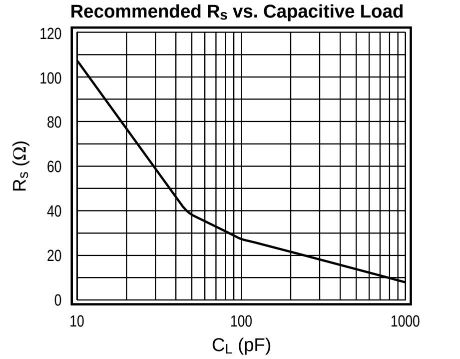
Open Loop Transimpedance Gain, Z(s)



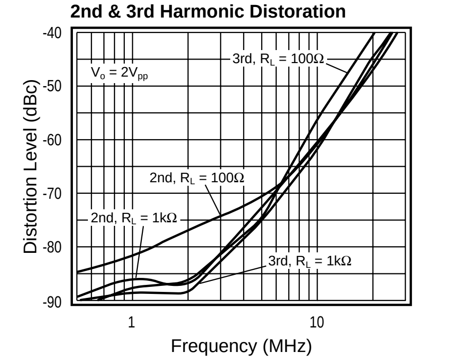
Maximum Output Voltage vs. R_L



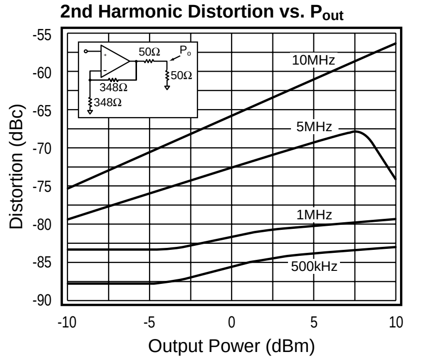
Recommended R_S vs. Capacitive Load



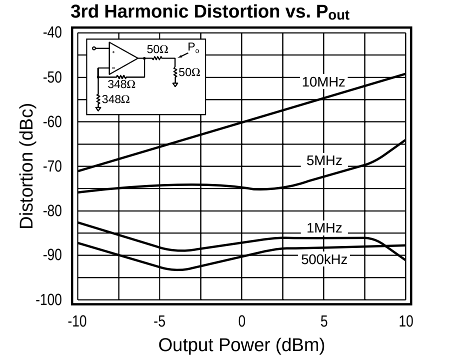
2nd & 3rd Harmonic Distoration



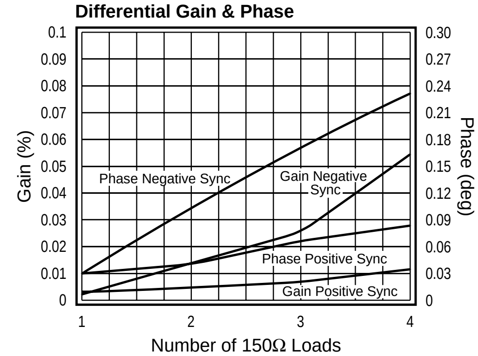
2nd Harmonic Distortion vs. P_{out}



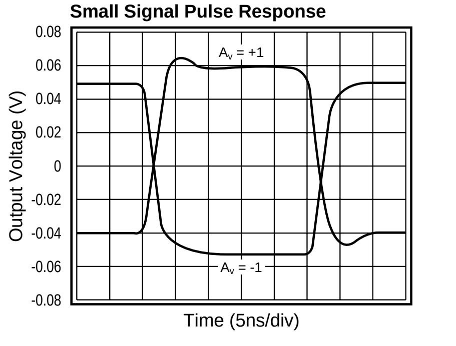
3rd Harmonic Distortion vs. P_{out}



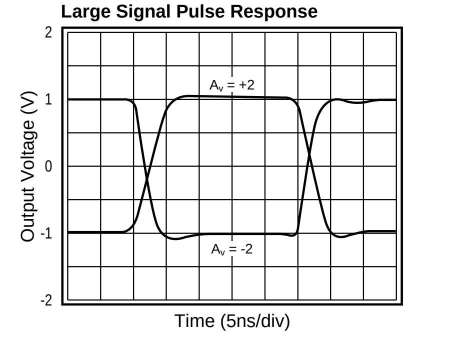
Differential Gain & Phase



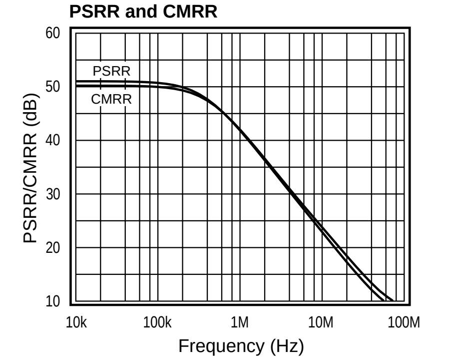
Small Signal Pulse Response



Large Signal Pulse Response

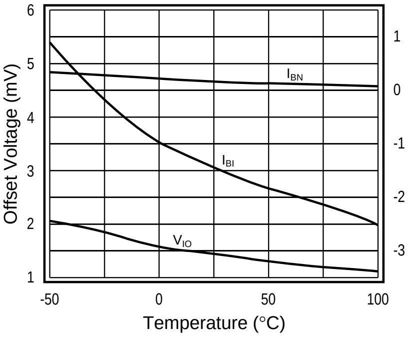


PSRR and CMRR

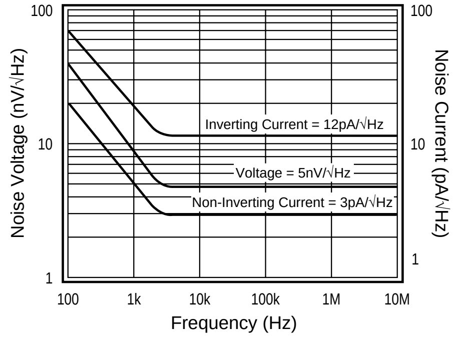


CLC416 Typical Performance Characteristics (V_{cc} = ±5V, A_v = +2, R_f = 348Ω, R_L = 100Ω; unless specified)

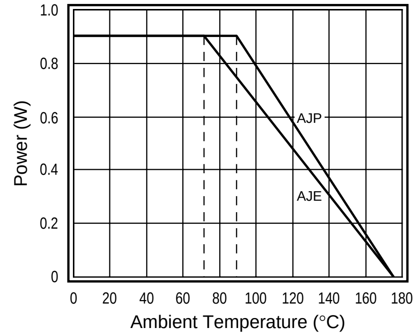
Typical DC Errors vs. Temperature



Equivalent Input Noise



Power Derating Curves



CLC416 OPERATION

Description

The CLC416 is a dual current feedback amplifier with the following features:

- Differential gain and phase errors of 0.01% and 0.03° into a 150Ω load
- Low, 3.9mA, supply current per amplifier

The professional video quality differential gain and phase errors and low power capabilities of the CLC416 make this product a good choice for video applications.

Gain

The non-inverting and inverting gain equations for the CLC416 are as follows:

Non-inverting Gain: $1+\frac{R_f}{R_g}$

Inverting Gain: $-\frac{R_f}{R_g}$

Where R_f is the feedback resistor and R_g is the gain setting resistor. Figure 1 shows the general non-inverting gain configuration including the recommended bypass capacitors.

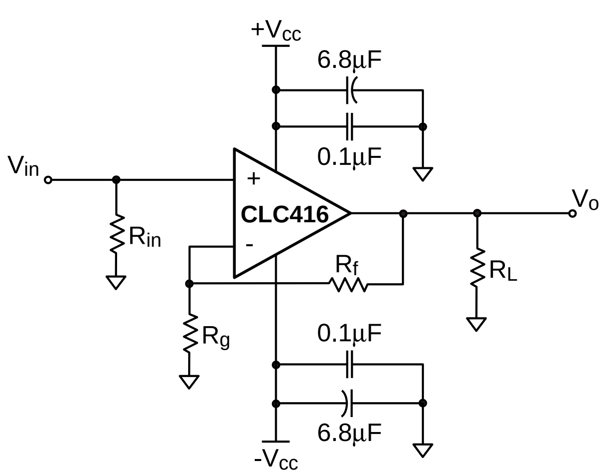


Figure 1: Recommended Non-Inverting Gain Circuit

Feedback Resistor Selection

The feedback resistor, R_f, determines the loop gain and frequency response of a current feedback amplifier. Optimum performance of the CLC416, at a gain of +2V/V, is achieved with R_f equal to 348Ω. The frequency response plots in the typical performance section illustrate the recommended R_f for several gains. Within limits, R_f can be adjusted to optimize the frequency response.

- Decrease R_f to peak frequency response and extend bandwidth
- Increase R_f to roll off frequency response and reduce bandwidth

As a rule of thumb, if the recommended R_f is doubled, the bandwidth will be cut in half.

Channel Matching

Channel matching and crosstalk efficiency are largely dependent on board layout. The layout of National's dual amplifier evaluation boards are designed to produce optimum channel matching and isolation. Typical channel matching for the CLC416 is shown in Figure 2.

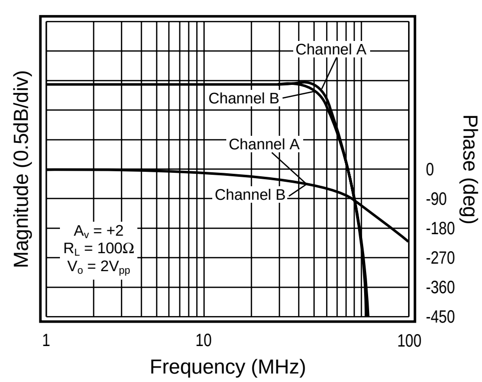


Figure 2: Channel Matching

The CLC416's channel-to-channel isolation is better than 70dB for input frequencies of 4MHz. Input referred crosstalk vs. frequency is illustrated in Figure 3.

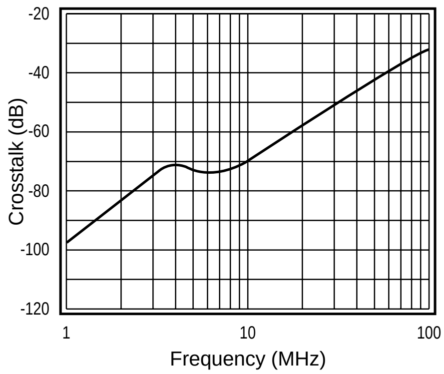


Figure 3: Input Referred Crosstalk vs. Frequency

Driving Cables and Capacitive Loads

When driving cables, double termination is used to prevent reflections. For capacitive load applications, a small series resistor at the output of the CLC416 will improve stability. The ***R_s vs. Capacitive Load*** plot, in the ***Typical Performance*** section, gives the recommended series resistance value for optimum flatness at various capacitive loads.

Power Dissipation

The power dissipation of an amplifier can be described in two conditions:

- Quiescent Power Dissipation - P_Q (No Load Condition)
- Total Power Dissipation - P_T (with Load Condition)

The following steps can be taken to determine the power consumption for each CLC416 amplifier:

1. Determine the quiescent power $P_Q = I_{cc} (V_{CC} - V_{EE})$
2. Determine the RMS power at the output stage $P_O = (V_{cc} - V_{load}) (I_{load})$, where V_{load} and I_{load} are the RMS voltage and current across the external load.
3. Determine the total RMS power $P_T = P_Q + P_O$

Add the total RMS powers for both channels to determine the power dissipated by the dual.

The maximum power that the package can dissipate at a given temperature is illustrated in the ***Power Derating*** curves in the ***Typical Performance*** section. The power derating curve for any package can be derived by utilizing the following equation:

$$P = \frac{(175° - Tamb)}{\theta_{JA}}$$

where: T_{amb} = Ambient temperature (°C)
θ_{JA} = Thermal resistance, from junction to ambient, for a given package (°C/W)

Layout Considerations

A proper printed circuit layout is essential for achieving high frequency performance. National provides evaluation boards for the CLC416 (CLC730038 - DIP, CLC730036 - SOIC) and suggests their use as a guide for high frequency layout and as an aid for device testing and characterization.

Supply bypassing is required for best performance. The bypass capacitors provide a low impedance return current path at the supply pins. They also provide high frequency filtering on the power supply traces. Other layout factors play a major role in high frequency performance. The following are recommended as a basis for high frequency layout:

1. Include 6.8µF tantalum and 0.1µF ceramic capacitors on both supplies.
2. Place the 6.8µF capacitors within 0.75 inches of the power pins.
3. Place the 0.1µF capacitors within 0.1 inches of the power pins.
4. Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance.
5. Minimize all trace lengths to reduce series inductances.

Additional information is included in the evaluation board literature.

SPICE Models

SPICE models provide a means to evaluate amplifier designs. Free SPICE models are available for National's monolithic amplifiers that:

- Support Berkeley SPICE 2G and its many derivatives
- Reproduce typical DC, AC, Transient, and Noise performance
- Support room temperature simulations

The ***readme*** file that accompanies the diskette lists released models, and provides a list of modeled parameters. The application note OA-18, Simulation SPICE Models for National's Op Amps, contains schematics and a reproduction of the ***readme*** file.

Applications Circuits

Instrumentation Amplifier

An instrumentation circuit is shown on the front page and reproduced in Figure 4. The DC CMRR can be fine tuned by adjusting R_1.

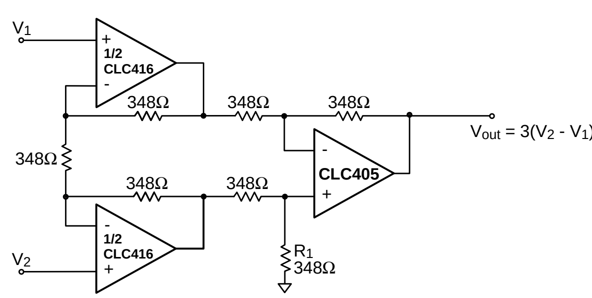


Figure 4: Instrumentation Amplifier

Differential Line Receiver

Figure 5 illustrates a Differential Line Receiver. The circuit will convert differential signals to single-ended signals.

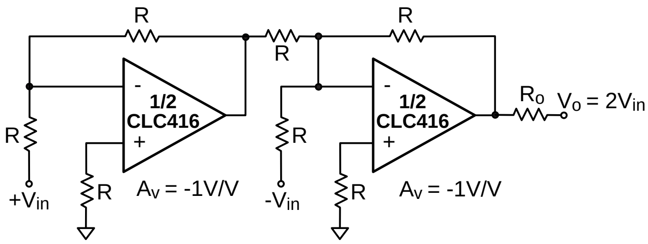


Figure 5: Differential Line Receiver

Bandpass Filter

Figure 6 illustrates a low-sensitivity bandpass filter and design equations. This topology utilizes the CLC416's closely matched amplifiers to obtain low op-amp sensitivity at high frequencies. The CLC405 is used as a buffer to obtain low output impedance. The overall circuit gain is unity. For additional gain, the CLC405 can be configured as a non-inverting amplifier.

To design the filter, choose C and then determine values for R and R_1 based on the desired resonant frequency (f_r) and Q factor.

Figure 7 illustrates a bandpass filter with Q = 10 and f_r = 1MHz. The component values used are listed below:

$R_1 = 4.9k\Omega$
$R = 499\Omega$
$C = 330pF$
$R_f = 2k\Omega$

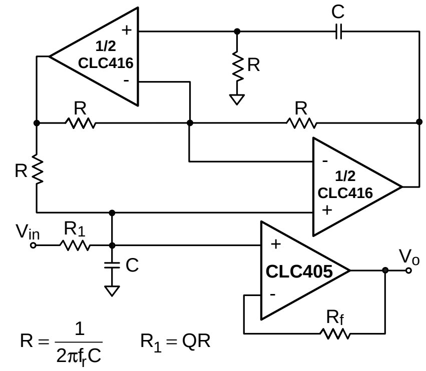


Figure 6: Bandpass Filter Topology

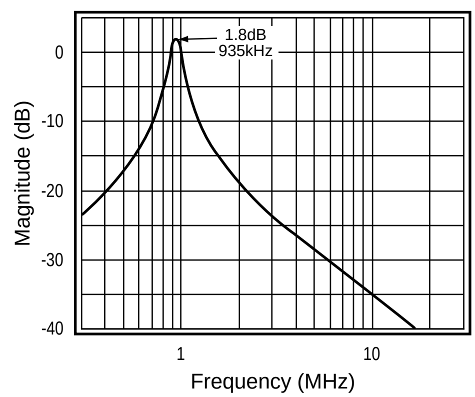


Figure 7: Bandpass Response

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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