

# CLC449

*CLC449 1.1GHz Ultra Wideband Monolithic Op Amp*



Literature Number: SNOS827B

# CLC449

## 1.1GHz Ultra Wideband Monolithic Op Amp

### General Description

The CLC449 is an ultra high speed monolithic op amp, with a typical  $-3\text{dB}$  bandwidth of  $1.1\text{GHz}$  at a gain of  $+2$ . This wideband op amp supports rise and fall times less than  $1\text{ns}$ , settling time of  $6\text{ns}$  (to  $0.2\%$ ) and slew rate of  $2500\text{V}/\mu\text{s}$ . The CLC449 achieves 2nd harmonic distortion of  $-68\text{dBc}$  at  $5\text{MHz}$  at a low supply current of only  $12\text{mA}$ . These performance advantages have been achieved through improvements in National's proven current feedback topology combined with a high speed complementary bipolar process.

The DC to  $1.2\text{GHz}$  bandwidth of the CLC449 is suitable for many IF and RF applications as a versatile op amp building block for replacement of AC coupled discrete designs. Operational amplifier functions such as active filters, gain blocks, differentiation, addition, subtraction and other signal conditioning functions take full advantage of the CLC449's unity-gain stable closed-loop performance.

The CLC449 performance provides greater headroom for lower frequency applications such as component video, high resolution workstation graphics, and LCD displays. The amplifier's  $0.1\text{dB}$  gain flatness to beyond  $200\text{MHz}$ , plus  $0.8\text{ns}$  ( $2\text{V}$  step) rise and fall times are ideal for improved time domain performance. In addition, the  $0.03\%/0.02^\circ$  differential gain/phase performance allows system flexibility for handling standard NTSC and PAL signals.

In applications using high speed flash A/D and D/A converters, the CLC449 provides the necessary wide bandwidth ( $1.1\text{GHz}$ ), settling ( $6\text{ns}$  to  $0.02\%$ ) and low distortion into  $50\Omega$  loads to improve SFDR.

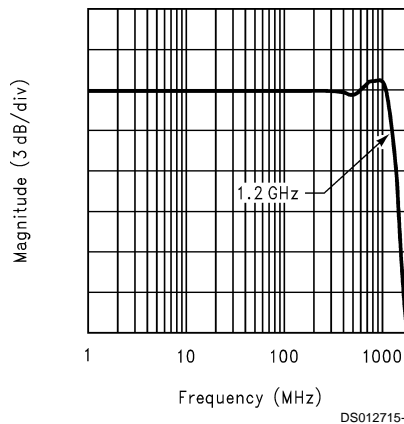
### Features

- $1.1\text{GHz}$  small-signal bandwidth ( $A_v = +2$ )
- $2500\text{V}/\mu\text{s}$  slew rate
- $0.03\%$ ,  $0.02^\circ$   $D_G$ ,  $D_\Phi$
- $6\text{ns}$  settling time to  $0.2\%$
- 3rd order intercept,  $30\text{dBm}$  @  $70\text{MHz}$
- Dual  $\pm 5\text{V}$  or single  $10\text{V}$  supply
- High output current:  $80\text{mA}$
- $2.5\text{dB}$  noise figure

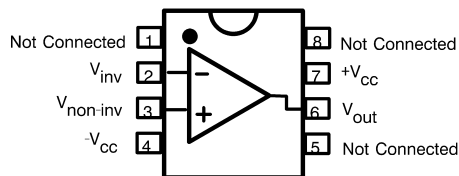
### Applications

- High performance RGB video
- RF/IF amplifier
- Instrumentation
- Medical electronics
- Active filters
- High speed A/D driver
- High speed D/A buffer

Frequency Response ( $A_v = +2\text{V/V}$ )



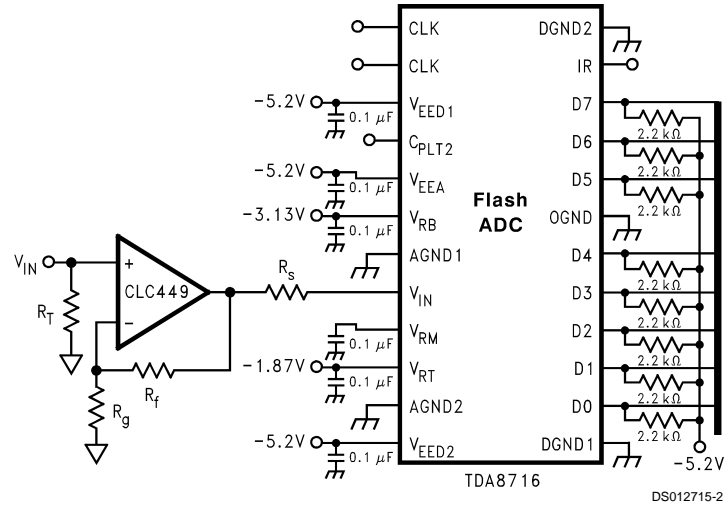
### Connection Diagram



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**Pinout  
DIP & SOIC**

## Typical Application



120MSPS High Speed Flash ADC Driver

## Ordering Information

Package	Temperature Range Industrial	Part Number	Package Marking	NSC Drawing
8-pin plastic DIP	-40°C to +85°C	CLC449AJP	CLC449AJP	N08E
8-pin plastic SOIC	-40°C to +85°C	CLC449AJE	CLC449AJE	M08A

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	$\pm 6V$
$I_{OUT}$ is short circuit protected to ground	
Common Mode Input Voltage	$\pm V_{CC}$
Maximum Junction Temperature	$+150^{\circ}C$
Operating Temperature Range	$-40^{\circ}C$ to $+85^{\circ}C$

Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$
Lead Solder Duration ( $+300^{\circ}C$ )	10 sec
ESD (human body model)	500V

**Operating Ratings**

Thermal Resistance		
Package	( $\theta_{JC}$ )	( $\theta_{JA}$ )
MDIP	$90^{\circ}C/W$	$105^{\circ}C/W$
SOIC	$110^{\circ}C/W$	$130^{\circ}C/W$

**Electrical Characteristics**

$A_V = +2$ ,  $V_{CC} = \pm 5V$ ,  $R_L = 100\Omega$ ,  $R_f = 250\Omega$ ; unless specified

Symbol	Parameter	Conditions	Typ	Min/Max (Note 2)			Units
	Ambient Temperature	CLC449AJ	$+25^{\circ}C$	$+25^{\circ}C$	0 to $70^{\circ}C$	$-40$ to $+85^{\circ}C$	
<b>Frequency Domain Response</b>							
	-3dB Bandwidth						
	Small Signal	$<0.2V_{PP}$	1100				MHz
	Large Signal	$<2.0V_{PP}$	500	380	380	360	MHz
	$\pm 0.1$ dB Bandwidth	$<2.0V_{PP}$	200				MHz
	Gain Flatness						
	Peaking	DC to 200MHz	0				dB
	Rolloff	DC to 200MHz	0.1	0.5	0.5	0.5	dB
	Linear Phase Deviation	$<200MHz$	0.8				deg
	Differential Gain	$R_L = 150\Omega$ , 4.43MHz	0.03	0.05	0.05	0.05	%
	Differential Phase	$R_L = 150\Omega$ , 4.43MHz	0.02	0.02	0.05	0.05	deg
<b>Time Domain Response</b>							
	Rise and Fall Time	2V Step	0.8	1.1	1.1	1.1	ns
	Settling Time to $\pm 0.2\%$	2V Step	6				ns
	Settling Time to $\pm 0.1\%$	2V Step	11				ns
	Overshoot	2V Step	10	18	18	18	%
	Slew Rate	4V Step	2500	2000	2000	2000	V/ $\mu s$
<b>Distortion And Noise Response</b>							
	2nd Harmonic Distortion	$2V_{PP}$ , 5MHz	-63	-59	-59	-59	dBc
		$2V_{PP}$ , 20MHz	-52	-48	-48	-48	dBc
		$2V_{PP}$ , 50MHz	-44	-40	-40	-40	dBc
	3rd Harmonic Distortion	$2V_{PP}$ , 5MHz	-84	-77	-75	-75	dBc
		$2V_{PP}$ , 20MHz	-73	-66	-64	-64	dBc
		$2V_{PP}$ , 50MHz	-62	-55	-53	-53	dBc
	3rd Order Intercept	70MHz	30				dBm
	1dB Gain Compression @ 50MHz		16				dBm
	Equivalent Input Noise						
	Non-Inverting Voltage	1MHz	2.2	2.9			$nV/\sqrt{Hz}$
	Inverting Current	1MHz	15	20.0			$pA/\sqrt{Hz}$
	Non-Inverting Current	1MHz	3	5.0			$pA/\sqrt{Hz}$
<b>Static, DC Performance</b>							
	Input Offset Voltage (Note 3)		3	7	9	9	mV

## Electrical Characteristics (Continued)

$A_V = +2$ ,  $V_{CC} = \pm 5V$ ,  $R_L = 100\Omega$ ,  $R_f = 250\Omega$ ; unless specified

Symbol	Parameter	Conditions	Typ	Min/Max (Note 2)				Units
<b>Static, DC Performance</b>								
	Average Drift		25					$\mu V/^\circ C$
	Input Bias Current (Note 3)	Non-Inverting	6	30	45	60		$\mu A$
	Average Drift		50					$nA/^\circ C$
	Input Bias Current (Note 3)	Inverting	2	20	25	40		$\mu A$
	Average Drift		25					$nA/^\circ C$
	Power Supply Rejection Ratio	DC	48	43	41	41		dB
	Common Mode Rejection Ratio	DC	47	44	45	46		dB
	Supply Current (Note 3)	$R_L = \infty$	12	13.5	14	14		mA
<b>Miscellaneous Performance</b>								
	Input Resistance	Non-Inverting	400	200	200	150		K $\Omega$
	Input Capacitance	Non-Inverting	1.3					pF
	Output Resistance	Closed Loop	0.1	0.15	0.15	0.25		$\Omega$
	Output Voltage Range	$R_L = \infty$	3.3	3.1	3.1	3.1		V
		$R_L = 100\Omega$	2.9	2.8	2.8	2.8		V
	Input Voltage Range	Common-Mode	2.4	2.2	2.1	1.9		V
	Output Current		80	60	50	40		mA

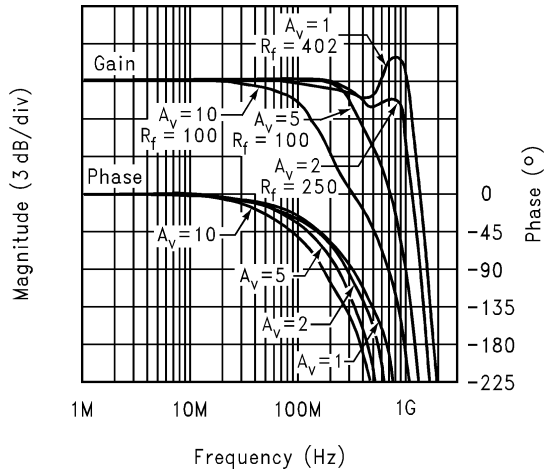
**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

**Note 2:** Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

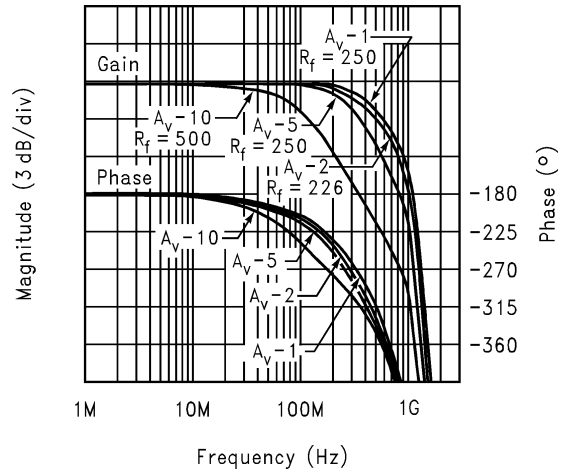
**Note 3:** AJ-level: spec. is 100% tested at +25°C.

## Typical Performance Characteristics

### Non-Inverting Frequency Response

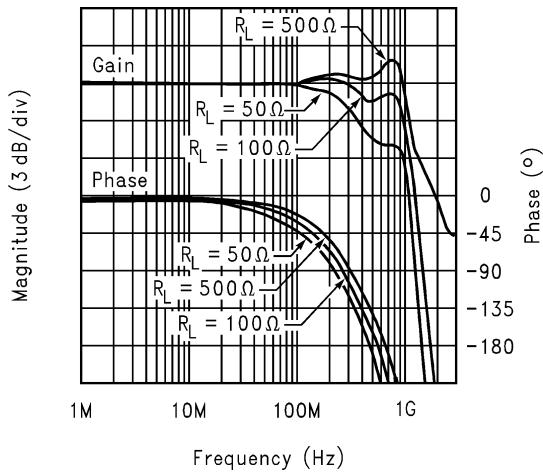


### Inverting Frequency Response



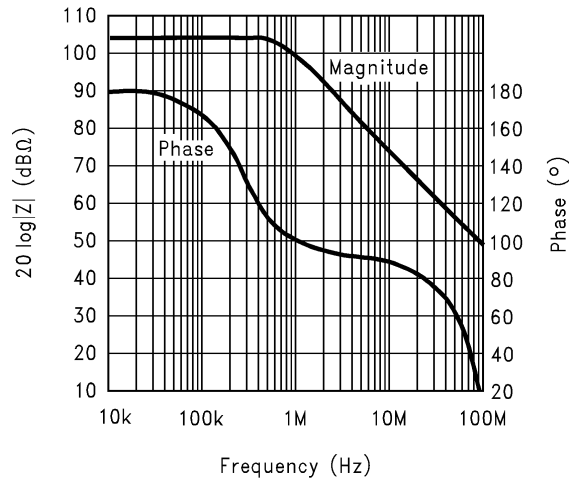
# Typical Performance Characteristics (Continued)

Frequency Response vs. Load



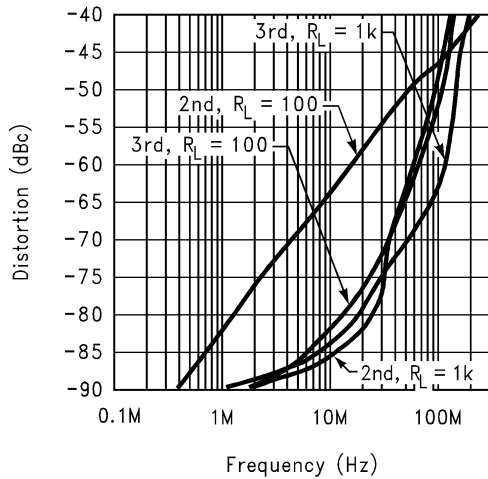
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Open Loop Transimpedance, Z(s)



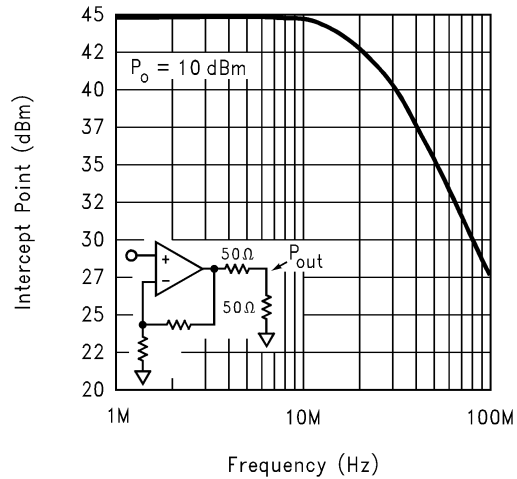
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Harmonic Distortion vs. Frequency



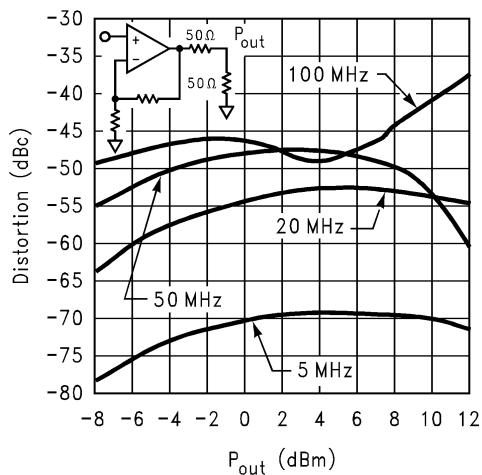
DS012715-8

2-Tone, 3rd Order Intermodulation Intercept



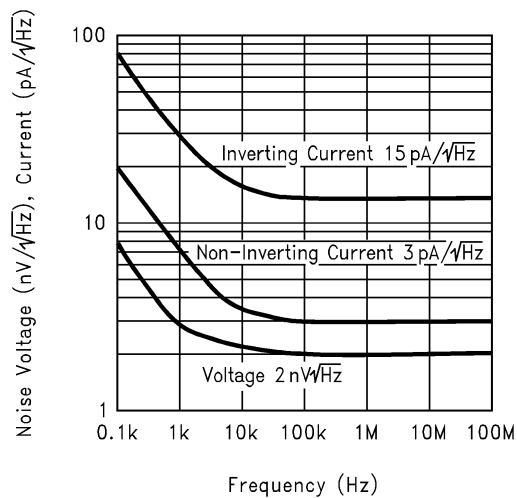
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2nd Harmonic Distortion vs. P<sub>out</sub>



DS012715-10

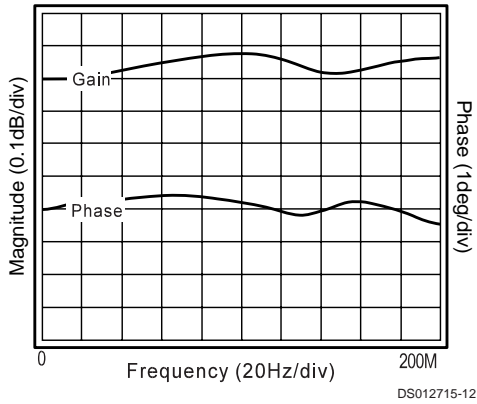
3rd Harmonic Distortion vs. P<sub>out</sub>



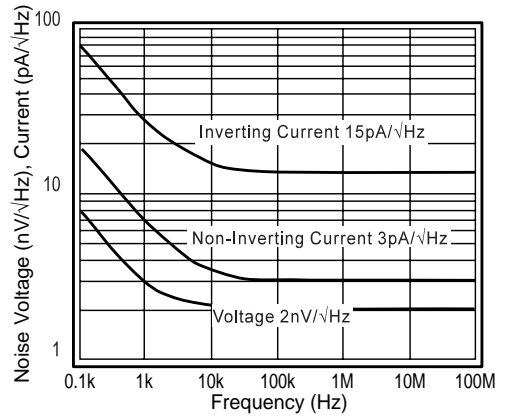
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# Typical Performance Characteristics (Continued)

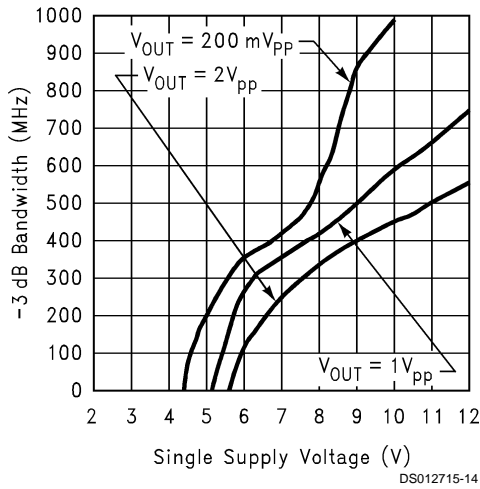
**Gain Flatness and Linear Phase**



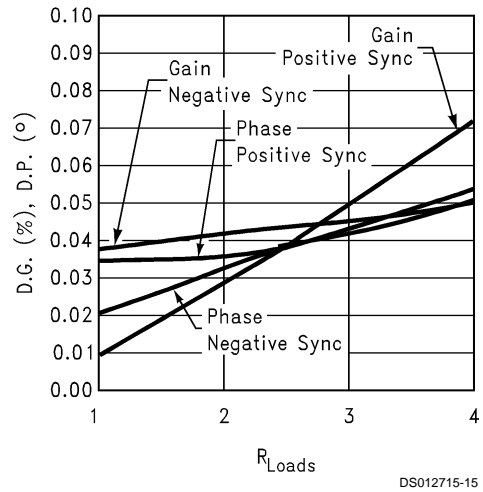
**Equivalent Input Noise**



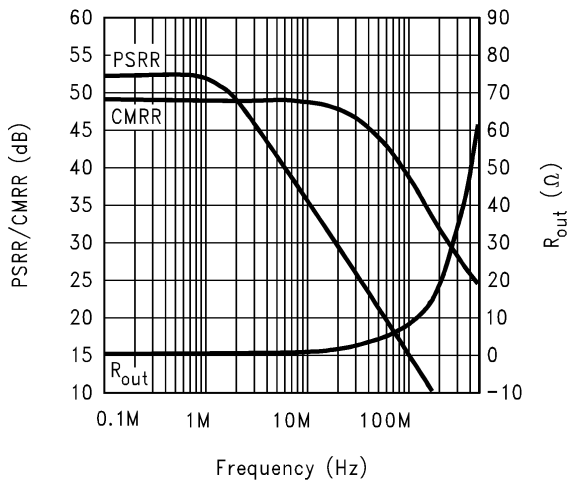
**Single Supply -3dB Bandwidth**



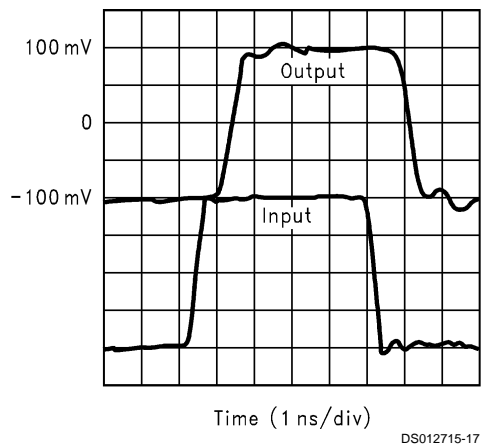
**Differential Gain and Phase**



**PSRR, CMRR, and Closed Loop R<sub>OUT</sub>**

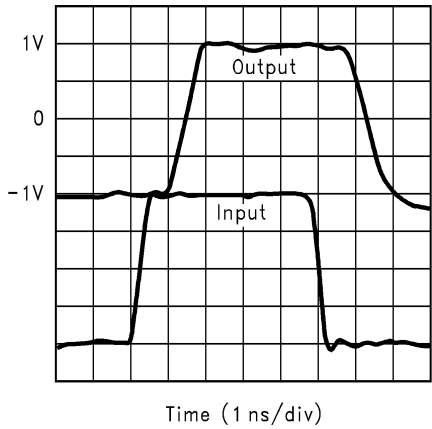


**Small Signal Pulse Response**

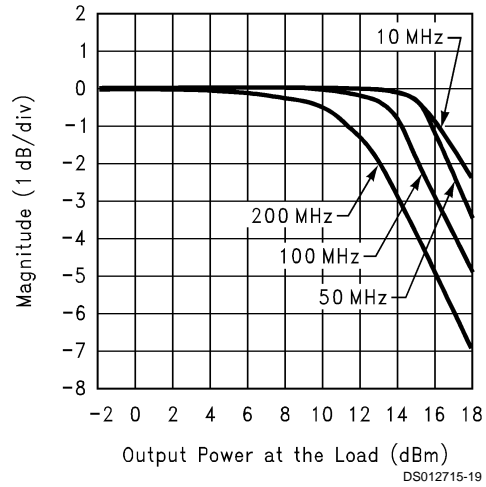


# Typical Performance Characteristics (Continued)

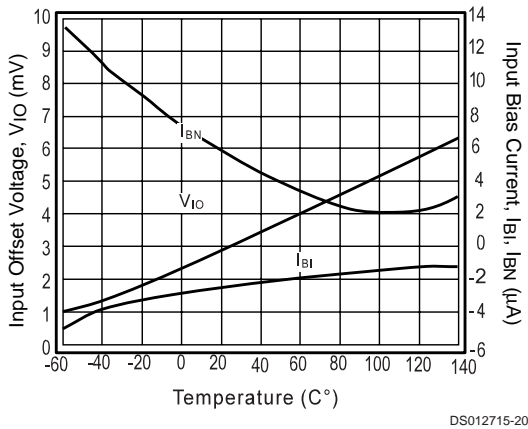
Large Signal Pulse Response



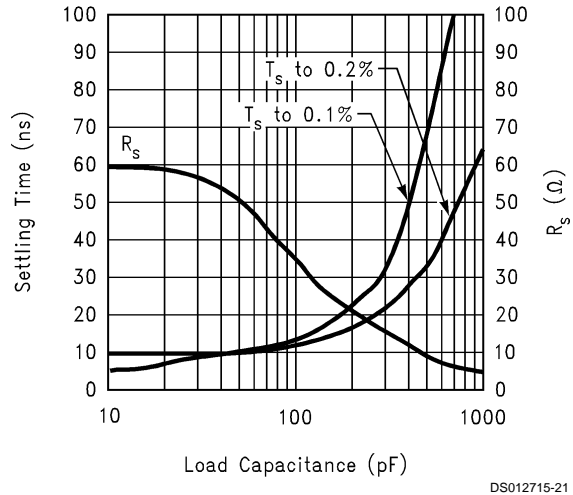
Gain Compression



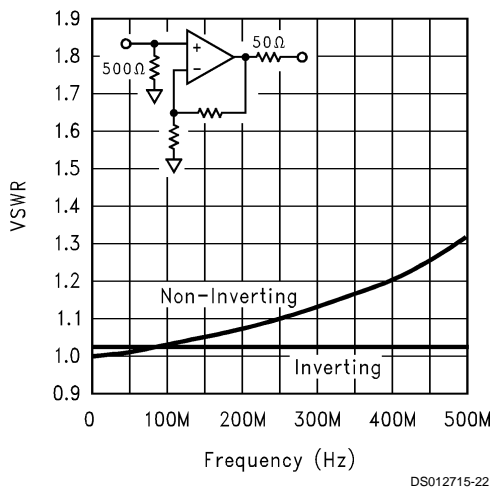
Typical  $I_{BI}$ ,  $I_{BN}$ ,  $V_{IO}$  vs. Temperature



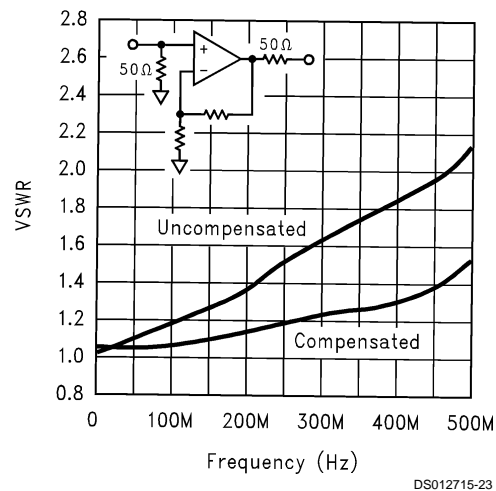
$R_s$  and Settling Time vs.  $C_L$



Input VSWR



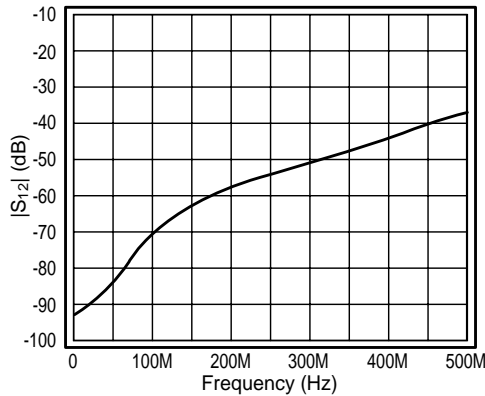
Output VSWR





## Typical Performance Characteristics (Continued)

### Reverse Isolation ( $S_{12}$ )



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## Application Division

### CLC449 Operation

#### CLC449 Extended Application Information

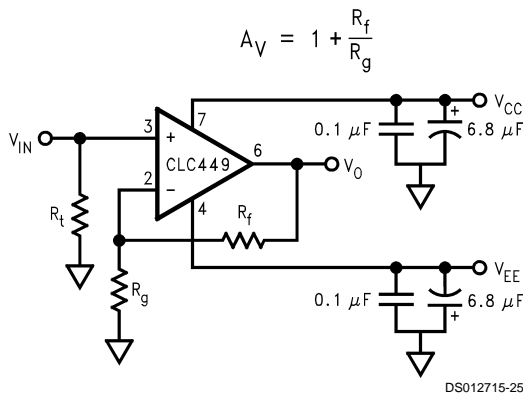
The following design and application topics will supply you with:

- A comprehensive set of design parameters and design parameter adjustment techniques.
- A set of formulas that support design parameter change prediction
- A series of common applications that the CLC449 supports.
- A set of easy to use design guidelines for the CLC449.

Additional design applications are possible with the CLC449. If you have application questions, call 1-800-272-9959 in the U.S. to contact a technical staff member.

#### DC Gain (Non-inverting)

The non-inverting DC voltage gain for the configuration shown in is:



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FIGURE 1. Non-Inverting Gain

The normalized gain plots in the **Typical Performance Characteristics** section show different feedback resistors,  $R_f$ , for different gains. These values of  $R_f$  are recommended for obtaining the highest bandwidth with minimal peaking. The resistor  $R_t$  in *Figure 1* provides DC bias for the non-inverting input.

For  $A_V \leq 5$ , calculate the recommended  $R_f$  as follows:

$R_f \approx 340 - A_V \times R_i$  where  $R_i = 45\Omega$ . For  $A_V > 5$ , the minimum recommended  $R_f$  is  $100\Omega$ .

Select  $R_g$  to set the DC gain:

$$R_g = \frac{R_f}{A_V - 1}$$

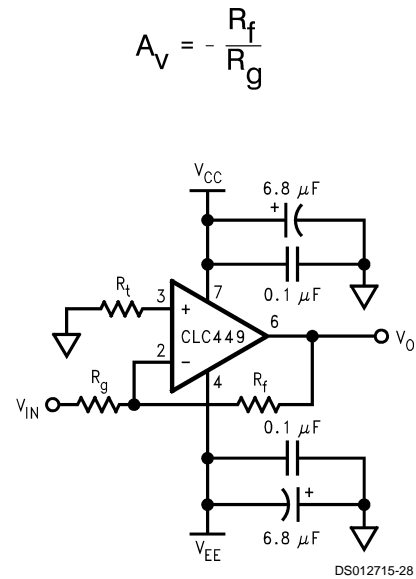
Accuracy of DC gain is usually limited by the tolerance of  $R_f$  and  $R_g$ .

#### DC Gain (unity gain buffer)

Unity gain buffers are easily designed with a current-feedback amplifier as long as the recommended feedback resistor  $R_f = 402\Omega$  is used and  $R_g = \infty$ , i.e., open. Parasitic capacitance at the inverting node may require a slight increase of  $R_f$  to maintain a flat frequency response.

#### DC Gain (inverting)

The inverting DC voltage gain for the configuration shown in *Figure 2* is



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FIGURE 2. Inverting Gain

## Application Division (Continued)

The normalized gain plots in the **Typical Performance Characteristics** section show different feedback resistors  $R_f$  for different gains. These values of  $R_f$  are recommended for obtaining the highest bandwidth with minimal peaking. The resistor  $R_f$  in *Figure 2* provides DC bias for the non-inverting input.

For  $|A_v| \leq 4$ , calculate the recommended  $R_f$  as follows:

$R_f \cong 295 - |A_v| \times R_i$  where  $R_i = 45\Omega$ . For  $|A_v| > 4$ , the minimum recommended  $R_f$  is  $100\Omega$ .

Select  $R_g$  to set the DC gain:

$$R_g = \frac{R_f}{|A_v|}$$

At large gains,  $R_g$  becomes small and will load the previous stage. This situation is resolved by driving  $R_g$  with a low impedance buffer like the CLC111, or increasing  $R_f$  and  $R_g$  see the **Bandwidth (Small Signal)** sub-section for the tradeoffs).

Accurate DC gain is usually limited by the tolerance of the external resistors  $R_f$  and  $R_g$ .

### Bandwidth (Small Signal)

The CLC449 current-feedback amplifier bandwidth is a function of the feedback resistor ( $R_f$ ), not of the DC voltage gain ( $A_v$ ). The bandwidth is approximately proportional to  $1/R_f$ . As a rule, if  $R_f$  doubles, the bandwidth is cut in half. Other AC specifications will also be degraded. **Decreasing  $R_f$  from the recommended value increases peaking and for very small values of  $R_f$  oscillation will occur.**

With an inverting amplifier design, peaking is sometimes observed. This is often the result of layout parasitics caused by inadequate ground planes or long traces. If this is observed, placing a 50 to  $200\Omega$  resistor between the non-inverting pin and ground will usually reduce the peaking.

### Bandwidth (Minimum Slew Rate)

Slew rate influences the bandwidth for large signal sinusoids. To determine an approximate value of slew rate, necessary to support large sinusoids use the following equation:

$$SR \cong 5 \times f \times V_{\text{peak}}$$

$V_{\text{peak}}$  is the peak output sinusoid voltage,  $f$  is the frequency of the sinusoid.

The slew rate of the CLC449 in inverting gains is always higher than in non-inverting gains.

### DC Design (Level Shifting)

*Figure 3* shows a DC level shifting circuit for inverting gain configurations.  $V_{\text{ref}}$  produces a DC output level shift of

$$-V_{\text{ref}} \times \frac{R_f}{R_{\text{ref}}}$$

which is independent of the DC output produced by  $V_{\text{in}}$ .

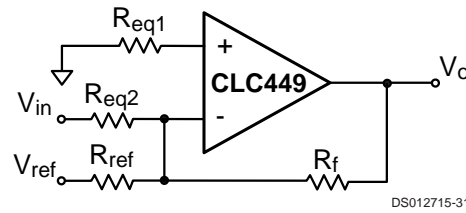


FIGURE 3. Level Shifting Circuit

### DC Design (Single Supply)

*Figure 4* is a typical single-supply circuit. Resistors  $R_1$  and  $R_2$  form a voltage divider that sets the non-inverting input DC voltage. This circuit has a DC gain of 1. The coupling capacitor  $C_1$  isolates the DC bias point from the previous stage. Both capacitors make a high pass response; the high frequency gain is determined by  $R_f$  and  $R_g$ .

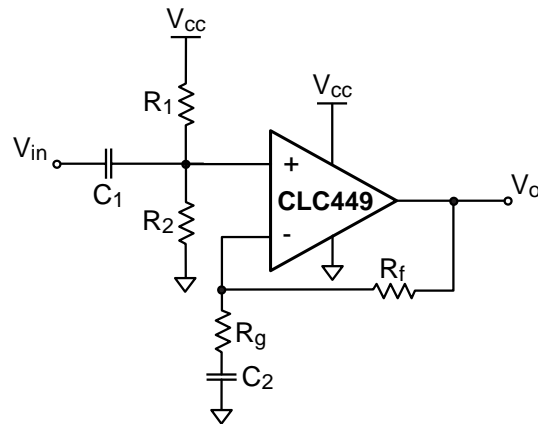


FIGURE 4. Single Supply Circuit

The complete gain equation for the circuit in *Figure 4* is

$$\frac{V_o}{V_{\text{in}}} = \frac{s\tau_1}{1 + s\tau_1} \cdot \frac{1 + s\tau_2 \cdot \left(1 + \frac{R_f}{R_g}\right)}{1 + s\tau_2}$$

where  $s = j\omega$ ,  $\tau_1 = (R_1 \parallel R_2) \times C_1$ , and  $\tau_2 = R_g C_2$ .

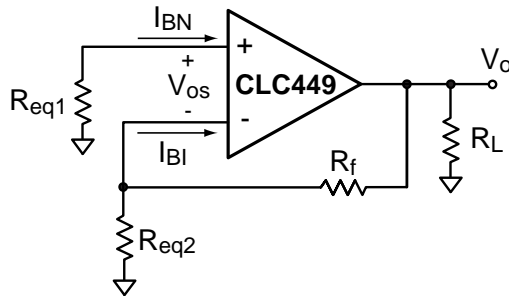
### DC Design (DC Offsets)

The DC offset model shown in *Figure 5* is used to calculate the output offset voltage. The equation for output offset voltage is:

$$V_o = - \left( V_{\text{os}} + I_{\text{BN}} \cdot R_{\text{eq1}} \right) \cdot \left( 1 + \frac{R_f}{R_{\text{eq2}}} \right) + (I_{\text{BI}} \cdot R_f)$$

The current offset terms,  $I_{\text{BN}}$  and  $I_{\text{BI}}$ , **do not track each other**. The specifications are stated in terms of magnitude only. Therefore, the terms  $V_{\text{OS}}$ ,  $I_{\text{BN}}$ , and  $I_{\text{BI}}$  may have either positive or negative polarity. Matching the equivalent resistance seen at both input pins does not reduce the output offset voltage.

## Application Division (Continued)



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FIGURE 5. DC Offset Model

### DC Design (Output Loading)

$R_L$ ,  $R_f$ , and  $R_g$  load the op amp output. The equivalent closed-loop load impedance seen by the output in Figure 5 is:

$$R_{L\_eq} = R_L || (R_f + R_{eq2}), \text{ non-inverting gain}$$

$$R_{L\_eq} = R_L || R_f \text{ inverting gain}$$

$R_{L\_eq}$  needs to be kept large enough so that the minimum available output current can produce the required output voltage swing.

### Capacitive Loads

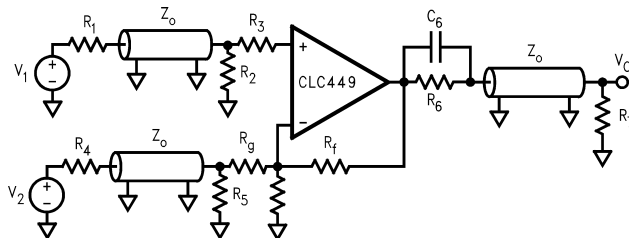
Capacitive loads, such as found in A/D converters, require a series resistor ( $R_s$ ) in the output to improve settling performance. The  $R_s$  and Settling Time vs.  $C_L$  plot in the **Typical Performance Characteristics** section provides the information for selecting this resistor.

Also, use a series resistor to reduce the effects of reactive loads on amplifier loop dynamics. For instance, driving coaxial cables without an output series resistor may cause peaking or oscillation.

### Transmission Line Matching

One method for matching the characteristic impedance of a transmission line is to place the appropriate resistor at the input or output of the amplifier. Figure 6 shows the typical circuit configurations for matching transmission lines.

In non-inverting gain applications,  $R_g$  is connected directly to ground. The resistors  $R_1$ ,  $R_2$ ,  $R_6$ , and  $R_7$  are equal to the characteristic impedance



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FIGURE 6. Transmission Line Matching

In inverting gain applications,  $R_3$  is connected directly to ground. The resistor  $R_4$ ,  $R_6$ , and  $R_7$  are equal to  $Z_0$ . The parallel combination of  $R_5$  and  $R_g$  is also equal to  $Z_0$ .

The input and output matching resistors attenuate the signal by a factor of 2, therefore additional gain is needed. Use  $C_6$  to match the output transmission line over a greater frequency range. It compensates for the increase of the op amp's output impedance with frequency.

### Thermal Design

To calculate the power dissipation for the CLC449, follow these steps:

1. Calculate the no-load op amp power:

$$P_{amp} = I_{cc} (V_{cc} - V_{EE})$$

2. Calculate the output stage's RMS power:

$$P_o = (V_{cc} - V_{load}) I_{load}, \text{ where } V_{load} \text{ and } I_{load} \text{ are the RMS voltage and current across the external load.}$$

3. Calculate the total op amp RMS power:

$$P_t = P_{amp} + P_o$$

To calculate the maximum allowable ambient temperature, solve the following equation:  $T_{amb} = 150 - P_t \times \theta_{JA}$  where  $\theta_{JA}$  is the thermal resistance from junction to ambient in  $^{\circ}\text{C}/\text{W}$ , and  $T_{amb}$  is in  $^{\circ}\text{C}$ . The **Package Thermal Resistance** section contains the thermal resistance for various packages.

### Dynamic Range (input/output protection)

Input ESD diodes are present on all connected pins for protection from static voltage damage. For a signal that may exceed the supply voltages, we recommend using diode clamps at the amplifier's input to limit the signals to less than the supply voltages.

**Dynamic Range (input/output levels)** The **Electrical Characteristics** section specifies the Common-Mode Input Range and Output Voltage Range; these voltage ranges scale with the supplies. Output Current also specified in the **Electrical Characteristics** section.

Unity gain applications are limited by the Common-Mode Input Range. At greater non-inverting gains, the Output Voltage Range becomes the limiting factor. Inverting gain applications are limited by the Output Voltage Range.

For transimpedance or inverting gain applications, the current ( $I_{inv}$ ) injected at the inverting input of the op amp needs to be:

$$|I_{inv}| \leq \frac{V_{max}}{R_f}$$

where  $V_{max}$  is the Output Voltage Range .

The voltage ranges discussed above are achieved as long as the equivalent output load is large enough so that the output current can produce the required output voltage swing. See the **DC Design (output loading)** sub-section for details.

### Dynamic Range (Intermods)

In RF applications, the CLC449 specifies a third order intercept of 30dBm at 70MHz and  $P_o = 10\text{dBm}$ .at a gain of 10. **A2-Tone, 3rd Order IMD Intercept** plot is found in the **Typical Performance Characteristics** section. The output power level is taken at the load. Third-order harmonic distortion is calculated with the formula:

$$HD3^{rd} = 2 \times (IP3_o - P_o)$$

where:

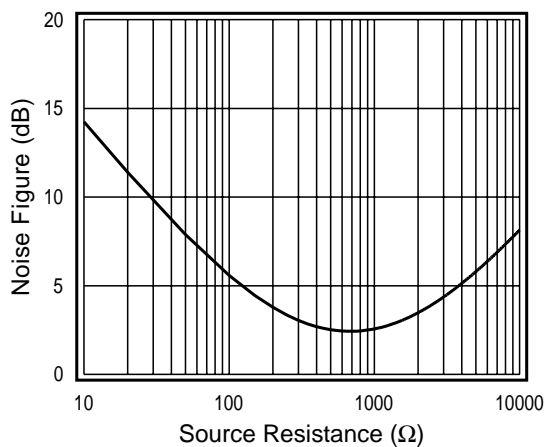
- $IP3_o$  = Third-order output intercept, dBm at the load.
- $P_o$  = output power level, dBm at the load.
- $HD3^{rd}$  = Third-order distortion from the fundamental, -dBc.

## Application Division (Continued)

- dBm is the power in mW, at the load, expressed in dB.
- Realized third-order output distortion is highly dependent upon the external circuit. Some of the common external circuit choices that improve 3<sup>rd</sup> order distortion are:
- short and equal return paths from the load to the supplies.
  - de-coupling capacitors of the correct value.
  - higher load resistance
  - a lower ratio of the output swing to the power supply voltage.

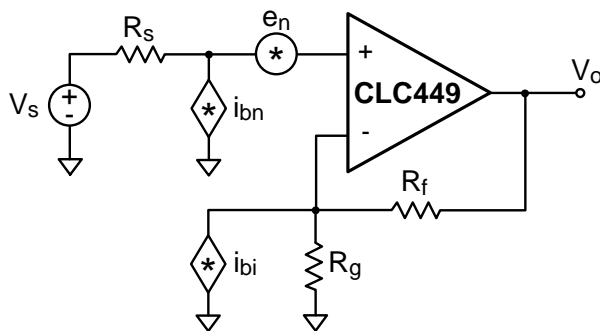
### Dynamic Range (Noise)

In RF applications, noise is frequently specified as Noise Figure (NF). *Figure 7* plots NF for the CLC449 at a gain of 10, with a feedback resistor  $R_f$  of 100 $\Omega$ , and with no input matching resistor. The minimum Noise Figure (2.5dB) for these conditions occurs when the source resistance equals 700 $\Omega$ .



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FIGURE 7. Noise Figure Plot



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FIGURE 8. CLC449 Noise Model

The CLC449 noise model in *Figure 8* is used to develop the equation below.

The equation for Noise Figure (NF) is:

$$NF = 10 \log \left( \frac{e_{ni}^2 + (i_{bn} R_s)^2 + 4kTR_s + (i_{bi} \cdot R_f \parallel R_g)^2 + 4kT \cdot R_f \parallel R_g}{4kTR_s} \right)$$

Where:

- $R_s$  is the source resistance at the non-inverting input.

- There is no matching resistor from the input to ground.
- $e_{ni}$ ,  $i_{bn}$ ,  $i_{bi}$  are the voltage and current noise density terms (see in the **Distortion and Noise Response** sub-section of the **Electrical Characteristics** section).
- $4kT = 16 \times 10^{-21} \text{J}$ ,  $T = 290^\circ \text{K}$ .
- $R_f$  is the feedback resistor and  $R_g$  is the gain setting resistor.

### Printed Circuit Board Layout

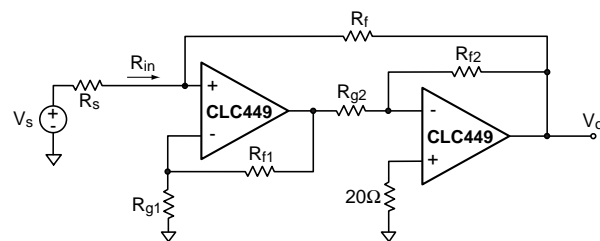
High Frequency op amp performance is strongly dependent on proper layout, proper resistive termination and adequate power supply decoupling. The most important layout points to follow are:

- Use a ground plane
- Bypass power supply pins with monolithic:
- ceramic capacitors of about 0.1 $\mu\text{F}$  placed less than 0.1" (3mm) from the pin
- tantalum capacitors of about 6.8 $\mu\text{F}$  for large signal current swings or improved power supply noise rejection; we recommend a minimum of 2.2  $\mu\text{F}$  for any circuit
- Minimize trace and lead lengths for components between the inverting and output pins
- Remove ground plane underneath the amplifier package and 0.1" (3mm) from all input/output pads
- If parts must be socketed, always use flush-mounted socket pins instead of high profile sockets.

Evaluation boards are available for proto-typing and measurements. Additional layout information is available in the evaluation board literature.

### Low Noise Composite Amp With Input Matching

The composite circuit shown in *Figure 9* eliminates the need for a matching resistor to ground at the input. By connecting two amplifiers in series, the first non-inverting and second inverting, an overall inverting gain is realized. The feedback resistor ( $R_f$ ) connected from the output of the second amplifier to the non-inverting input of the first amplifier closes the loop, and generates a set input resistance ( $R_{in}$ ) that can be matched to  $R_s$ . This resistor generates less noise than a matching resistor to ground at the input.



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FIGURE 9. Composite Amplifier

The input resistance and DC voltage gain of the amplifier are:

$$R_{in} = \frac{R_f}{1+G}, \text{ where } G = \left( 1 + \frac{R_{f1}}{R_{g1}} \right) \cdot \left( \frac{R_{f2}}{R_{g2}} \right)$$

$$\frac{V_o}{V_s} = -G \cdot \left( \frac{R_{in}}{R_{in} + R_s} \right)$$

Match the source resistance by setting:  $R_{in} = R_s$

Noise voltage produced by  $R_f$ , referred to the source  $V_s$  is:

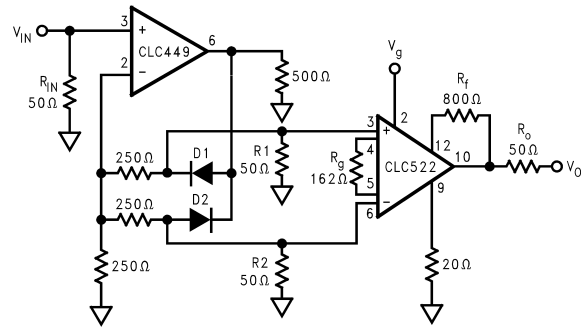
## Application Division (Continued)

$$e^2_{R_i} = 4kTR_s \cdot \left( \frac{R_s}{R_{in} \cdot (1+G)} \right)$$

The noise of a simple input matching resistor connected to ground can be calculated by setting G to 0 in this equation. Thus, this circuit reduces the thermal noise power produced by the matching resistor by a factor of (1+G).

### Rectifier Circuit

Wide bandwidth rectifier circuits have many applications. *Figure 10* shows a 200MHz wideband full-wave rectifier circuit using a CLC449 and a CLC522 amplifier. Schottky or PIN diodes are used for D<sub>1</sub> and D<sub>2</sub>. They produce an active half-wave rectifier whose signals are taken at the feedback diode connection. The CLC522 takes the difference of the two half-wave rectified signals, producing a full-wave rectifier. The CLC522 is used at a gain of 5 to achieve high differential bandwidth. For best high frequency performance, maintain low parasitic capacitance from the diodes D<sub>1</sub> and D<sub>2</sub> to ground, and from the input of the CLC522 to ground.



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FIGURE 10. Full-Wave Rectifier

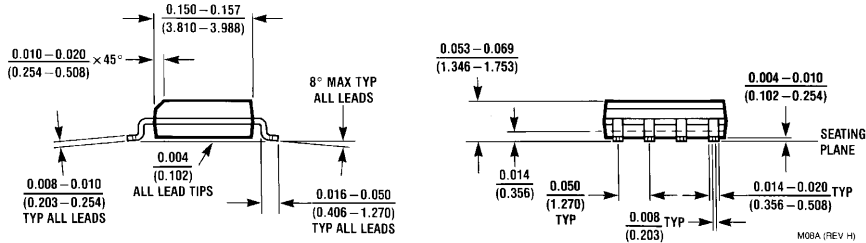
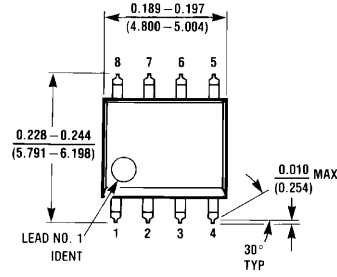
### Flash A/D Application

The Typical Application circuit on the front page shows the CLC449 driving a flash A/D. Flash A/D's require fast settling, low distortion, low noise and wide bandwidth to achieve high Effective Number of Bits and Spurious Free Dynamic Range (SFDR).

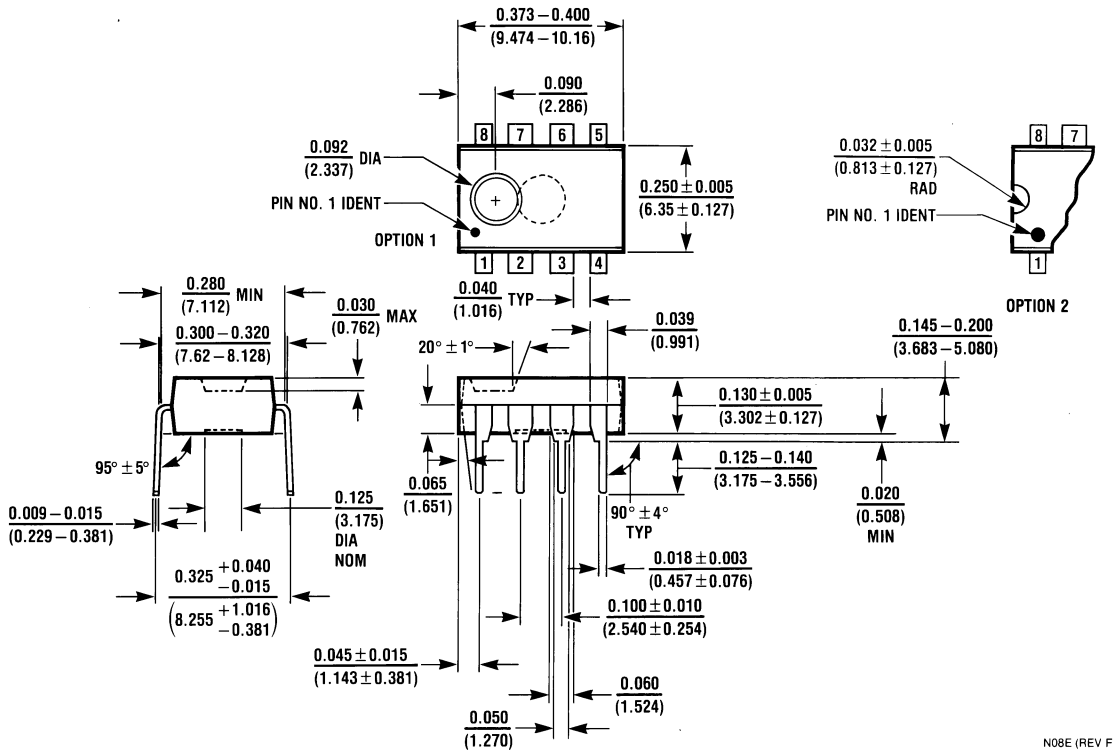
This circuit connects a CLC449 to a TDA8716, 8-bit, 120MHz Flash Converter. The input capacitance for this converter is typically 13pF plus layout capacitance. From the **R<sub>s</sub> and Settling Time vs. C<sub>L</sub>** plot in the **Typical Performance Characteristics** section, select a series resistor (R<sub>s</sub>) of 55Ω. Place R<sub>s</sub> in series with the output of the CLC449 to achieve settling to 0.1% in approximately 11ns.

Keep the amplifier noise seen at the A/D input at least 3dB lower than the A/D's noise, to avoid degrading A/D noise performance.

**Physical Dimensions** inches (millimeters) unless otherwise noted



**8-Pin SOIC**  
NS Package Number M08A



**8-Pin MDIP**  
NS Package Number N08E

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