CLC412 Dual Wideband Video Op Amp

Check for Samples: CLC412

FEATURES

- **Wide Bandwidth: 330MHz (A_V = +1); 250MHz (A_V = +2)**
- **0.1dB Gain Flatness to 30MHz**
- **Low Power: 5mA/Channel**
- **Very Low Diff. Gain, Phase: 0.02%, 0.02°**
- **-76dB Channel-to-Channel Crosstalk (10MHz)**
- **Fast Slew Rate: 1300V/µs**
- **Unity Gain Stable**

APPLICATIONS

- **HDTV, NTSC & PAL Video Systems**
- **Video Switching and Distribution**
- **IQ Amplifiers**
- **Wideband Active Filters**
- **Cable Drivers**
- **DC Coupled Single-to-Differential Conversions**

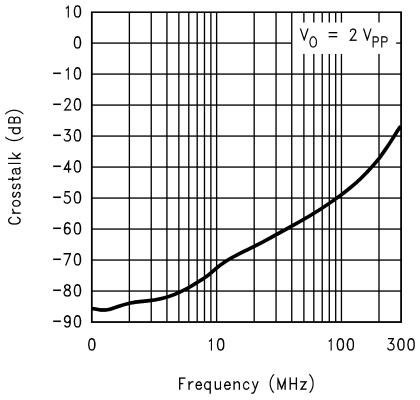


Figure 1. Channel-to-Channel Crosstalk

DESCRIPTION

The CLC412 combines a high speed complementary bipolar process with TI's current feedback topology to produce a very high speed dual op amp. The CLC412 provides a 250MHz small signal bandwidth at a gain of +2V/V and a 1300V/µs slew rate while consuming only 50mW per amplifier from ±5V supplies.

The CLC412 offers exceptional video performance with its 0.02% and 0.02° differential gain and phase errors for NTSC and PAL video signals while driving one back terminated 75Ω load. The CLC412 also offers a flat gain response of 0.1dB to 30MHz and very low channel-to-channel crosstalk of −76dB at 10MHz. Additionally, each amplifier can deliver a 70mA continuous output current. This level of performance makes the CLC412 an ideal dual op amp for high density broadcast quality video systems.

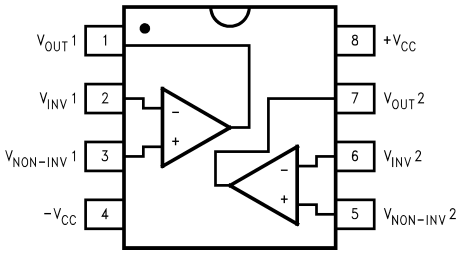
The CLC412's two very well matched amplifiers support a number of applications such as differential line drivers and receivers. In addition, the CLC412 is well suited for Sallen Key active filters in applications such as anti-aliasing filters for high speed A/D converters. Its small 8-pin SOIC package, low power requirement, low noise and distortion allow the CLC412 to serve portable RF applications such as IQ channels.

Enhanced Solutions (Military/Aerospace)

SMD Number: 5962-94719

Space level versions also available.

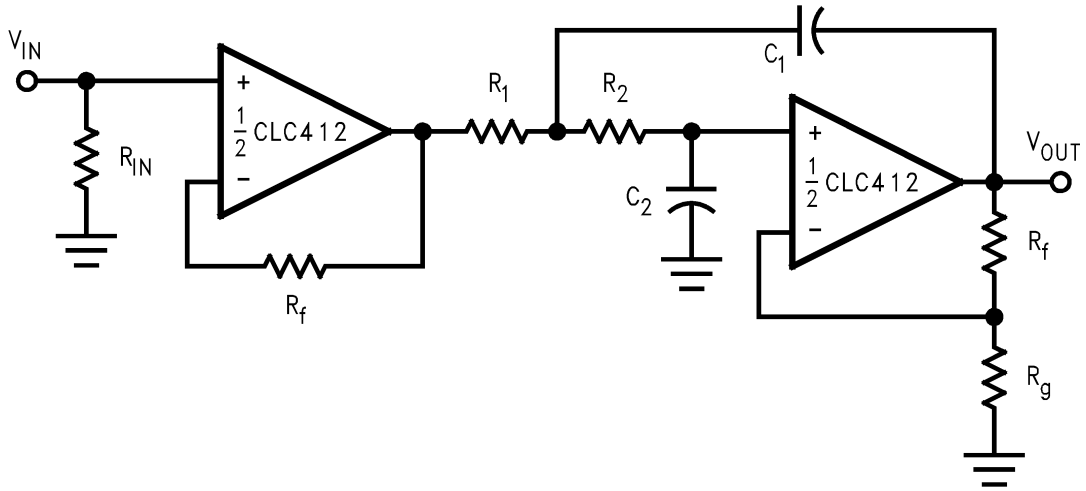
CONNECTION DIAGRAM



Pinout
PDIP & SOIC

TYPICAL APPLICATION

$$\frac{V_{OUT}}{V_{IN}} = \frac{\frac{K_o}{R_1 R_2 C_1 C_2}}{s^2 + s\left[\frac{1}{R_1 C_1} + \frac{1}{R_2 C_2} + \frac{1 - K_9}{R_2 C_2}\right] + \frac{1}{R_1 R_2 C_1 C_2}}$$



Sallen-Key Low-Pass Filter

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)(2)

		Value	Unit
V_{CC}		±7	V
I_{OUT}	Short Circuit protected to ground, however maximum reliability is obtained if I_{OUT} does not exceed..	125	mA
Common-Mode Input Voltage		$\pm V_{CC}$	V
Maximum Junction Temperature		+150	°C
Operating Temperature Range		−40 to +85	°C
Storage Temperature Range		−65 to +150	°C
Lead Temperature	Soldering 10 sec	+300	°C
ESD	Human Body Model	1000	V

(1) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The table of ELECTRICAL CHARACTERISTICS specifies conditions of device operation.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

OPERATING RATINGS

Thermal Resistance		
Package	(θ_{JC})	(θ_{JA})
PDIP	70°C/W	125°C/W
SOIC	65°C/W	145°C/W

ELECTRICAL CHARACTERISTICS

(A_V = +2, R_f = 634Ω, V_{CC} = ±5 V, R_L = 100Ω; Unless Specified).

Symbol	Parameter	Conditions	Typ	Min/Max Ratings (1)			Units
Ambient Temperature		CLC412AJ	+25°C	−40°C	+25°C	+85°C	
Frequency Domain Response							
SSBW	-3dB Bandwidth	V_{OUT} < 0.5V_{PP}	250	150	175	135	MHz
LSBW		V_{OUT} < 4.0V_{PP}	105	80	80	65	MHz
	Gain Flatness	V_{OUT} < 0.5V_{PP}					
GFP	Peaking	DC to 30MHz	0.1	0.1	0.1	0.2	dB
GFR	Rolloff	DC to 30MHz	0.1	0.4	0.3	0.3	dB
LPD	Linear Phase Deviation	DC to 75MHz	0.5	1.3	1.0	1.0	deg
DG	Differential Gain	R_L = 150Ω, 4.43MHz	0.02	0.04	0.04	0.08	%
DP	Differential Phase	R_L = 150Ω, 4.43MHz	0.02	0.04	0.04	0.08	deg
Time Domain Response							
TRS	Rise and Fall Time	0.5V Step	1.4	2.3	2.0	2.6	ns
TRL		4V Step	3.2	4.4	4.4	4.8	ns
TSS	Settling Time to 0.05%	2V Step	12	18	18	20	ns
OS	Overshoot	0.5V Step	8	15	15	15	%
SR	Slew Rate	2V Step	1300	1000	1000	800	V/µs

(1) Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

ELECTRICAL CHARACTERISTICS (continued)

(A_V = +2, R_f = 634Ω, V_{CC} = ±5 V, R_L = 100Ω; Unless Specified).

Symbol	Parameter	Conditions	Typ	Min/Max Ratings (1)			Units
Distortion And Noise Response							
HD2	2nd Harmonic Distortion	$2V_{PP}$, 20MHz	−46	−42	−42	−38	dBc
HD3	3rd Harmonic Distortion	$2V_{PP}$, 20MHz	−50	−46	−46	−42	dBc
IMD	3rd Order Intermodulation Intercept	10MHz	43	–	–	–	dBm_{1Hz}
	Equivalent Input Noise						
VN	Non-Inverting Voltage	>1MHz	3.0	3.4	3.4	3.8	$nV/\sqrt{Hz}$
NICN	Inverting Current	>1MHz	12.0	13.9	13.9	15.5	$pA/\sqrt{Hz}$
ICN	Non-Inverting Current	>1MHz	2.0	2.6	2.6	3.0	$pA/\sqrt{Hz}$
SNF	Noise Floor	>1MHz	−157	−156	−156	−155	dBm_{1Hz}
XTLKA	Crosstalk Input Referred	10MHz	−76	−70	−70	−70	dB
Static, DC Performance							
VIO	Output Offset Voltage(2)		±2	±10	±6	±12	mV
DVIO	Average Drift		±30	±60	-	±60	µV/°C
IBN	Input Bias Current(2)	Non-Inverting	±5	±28	±12	±12	µA
DIBN	Average Drift		±30	±187	-	±90	nA/°C
IBI	Input Bias Current(2)	Inverting	±3	±34	±15	±20	µA
DIBI	Average Drift		±20	±125	-	±80	nA/°C
PSRR	Power Supply Rejection Ratio	DC	50	46	46	44	dB
CMRR	Common Mode Rejection Ratio	DC	50	45	45	43	dB
ICC	Supply Current (2)	R_L = ∞	10.2	13.6	12.8	12.8	mA
Miscellaneous Performance							
RIN	Input Resistance	Non-Inverting	1000	300	500	500	kΩ
CIN	Input Capacitance	Non-Inverting	1.0	2.0	2.0	2.0	pF
ROUT	Output Resistance	Closed Loop	0.04	0.6	0.3	0.2	Ω
VO	Output Voltage Range	R_L = ∞	+3.8, −3.3	+3.6, −2.9	+3.7, −3.0	+3.7, −3.0	V
VOL		R_L = 100Ω	+3.1, −2.9	+2.0, −2.5	±2.7	±2.7	V
VOLC		R_L = 100Ω (0° to 70°C)			+2.5, −2.6		V
CMIR	Input Voltage Range	Common Mode	±2.2	±1.4	±2.0	±2.0	V
IO	Output Current		70	25	45	45	mA

(2) AJ-level: spec. is 100% tested at +25°C.

TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C, V_{CC} = ±5V, A_V = ±2V/V, R_f = 634Ω, R_L = 100Ω, Unless Specified).

Non-Inverting Frequency Response

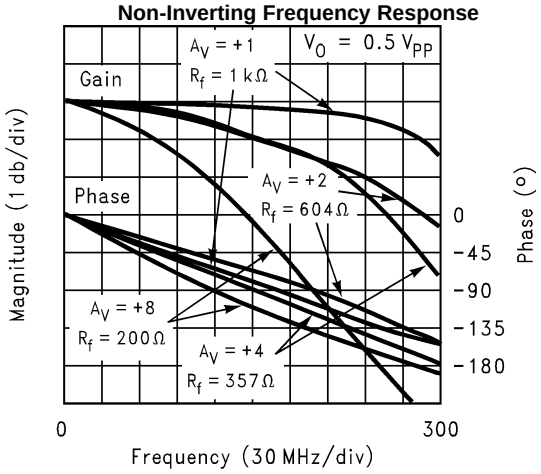


Figure 2.

Inverting Frequency Response

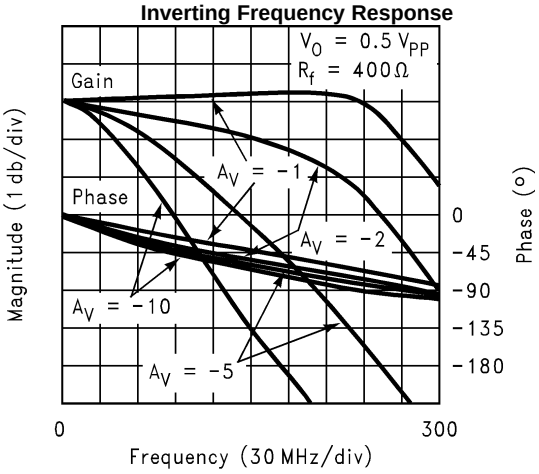


Figure 3.

Frequency Response vs. V_{OUT}

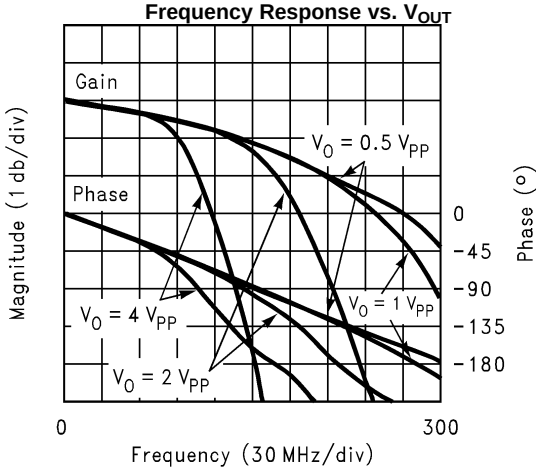


Figure 4.

Small Signal Channel Matching

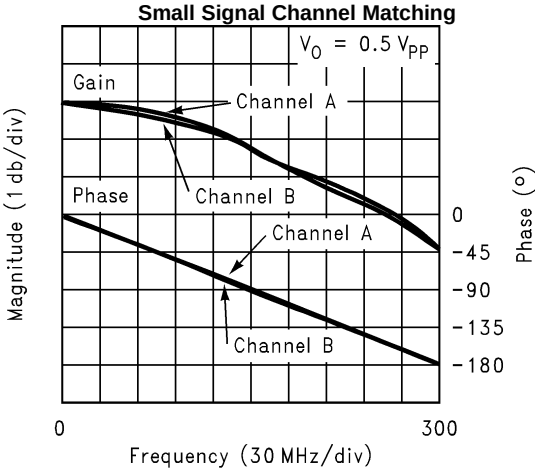


Figure 5.

Gain Flatness for Various Gains

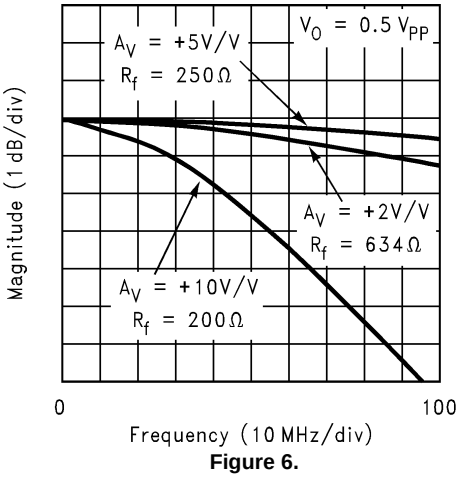


Figure 6.

Frequency Response vs. Load (R_L)

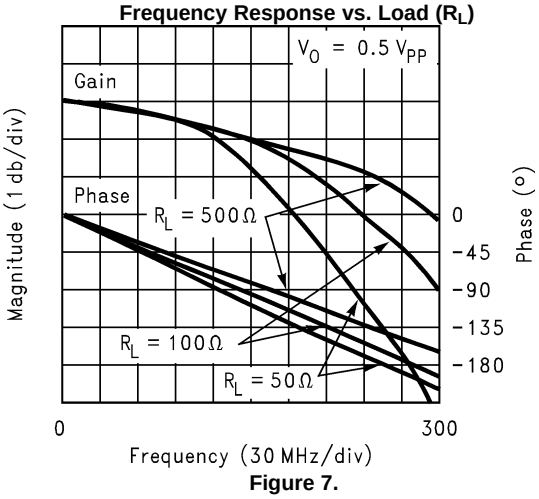


Figure 7.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(T_A = 25°C, V_{CC} = ±5V, A_V = ±2V/V, R_f = 634Ω, R_L = 100Ω, Unless Specified).

Pulse Response

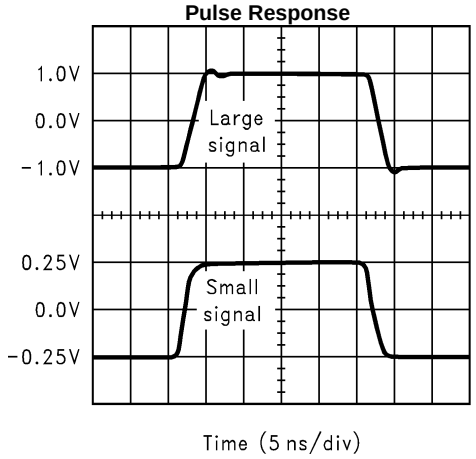


Figure 8.

Pulse Crosstalk

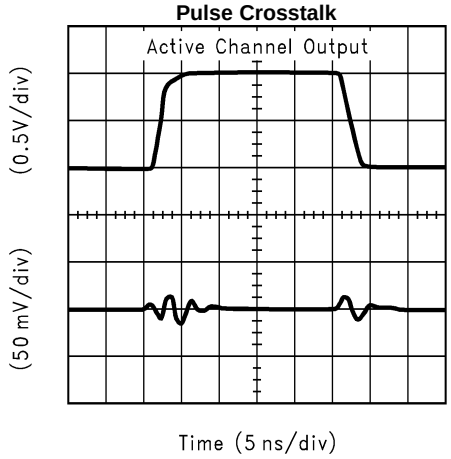


Figure 9.

Phase Linearity

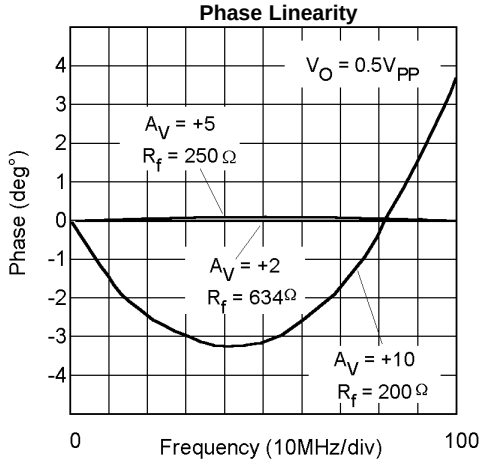


Figure 10.

Input-Referred Crosstalk

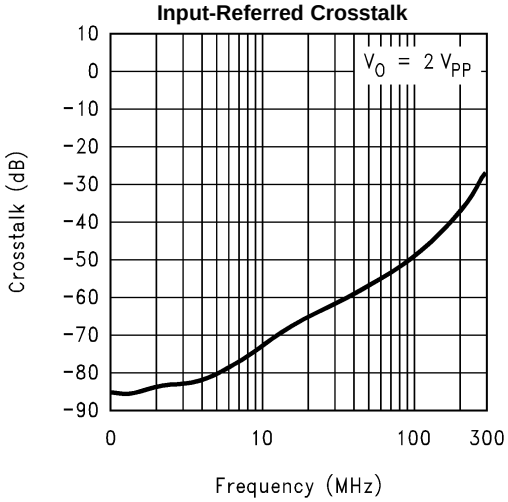


Figure 11.

Short-Term Settling Time

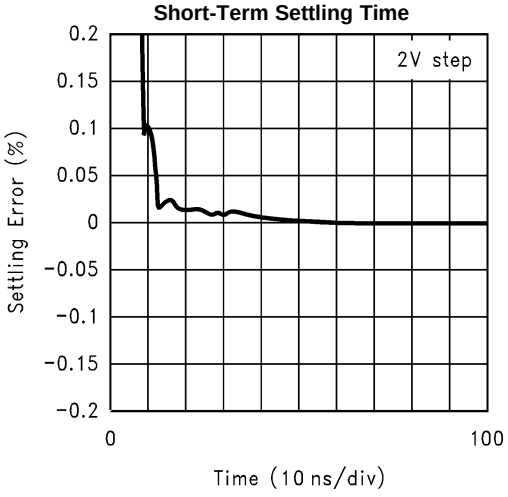


Figure 12.

Long-Term Settling Time

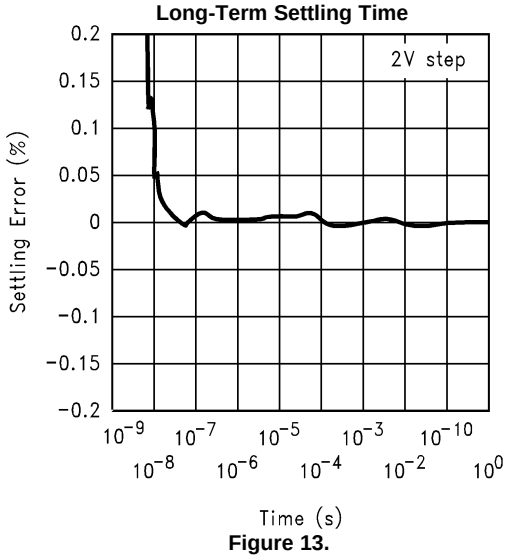


Figure 13.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(T_A = 25°C, V_{CC} = ±5V, A_V = ±2V/V, R_f = 634Ω, R_L = 100Ω, Unless Specified).

R_S and Settling Time vs. Capacitive Load

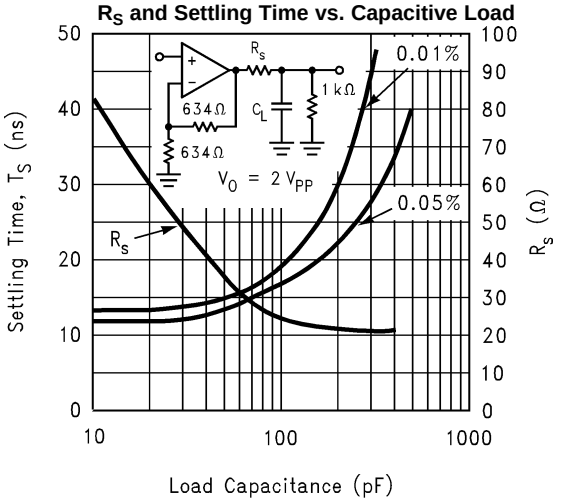


Figure 14.

Maximum Output Swing vs. Frequency

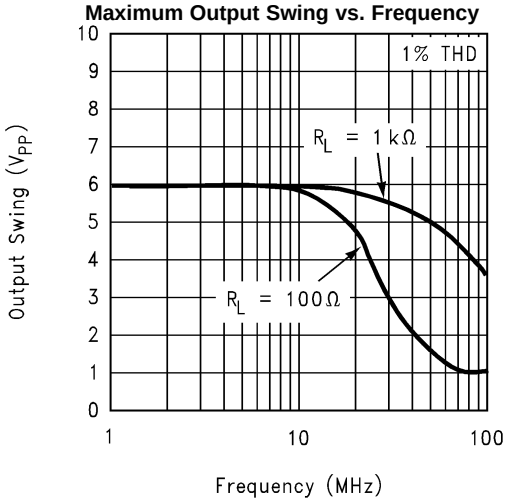


Figure 15.

−3dB Bandwidth vs. Output Voltage

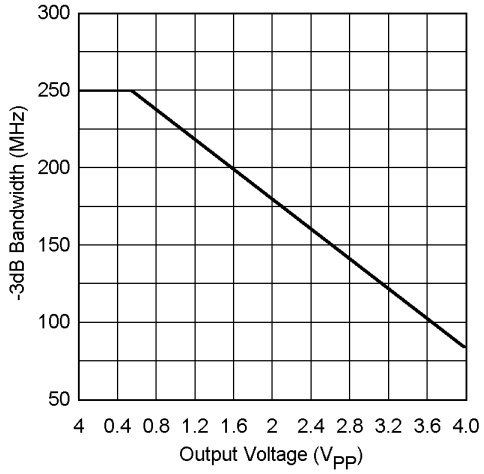


Figure 16.

Typical DC Errors vs. Temperature

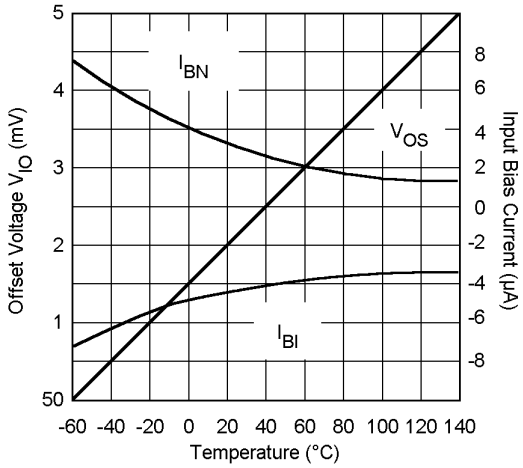


Figure 17.

Typical DC Errors Mismatch vs. Temp

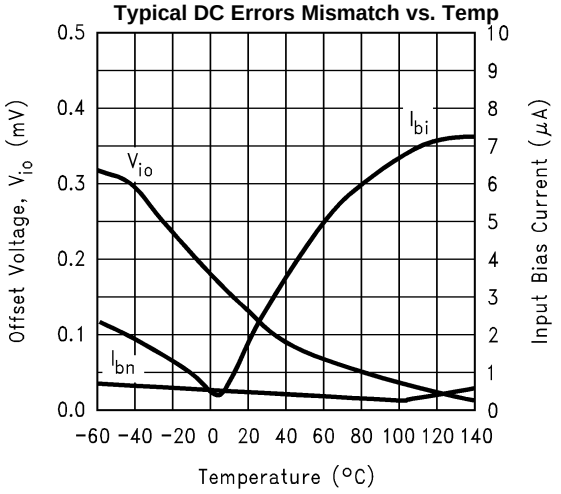


Figure 18.

Open-Loop Transimpedance, Z(s)

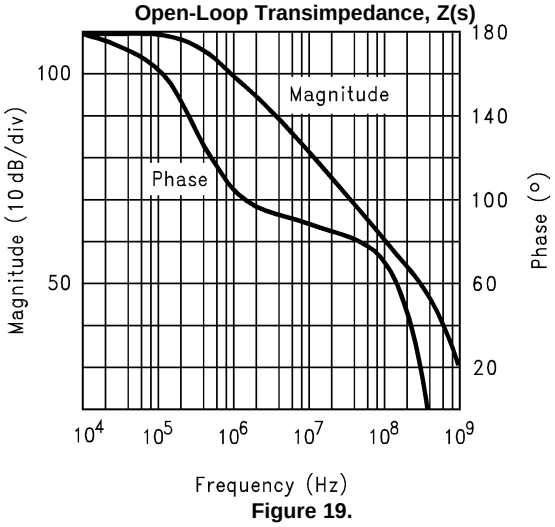


Figure 19.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(T_A = 25°C, V_{CC} = ±5V, A_V = ±2V/V, R_f = 634Ω, R_L = 100Ω, Unless Specified).

Equivalent Input Noise

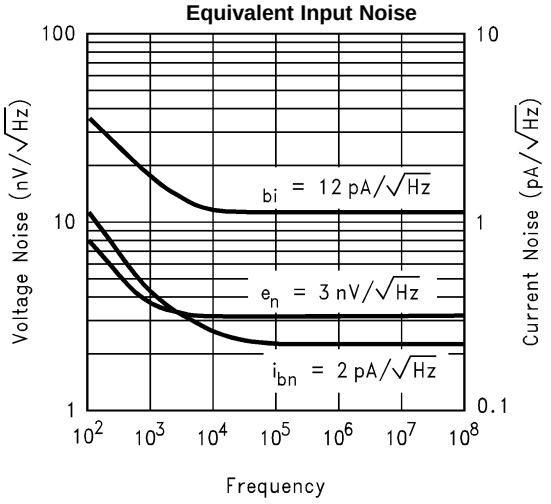


Figure 20.

Total Input-Referred Noise vs. Gain

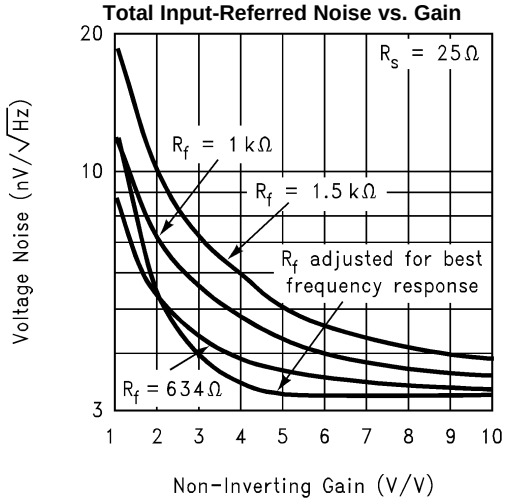


Figure 21.

Differential Gain vs. Frequency

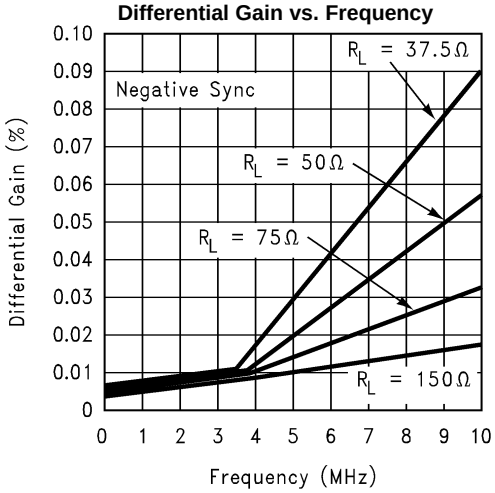


Figure 22.

2nd Harmonic Distortion

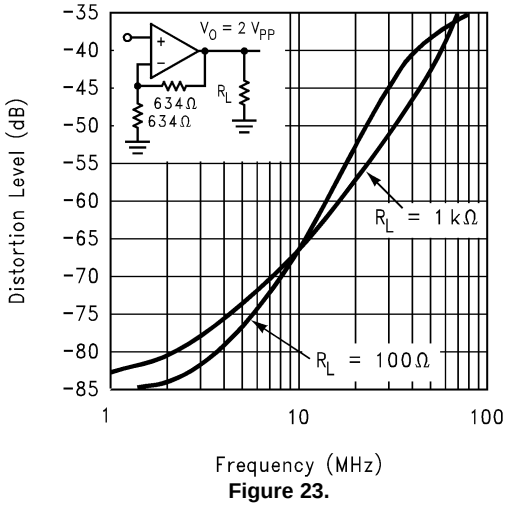


Figure 23.

Group Delay Variation

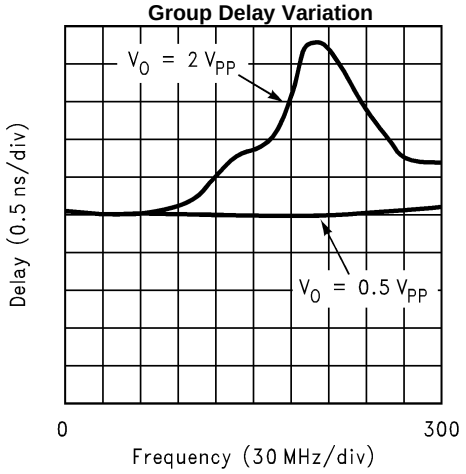


Figure 24.

Differential Phase vs. Frequency

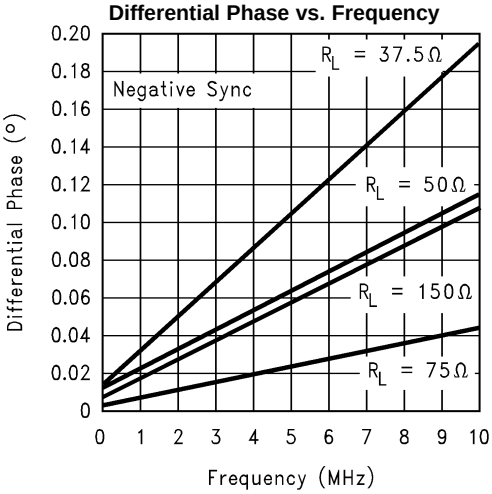


Figure 25.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(T_A = 25°C, V_{CC} = ±5V, A_V = ±2V/V, R_f = 634Ω, R_L = 100Ω, Unless Specified).

3rd Harmonic Distortion

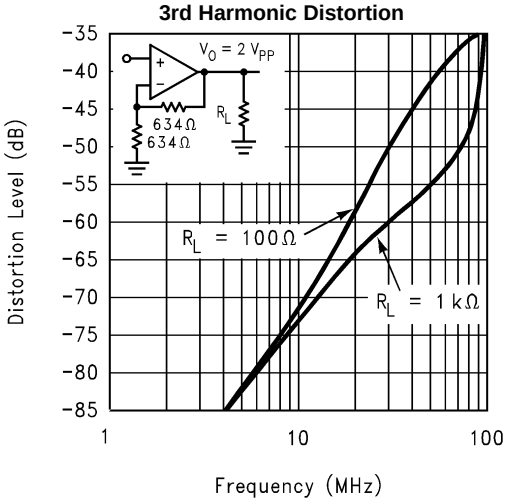


Figure 26.

2nd Harmonic Distortion vs. P_{OUT}

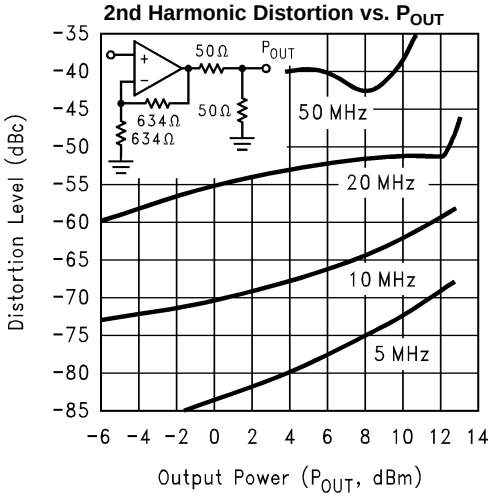


Figure 27.

PSRR, CMRR and Closed Loop R_O

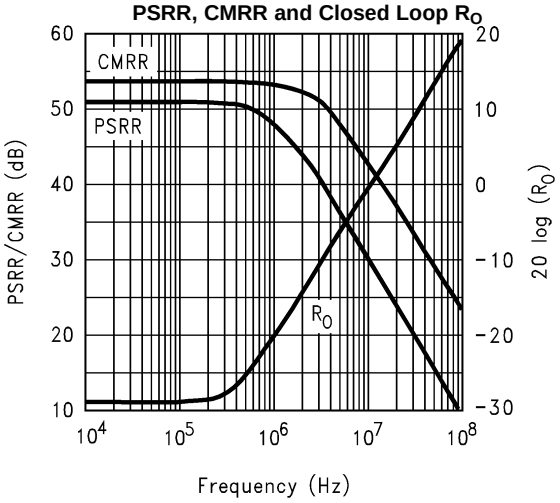


Figure 28.

2-Tone, 3rd Order Intermod Intercept

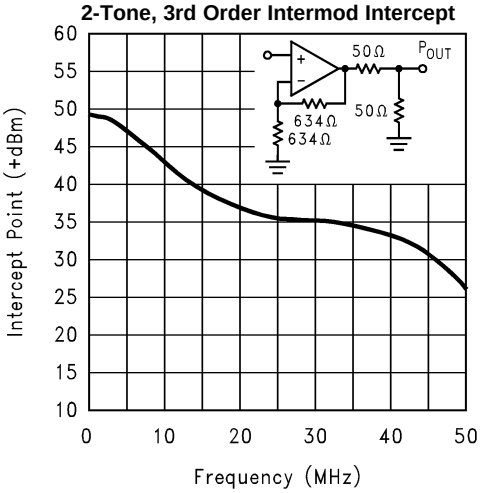


Figure 29.

3rd Harmonic Distortion vs. P_{OUT}

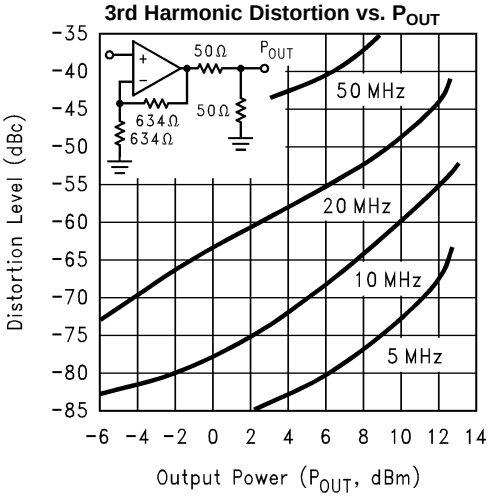


Figure 30.

−3dB Bandwidth Variation Over Process

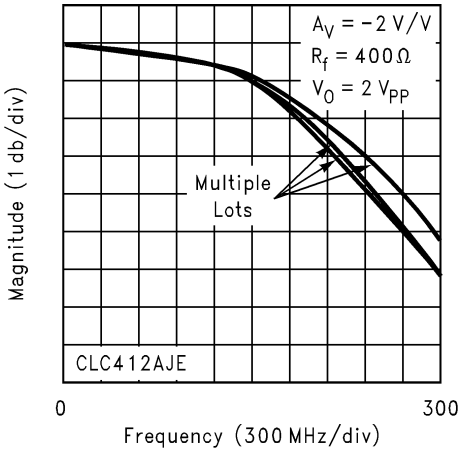


Figure 31.

APPLICATION DIVISION

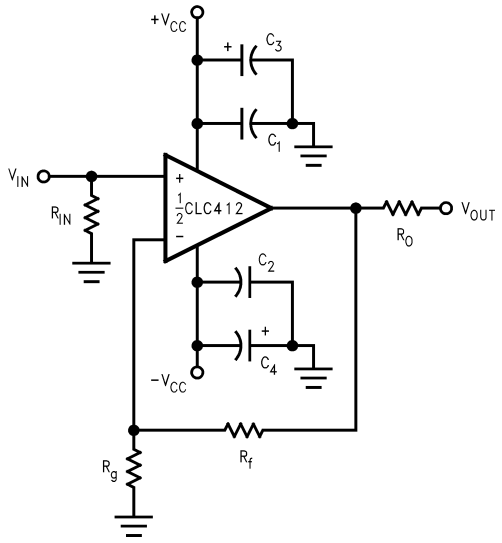


Figure 32.

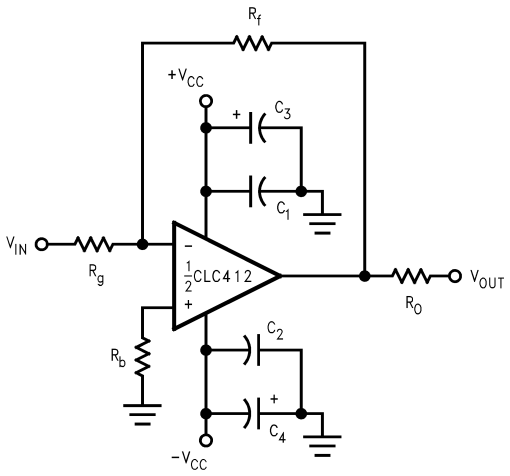


Figure 33.

Application Introduction

Offered in an 8-pin package for reduced space and cost, the wideband CLC412 dual current-feedback op amp provides closely matched DC & AC electrical performance characteristics making the part an ideal choice for wideband signal processing. Applications such as broadcast quality video systems, IQ amplifiers, filter blocks, high speed peak detectors, integrators and transimpedance amplifiers will all find superior performance in the CLC412 dual op amp.

Feedback Resistor Selection

The loop gain and frequency response for a current-feedback operational amplifier is determined largely by the feedback resistor, R_f. The ELECTRICAL CHARACTERISTICS and TYPICAL PERFORMANCE CHARACTERISTICS plots specify an R_f of 634Ω, a gain of +2V/V and operation with ±5V power supplies (unless otherwise stated). Generally, lowering R_f from its recommended value will peak the frequency response and extend the bandwidth while increasing its value will roll off the response. Reducing the value of R_f too far below its recommended value will cause overshoot, ringing and eventually oscillation.

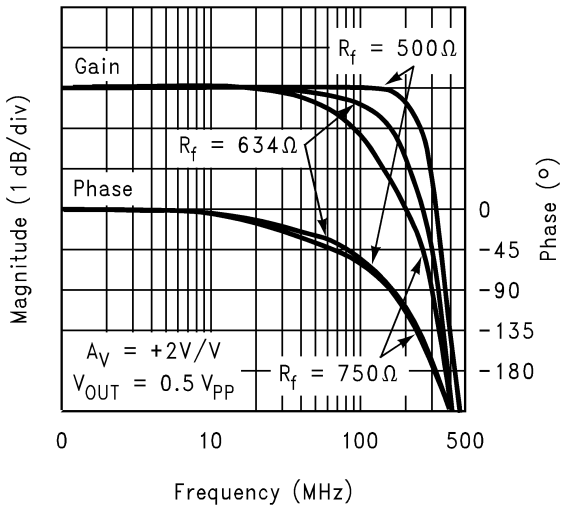


Figure 34. Frequency Response vs. R_f

The plot above (Figure 34), labeled “Frequency Response vs. R_f” shows the CLC412's frequency and phase response as R_f is varied while the gain remains constant at +2V/V (R_L = 100Ω). This plot shows that one particular value of R_f will optimize the frequency and phase response at the specified gain setting, i.e. 634Ω at a gain of +2V/V. Current-feedback op amps, unlike voltage-feedback op amps, have a direct relationship between their frequency and phase response to the value of the feedback resistor, R_f. For more information see Application Note OA-13 which describes the relationship between R_f and closed-loop frequency response.

When configuring the CLC412 for other inverting or non-inverting gains, it is necessary to adjust the value of the feedback resistor in order to optimize the device's frequency and phase response. The two plots below provide the means of selecting the recommended feedback resistor value for both inverting and non-inverting gain selections.

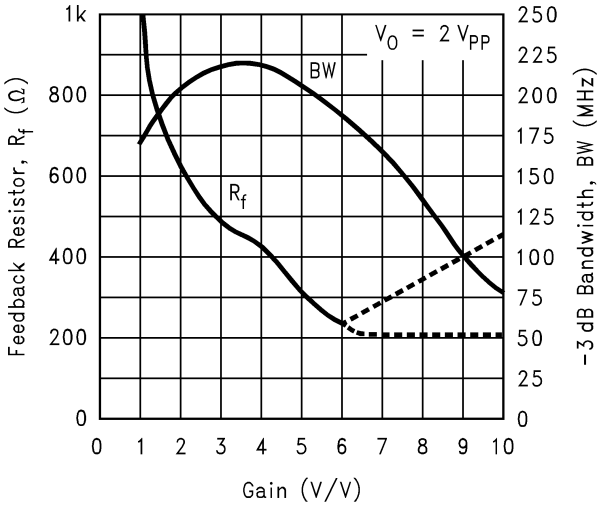


Figure 35. R_f vs. Non-Inverting Gain (AJE & AJP)

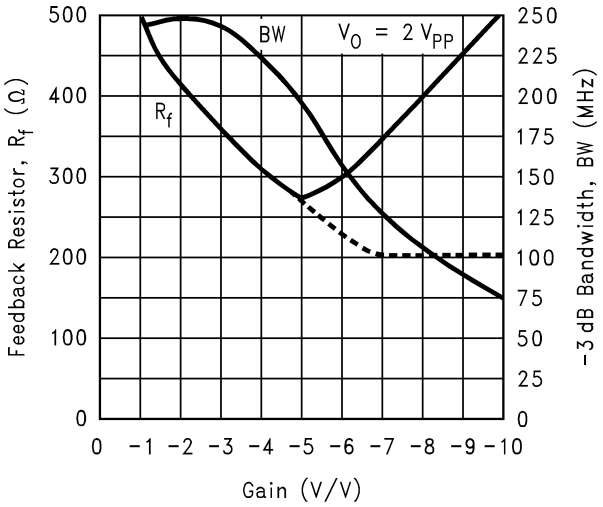


Figure 36. R_f vs. Inverting Gain (AJE & AJP)

Both plots show the value of R_f approaching a non-zero minimum (dashed line) at high gains, which is characteristic of current-feedback op amps, while the linear portion of the two (solid) curves (i.e., -5 > A_V > +6) results from the limitation placed on R_g (i.e., $R_g \geq 50\Omega$). This limitation is due to the desire to keep R_g greater in value than that of the inverting input resistance. Therefore, the resulting small-signal bandwidth curves, labeled "BW", correspond to the two (solid) "R_f" curves. These results may deviate from that produced by the analysis of OA-13 since these plots were produced from an actual board layout that included parasitic capacitances not accounted for by the analysis of OA-13. It should be noted that a non-inverting gain of +1V/V requires an R_f = 1kΩ and the output voltage used for both plots is $2V_{PP}$.

In order to bandlimit the CLC412 at any particular gain setting, a larger value of R_f (than previously recommended in the plots above) is needed. Following the analysis in OA-13, we find the CLC412's "optimum feedback transimpedance", Z_t*, below.

$$Z^*_t = R_f + R_{IN}\left[1 + \frac{R_f}{R_g}\right]$$

$$= 634 + 60\left[1 + \frac{634}{634}\right]$$

$$= 754\Omega$$

$$20\log(754) = 57.5\text{dB} \quad (1)$$

The "optimum feedback transimpedance" is unique for each current-feedback op amp and determines the recommended value of R_f for a particular gain setting. Drawing a horizontal line on the "Open-loop Transimpedance, Z(s)" plot from 57.5dB (on the left vertical axis), we find the intersection with the transimpedance magnitude trace occurs at a frequency of 180MHz. This frequency is only an approximation of the CLC412's small-signal bandwidth. From this intersection, one can see that an increase in Z_t will produce a new intersection occurring at a lower frequency. This is the process to follow when bandlimiting. Once the target small-signal bandwidth is determined, the new value of Z_t is picked off the graph at the point where this frequency and the transimpedance magnitude trace intersect. One can then back track to figure the value of the feedback resistor, $R_f = Z_t - R_{in}(1 + R_f/R_g)$. This new value of R_f will produce the desired frequency roll-off.

Circuit Layout

With all high frequency devices, board layouts with stray capacitances have a strong influence over AC performance. The CLC412 is no exception and its input and output pins are particularly sensitive to the coupling of parasitic capacitances (to AC ground) arising from traces or pads placed too closely (<0.1”) to power or ground planes. In some cases, due to the frequency response peaking caused by these parasitics, a small adjustment of the feedback resistor value will serve to compensate the frequency response. Also, it is very important to keep the parasitic capacitance across the feedback resistor to an absolute minimum.

The performance plots in the data sheet can be reproduced using the evaluation boards available from Texas Instruments. There are two types of boards; the PDIP (#730038) and SOIC (#730036). The #730036 board uses all SMT parts for the evaluation of the CLC412 in its surface mount package. Either of these layouts can assist the designer in obtaining the desired performance. In addition, the boards can serve as an example layout for the final production printed circuit board.

Care must also be taken with the CLC412's layout in order to achieve the best circuit performance, particularly channel-to-channel isolation. The decoupling capacitors (both tantalum and ceramic) must be chosen with good high frequency characteristics to decouple the power supplies and the physical placement of the CLC412's external components is critical. Grouping each amplifier's external components with their own ground connection and separating them from the external components of the opposing channel with the maximum possible distance is recommended. The input (R_{in}) and gain setting resistors (R_f) are the most critical. It is also recommended that the ceramic decoupling capacitor (0.1µF chip or radial-leaded with low ESR) should be placed as closely to the power pins as possible.

Package Parasitics

In addition to the parasitic capacitances arising from the board layout, each of the CLC412's packages has its own characteristic set of parasitic capacitances and inductances causing frequency response variation from package to package as shown in the plot below (Figure 37), labeled “Frequency Response vs. Package Type”. Due to its much smaller size, the CLC412AJE (8-pin SOIC) shows the least amount of peaking.

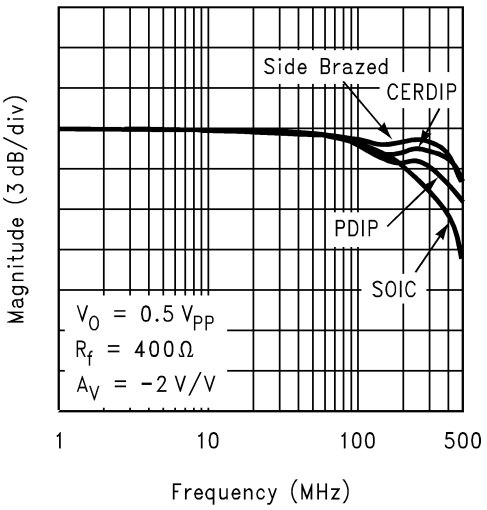


Figure 37. Frequency Response vs. Package Type

Matching Performance

With proper board layout, the AC performance match between the two CLC412's amplifiers can be tightly controlled as shown in TYPICAL PERFORMANCE CHARACTERISTICS plot labeled “Small-Signal Channel Matching”.

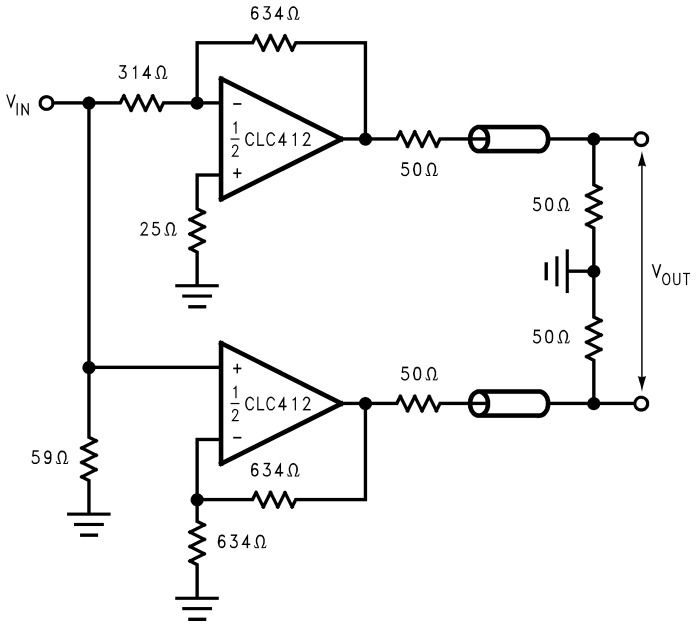


Figure 38.

The measurements were performed with SMT components using the recommended value of feedback resistor of 634Ω at a gain of +2V/V. The pulse response plot labeled “Pulse Matching” found below shows the group delay matching between amplifiers of the CLC412. The circuit topology is described in Figure 38.

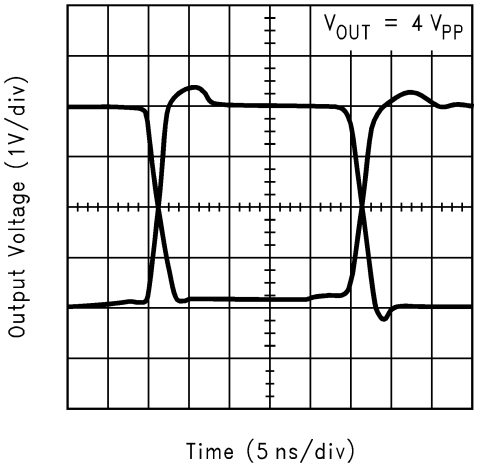


Figure 39. Large Signal Pulse Response

The CLC412's amplifiers, built on the same die, provide the advantage of having tightly matched DC characteristics. The typical DC matching specifications of the CLC412 are:

ΔVio = ±0.60mV, Δlbn = ±0.25μA, Δlbi = ±1.5μA.

Slew Rate and Settling Time

One of the advantages of current-feedback topology is an inherently high slew rate which produces a wider full power bandwidth. The CLC412 has a typical slew rate of 1300V/μs. The required slew rate for a design can be calculated by the following equation:

$$SR = 2\pi f V_{pk} \quad (2)$$

Careful attention to parasitic capacitances is critical to achieving the best settling time performance. The CLC412 has a typical short term settling time of 0.05% of 12ns for a 2V step. Also, the amplifier is virtually free of any long term thermal tail effects at low gains as shown in the TYPICAL PERFORMANCE CHARACTERISTICS plot labeled "Long Term Settling Time."

When measuring settling time, a solid ground plane should be used in order to reduce ground inductance which can cause common-ground-impedance coupling. Power supply and ground trace parasitic capacitances and the load capacitance will also affect settling time.

Placing a series resistor (R_s) at the output pin is recommended for optimal settling time performance when driving a capacitive load. The TYPICAL PERFORMANCE CHARACTERISTICS plot labeled "R_s and Settling Time vs. Capacitive Load" provides a means for selecting a value of R_s for a given capacitive load. The plot also shows the resulting settling time to 0.05% and 0.01%.

DC & Noise Performance

A current-feedback amplifier's input stage does not have equal nor correlated bias currents, therefore they cannot be canceled and each contributes to the total DC offset voltage at the output by the following equation:

$$V_{OFFSET} = \pm \left[I_{BN} \times R_S \left[1 + \frac{R_f}{R_g} \right] + V_{IO} \left[1 + \frac{R_f}{R_g} \right] + I_{BI} \times R_f \right] \quad (3)$$

The input resistor R_{in} is the resistance looking from the non-inverting input back toward the source. For inverting DC-offset calculations, the source resistance seen by the input resistor R_g must be included in the output offset calculation as a part of the non-inverting gain equation. Application note OA-7 gives several circuits for DC offset correction. The noise currents for the inverting and non-inverting inputs are graphed in the TYPICAL PERFORMANCE CHARACTERISTICS plot labeled "Equivalent Input Noise". A more complete discussion of amplifier input-referred noise and external resistor noise contribution can be found in OA-12.

Differential Gain & Phase

The CLC412 can drive multiple video loads with very low differential gain and phase errors. The TYPICAL PERFORMANCE CHARACTERISTICS plots labeled "Differential Gain vs. Frequency" and "Differential Phase vs. Frequency" show performance for loads from 1 to 4. The ELECTRICAL CHARACTERISTICS table also specifies ensured performance for one 150Ω load at 4.43MHz. For NTSC video, the ensured performance specifications also apply. Application note OA-08, "Differential Gain and Phase for Composite Video Systems", describes in detail the techniques used to measure differential gain and phase.

I/O Voltage & Output Current

The usable common-mode input voltage range (CMIR) of the CLC412 specified in the ELECTRICAL CHARACTERISTICS table of the data sheet shows a range of ±2.2 volts. Exceeding this range will cause the input stage to saturate and clip the output signal.

The output voltage range is determined by the load resistor and the choice of power supplies. With ±5 volts the class A/B output driver will typically drive +3.1/-2.7 volts into a load resistance of 100Ω. Increasing the supply voltages will change the common-mode input and output voltage swings while at the same time increase the internal junction temperature. The output voltage for different load resistors can be determined from the data sheet plots labeled "Frequency Response vs. Load (R_L)" and "Maximum Output Swing vs. Frequency".

Applications Circuits

Single-to-Differential Line Driver

The CLC412's well matched AC channel-response allows a single-ended input to be transformed to highly matched push-pull driver. From a 1V single-ended input the circuit of Figure 40 produces 1V differential signal between the two outputs. For larger signals the input voltage divider ($R_1 = 2R_2$) is necessary to limit the input voltage on channel 2. To achieve the same performance when driving a matched load, see Figure 38.

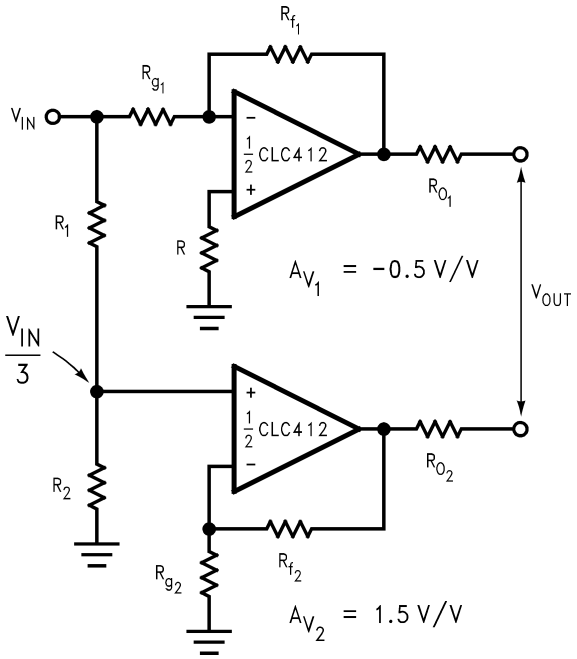


Figure 40.

Differential Line Receiver. Figure 41 and Figure 42 show two different implementations of an instrumentation amplifier which convert differential signals to single-ended. Figure 42 allows CMRR adjustment through R_2.

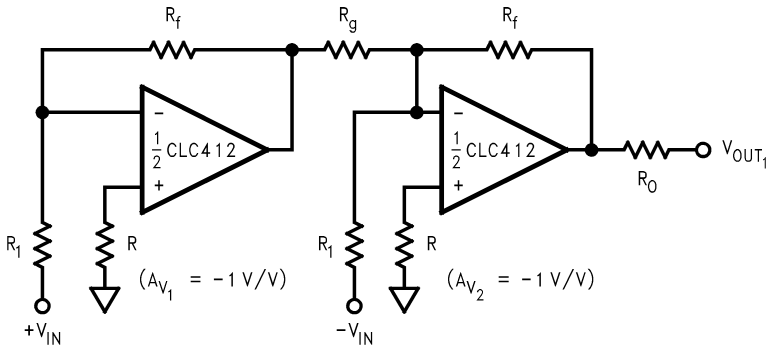


Figure 41.

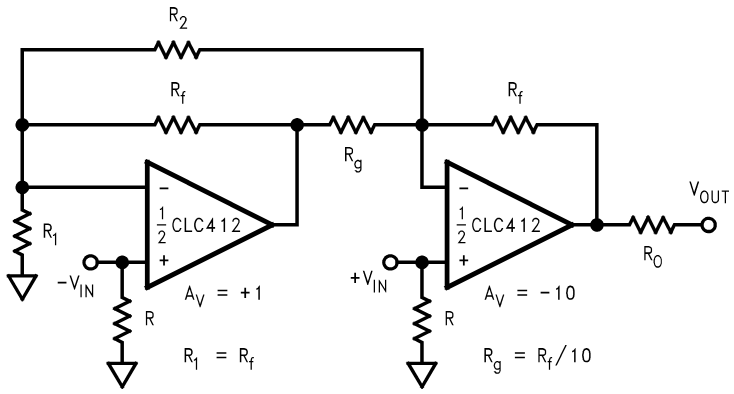


Figure 42.

High Speed Instrumentation Amplifier

For applications requiring higher CMRR the composite circuit of Figure 43 uses the two amplifiers of the CLC412 to create balanced inputs for the CLC420 voltage-feedback op amp. The DC CMRR can be fine tuned through the adjustment of R_b. Further improvement of CMRR over frequency can be achieved through the placement of an RC network between the outputs (A and B) of the two amplifiers of the CLC412.

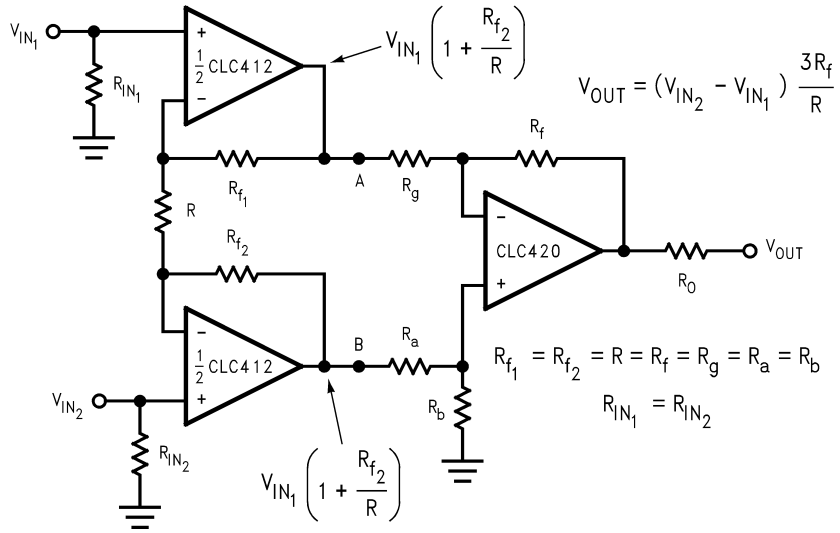


Figure 43.

Non-Inverting Current-Feedback Integrator

The circuit of Figure 44 achieves its high speed integration by placing one of the CLC412's amplifiers in the feedback loop of the second amplifier configured as shown.

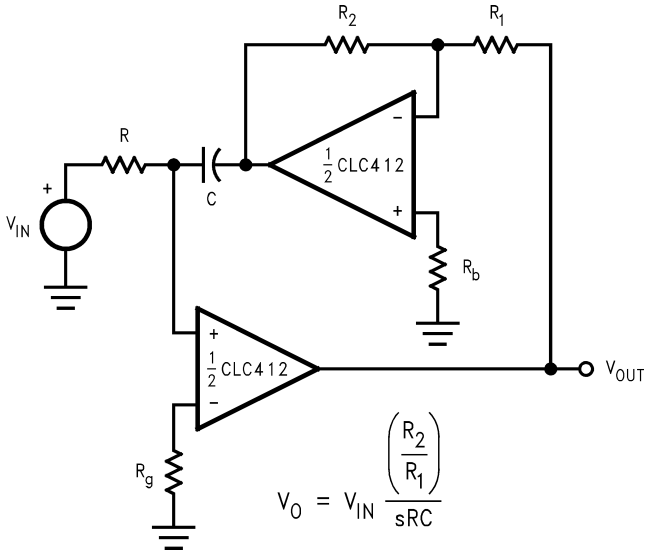


Figure 44.

Low Noise Wide-Bandwidth Transimpedance Amplifier

Figure 45 implements a low noise transimpedance amplifier using both channels of the CLC412. This circuit takes advantage of the lower input bias current noise of the non-inverting input and achieves negative feedback through the second CLC412 channel. The output voltage is set by the value of R_f while frequency compensation is achieved through the adjustment of R_T.

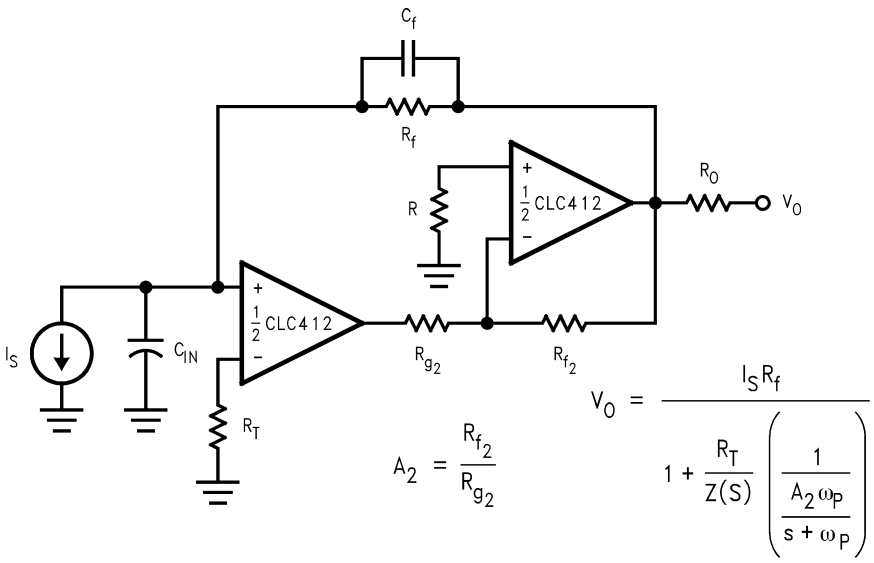


Figure 45.

Buffered 2nd-Order Sallen-Key Low-Pass Filter

Figure 46 shows one implementation of a 2nd order Sallen-Key low pass filter buffered by one of the CLC412's channels. The CLC412 enables greater precision since it provides the advantage of very low output impedance and very linear phase throughout the pass band.

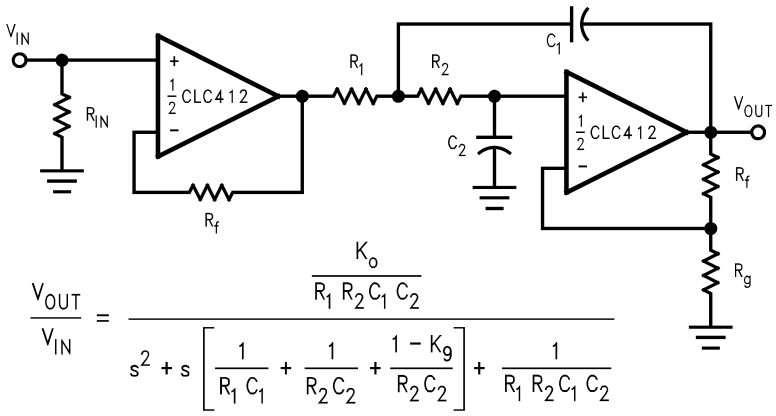


Figure 46.

REVISION HISTORY

Changes from Revision C (April 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	18

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