CLC533

CLC533 High Speed 4:1 Analog Multiplexer

Literature Number: SNOS834A

December 2001

National Semiconductor

CLC533
High Speed 4:1 Analog Multiplexer

General Description

The CLC533 is a high speed 4:1 multiplexer employing active input and output stages. The CLC533 innovative closed loop design dramatically improves accuracy over conventional analog multiplexer circuits. This monolithic device is constructed using an advanced high performance bipolar process.

The CLC533 has been specifically designed to provide a 17ns settling time to 0.01%. Fast settling time, coupled with adjustable bandwidth, and channel-to-channel isolation of 80dB @ 10MHz makes the CLC533 an ideal choice for infrared and CCD imaging systems. Low distortion and spurious signal levels (−80dBc) make the CLC533 a very suitable choice for I/Q processors in radar receivers.

The CLC533 is offered in two industrial versions, CLC533AJP\AJE specified from −40˚C to +85˚C and are packaged in 16-pin plastic DIP and SOIC packages.

Enhanced solutions (Military/Aerospace

SMD Number: 5962-93203

*Space level versions also available.

*For more information, visit http://www.national.com/

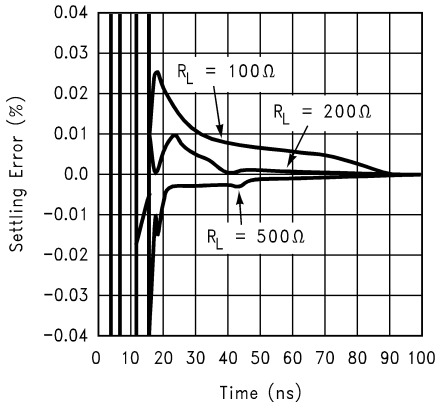
Features

- 17ns 12-bit settling time to .01%
- Low noise – 42µVrms
- High Isolation – 80dBc @ 10MHz
- 110MHz – 3dB bandwidth (A_V = +2)
- Low distortion – 80dBc @ 5MHz
- Adjustable bandwidth –180MHz (max)

Applications

- Infrared system multiplexing
- CCD sensor signals
- Radar I/Q switching
- High definition video HDTV
- Test and calibration

Settling Time vs. Load



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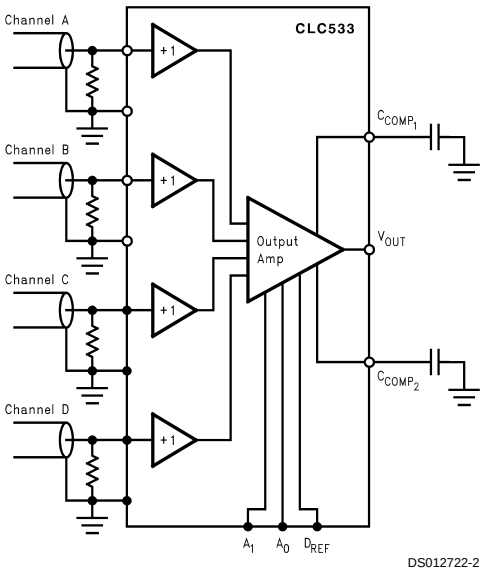
Functional Diagram

A_1	A_0	OUT
0	0	A
0	1	B
1	0	C
1	D	D

ECL Mode – D_{REF} = open
TTL Mode – D_{REF} = +5V



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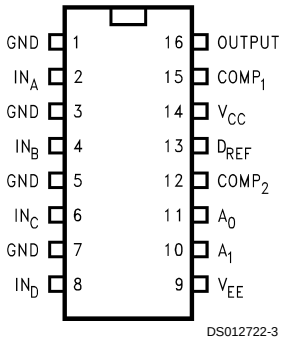
Connection Diagram



Pinout
DIP & SOIC

Ordering Information

Package	Temperature Range Industrial	Part Number	Package Marking	NSC Drawing
16-Pin Plastic DIP	−40˚C to +85˚C	CLC533AJP	CLC533AJP	N16E
16-Pin Plastic SOIC	−40˚C to +85˚C	CLC533AJE	CLC533AJE	M16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Positive Supply Voltage ($+V_{CC}$)	−0.5V to −7.0V
Negative Supply Voltage ($-V_{EE}$)	+0.5V to −7.0V
Differential Voltage between any two GND's	200mV
Analog Input Voltage Range	$-V_{EE}$ to $+V_{CC}$
Digital Input Voltage Range	$-V_{EE}$ to $+V_{CC}$
Output Short Circuit Duration (Shorted to GND)	Infinite
Junction Temperature	+150˚C
Operating Temperature Range	
CLC533AJP/AJE	−40˚C to +85˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Solder Duration (+300˚C)	10sec
ESD Rating (Human Body Model)	<500V

Recommended Operating Conditions

Positive Supply Voltage ($+V_{CC}$)	+5.0V
Negative Supply Voltage ($-V_{EE}$)	−5.2V or −5.0V
Differential Voltage Between any two GND's	10mV
Analog Input Voltage Range	±2V
A_X Input Voltage Range (TTL Mode)	0V to +5.0V
A_X Input Voltage Range (ECL Mode)	0V to −2.0V
C_{COMP} Range	5pF to 100pF

Operating Ratings

Thermal Resistance

Package	(θ_{JC})	(θ_{JA})
MDIP	45˚C/W	95˚C/W
SOIC	35˚C/W	100˚C/W

Electrical Characteristics

(Unless otherwise specified, all limits guaranteed for T_J= 25˚C, $+V_{CC}$ = +5.0 V; $-V_{EE}$ = −5.2V; R_{in} = 50Ω; R_L = 500Ω; C_{COMP} = 8pf; ECL Mode, pin 13 = NC)

Symbol	Parameters	Conditions	Typ	Max/Min Ratings (Note 2)			Units
Ambient Temperature		CLC533AJP/AJE	+25˚C	−40˚C	+25˚C	+85˚C	
Frequency Domain Response							
SSBW	-3dB Bandwidth	$V_{OUT} < 0.1V_{PP}$	180	130	130	110	MHz
LSBW		$V_{OUT} = 2V_{PP}$	45	35	35	30	MHz
	Gain Flatness	$V_{OUT} < 0.1V_{PP}$					
GFP	Peaking	0.1MHz to 200MHz	0.2	0.5	0.5	0.5	dB
GFR	Rolloff	0.1MHz to 100MHz	1.0	2.0	2.0	3.0	dB
LPD	Linear Phase Deviation	DC to 100MHz	2.0				deg
CT10	Crosstalk Rejection - 1 Channel	$2V_{PP}$, 10MHz	80	74	74	74	dB
CT20		$2V_{PP}$, 20MHz	74	68	68	68	dB
CT30		$2V_{PP}$, 30MHz	68	62	62	62	dB
3CT10	Crosstalk Rejection - 3 Channel	$2V_{PP}$, 10MHz	80	74	74	74	dB
3CT20		$2V_{PP}$, 20MHz	74	68	68	68	dB
3CT30		$2V_{PP}$, 30MHz	68	62	62	62	dB
Time Domain Performance							
TRS	Rise and Fall Time	0.5V Step	2.7	3.3	3.3	3.8	ns
TRL		2V Step	10	12.5	12.5	14.5	ns
TSP	Settling Time (Note 2)	±0.01%	17	24	24	27	ns
TSS	2V Step	±0.1%	13	18	18	21	ns
OS	Overshoot	2.0V Step	2	5	5	6	%
SR	Slew Rate		160	130	130	110	V/µs
Switch Performance							
SWT10	Channel to Channel Switching Time (2V Step at Output)	50% SELECT to 10% V_{OUT}	6	8	8	9	ns
SWT90		50% SELECT to 90% V_{OUT}	16	21	21	24	ns
ST	Switching Transient		30				mV
Distortion And Noise Performance							
HD2	2nd Harmonic Distortion	$2V_{PP}$, 5MHz	80	67	67	67	dBc
HD3	3rd Harmonic Distortion	$2V_{PP}$, 5MHz	86	67	67	67	dBc
	Equivalent Input Noise						

Electrical Characteristics (Continued)

(Unless otherwise specified, all limits guaranteed for T_J= 25˚C, $+V_{CC}$ = +5.0 V; $-V_{EE}$ = −5.2V; R_{in} = 50Ω; R_L = 500Ω; C_{COMP} = 8pf; ECL Mode, pin 13 = NC)

Symbol	Parameters	Conditions	Typ	Max/Min Ratings (Note 2)			Units
Distortion And Noise Performance							
SNF	Spot Noise Voltage	>1MHz	4.2				$nV/\sqrt{Hz}$
INV	Integrated Noise	1MHz to 100MHz	42	54		51	MVrms
SNF	Spot Noise Current		5				$pA/\sqrt{Hz}$
Static and DC Performance							
VOS	Analog Output Offset (Note 3)		1	2.5	3.5	4.5	mV
DVIO	Temperature Coefficient		15	75		20	µV/˚C
IBN	Analog Input Bias Current (Note 3)		50	280	120	120	µA
DIBN	Temperature Coefficient		0.3	2.0		0.8	µA/˚C
RIN	Analog Input Resistance		200	75	120	120	kΩ
CIN	Analog Input Capacitance		2	3.0	2.5	2.5	pF
GA	Gain Accuracy (Note 3)	±2V	0.994	0.988	0.988	0.988	V/V
ILIN	Integral End point Linearity	±1V (Full Scale)	0.02	0.05	0.03	0.03	%FS
VO	Output Voltage	No Load	±3.4	2.4	2.8	2.8	V
IO	Output Current		45	20	50	50	mA
RO	Output Resistance	DC	1.5	4.0	2.5	2.5	Ω
Digital Input Performance							
	ECL Mode (D_{REF} Floating)						
VIH1	Input Voltage Logic HIGH			−1.1	−1.1	−1.1	V
VIL1	Input Voltage Logic LOW			−1.5	−1.5	−1.5	V
IIH1	Input Current Logic HIGH		200	220	80	80	µA
IIL1	Input Current Logic LOW		200	220	80	80	µA
	TTL Mode (D_{REF} = +5V)						
VIH2	Input Voltage Logic HIGH			2.0	2.0	2.0	V
VIL2	Input Voltage Logic LOW			0.8	0.8	0.8	V
IIH2	Input Current Logic HIGH		200	220	80	80	µA
IIL2	Input Current Logic LOW		200	220	80	80	µA
Power Requirements							
ICC	Supply Current ($+V_{CC}$ = +5.0V) (Note 3)	No Load	28	38	36	36	mA
IEE	Supply Current ($-V_{EE}$ = −5.2V) (Note 3)	No Load	28.5	39	37	37	mA
PD	Nominal Power Dissipation	No Load	288				mW
PSRR	Power Supply Rejection Ratio (Note 3)			−53	−60	−60	dB

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

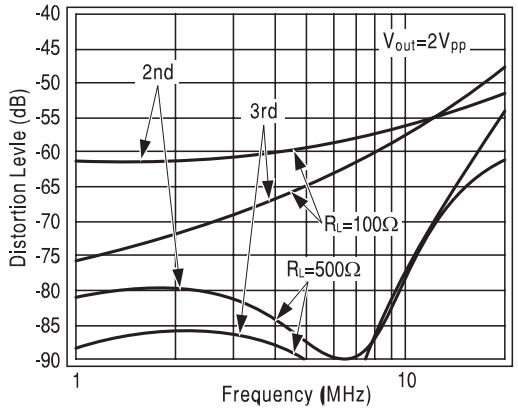
Note 3: AJ : 100% tested at T_J = +25˚C.

Note 4: Settling time measured from the 50% analog output transition.

Note 5: Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to maximum rating for extended periods may affect device reliability.

Typical Performance Characteristics (T_A = 25°C, $+V_{CC}$ = 5V, $-V_{EE}$ = −5.2V, R_L = 500Ω unless specified)

Small-Signal Gain & Phase vs. Load



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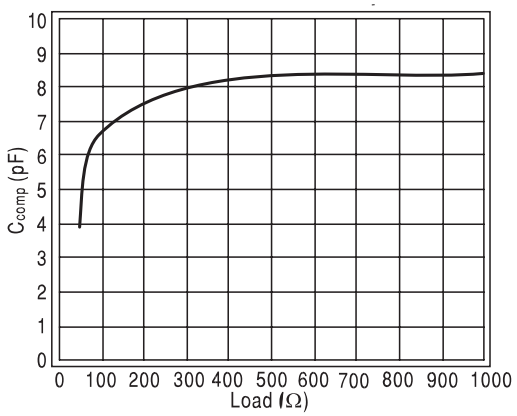
Recommended Compensation Cap vs. Load



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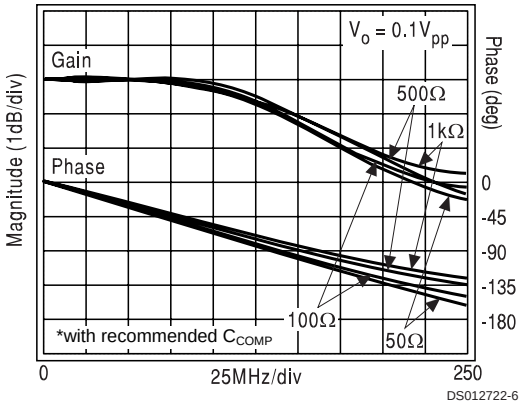
Small Signal Gain/Phase vs. Load



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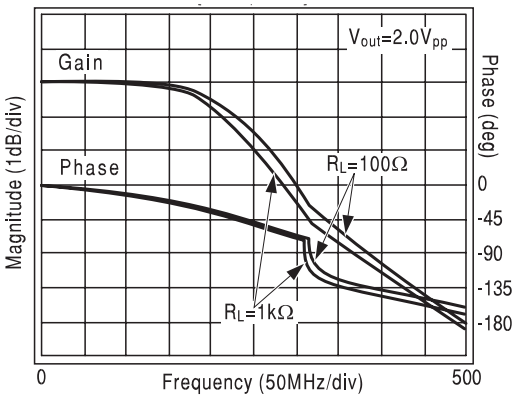
Large-Signal Frequency Response vs. Load



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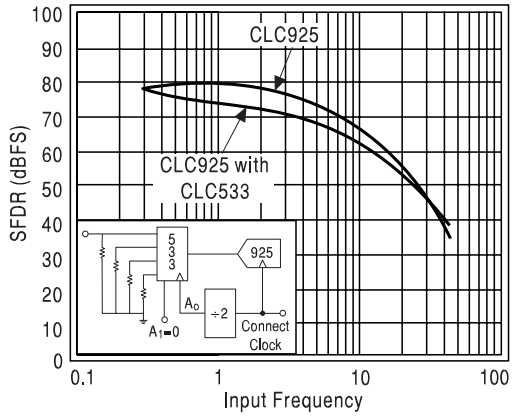
Switch Mode Distortion



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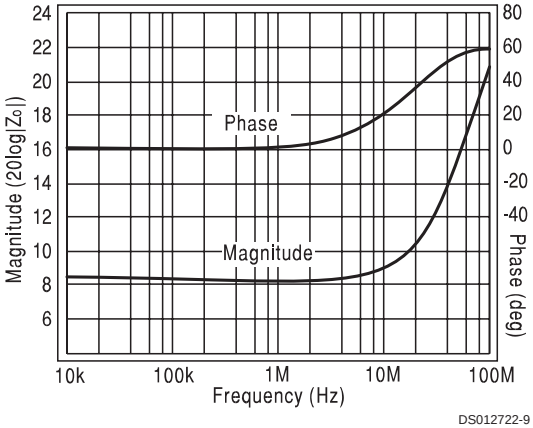
Output Impedance



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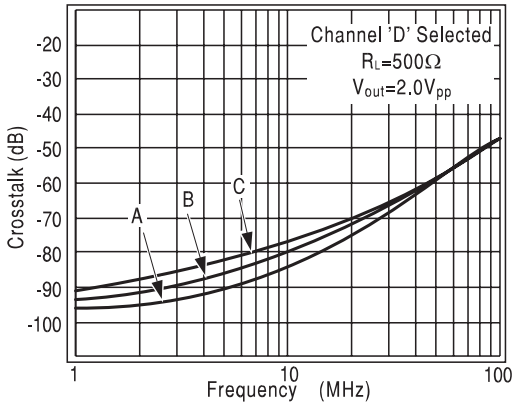
Typical Performance Characteristics (T_A = 25°C, $+V_{CC}$ = 5V, $-V_{EE}$ = −5.2V, R_L = 500Ω unless specified) (Continued)

Channel-Channel Crosstalk



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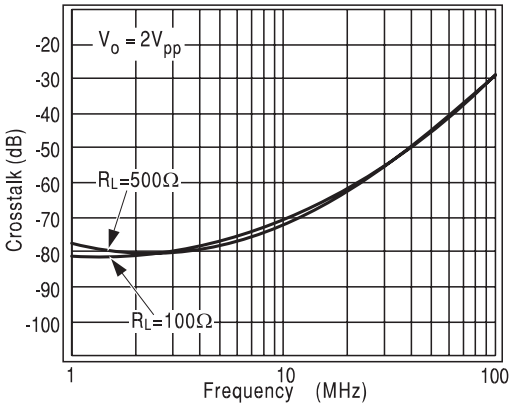
All Hostile Channel-to-Channel Crosstalk



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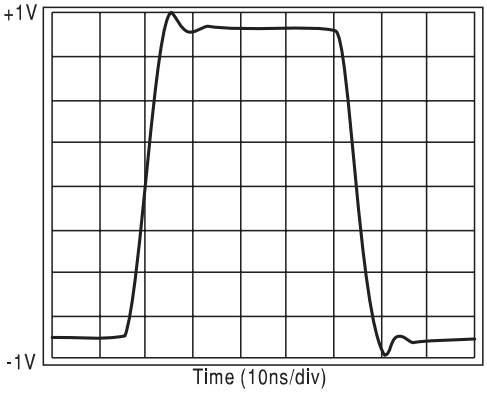
Digitalized Pulse Response



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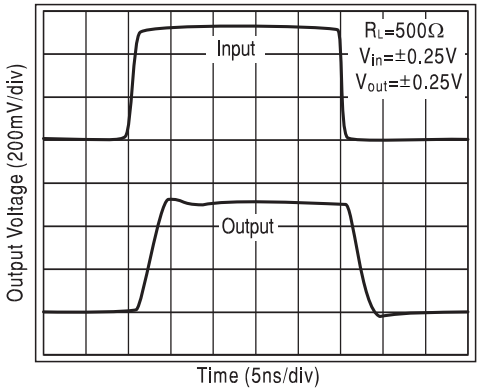
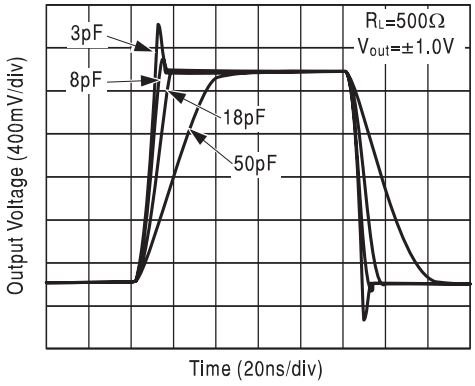
Small-Signal Pulse Response



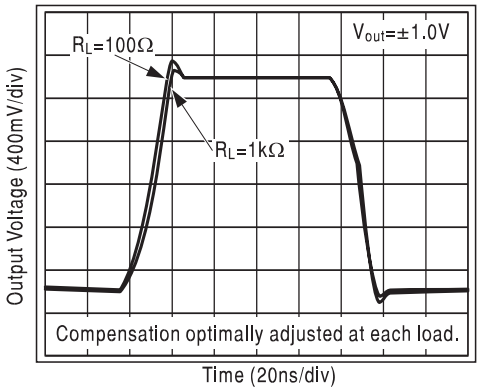
DS012722-13

Large-Signal Pulse Response vs. C_{comp}



DS012722-14

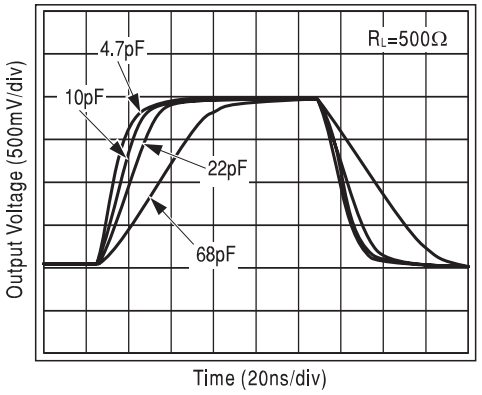
Large-Signal Pulse Response vs. Load



DS012722-15

Typical Performance Characteristics (T_A = 25°C, $+V_{CC}$ = 5V, $-V_{EE}$ = −5.2V, R_L = 500Ω unless specified) (Continued)

Switched Pulse Response vs. C_{comp}



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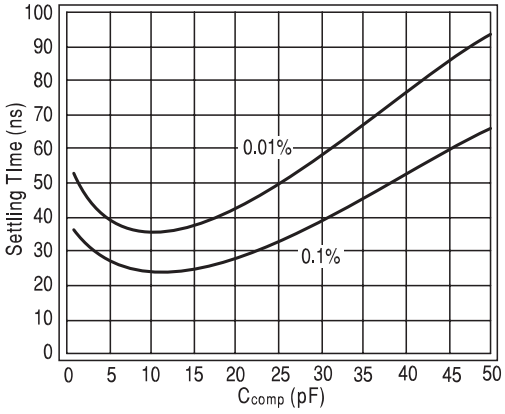
Settling Time vs. C_{comp}



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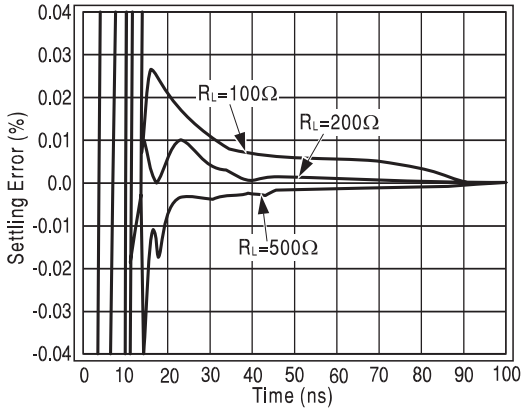
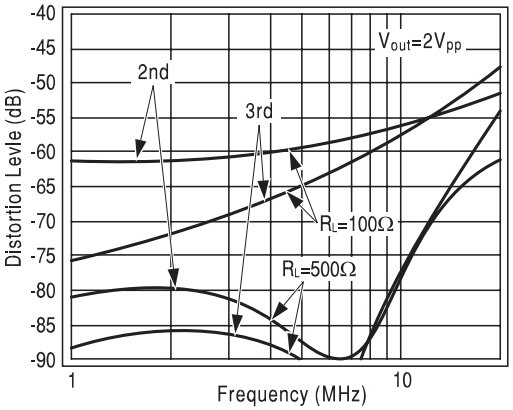
Settling Time vs. Load



DS012722-18

2nd & 3rd Harmonic Distortion



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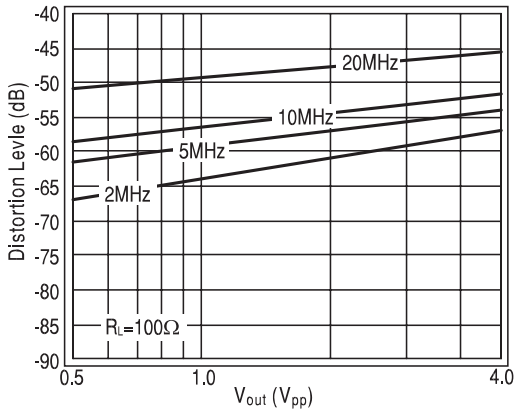
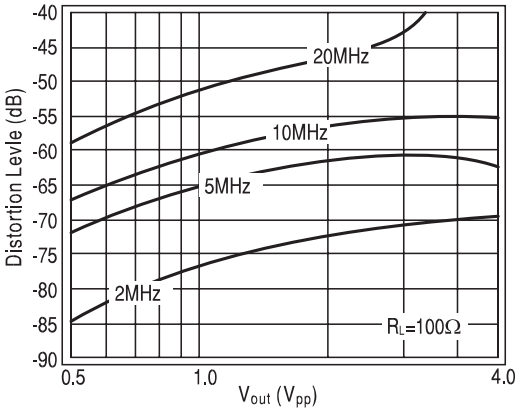
2nd Harmonic Distortion vs. V_{out}



DS012722-20

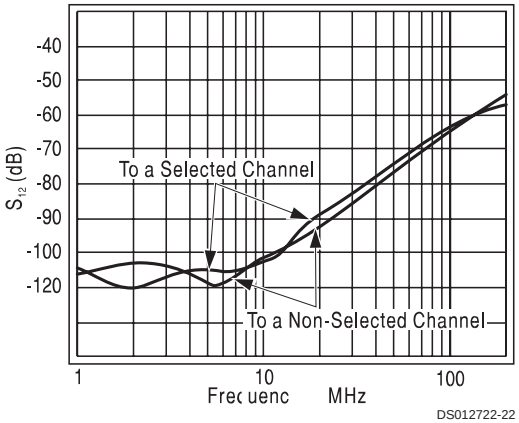
3rd Harmonic Distortion vs. V_{out}



DS012722-21

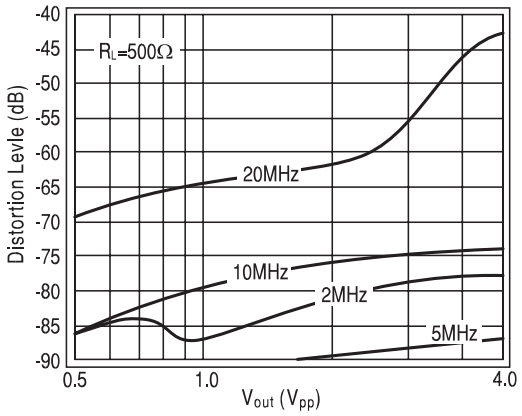
Typical Performance Characteristics (T_A = 25˚C, $+V_{CC}$ = 5V, $-V_{EE}$ = −5.2V, R_L = 500Ω unless specified) (Continued)

Reverse Transmission (S_{12})



DS012722-22

2nd Harmonic Distortion vs. V_{out}



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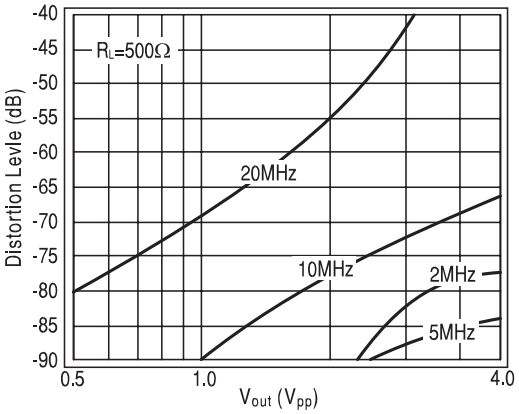
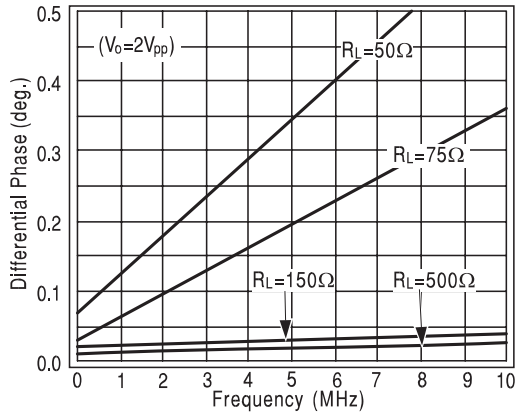
3rd Harmonic Distortion vs. V_{out}



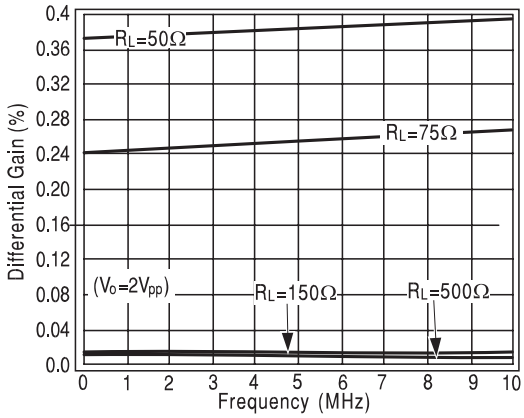
DS012722-24

Differential Phase (Negative Sync.)



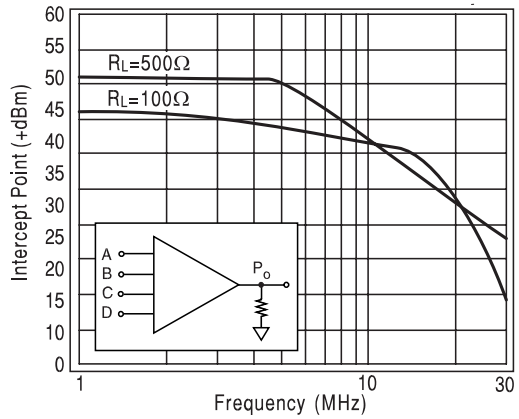
DS012722-25

Differential Gain (Negative Sync.)



DS012722-26

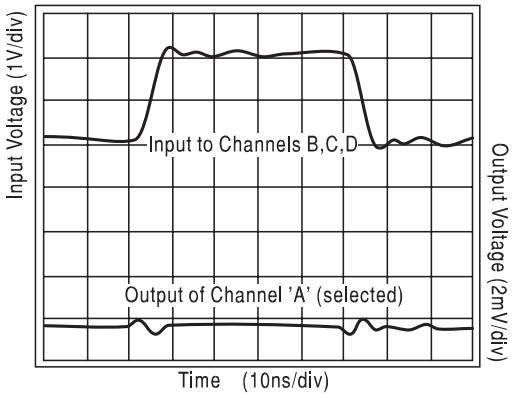
2- Tone, 3rd Order Intermodulation Intercept



DS012722-27

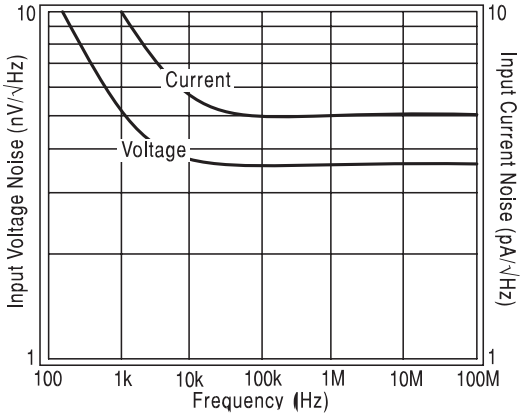
Typical Performance Characteristics (T_A = 25°C, $+V_{CC}$ = 5V, $-V_{EE}$ = −5.2V, R_L = 500Ω unless specified) (Continued)

Transient Isolation



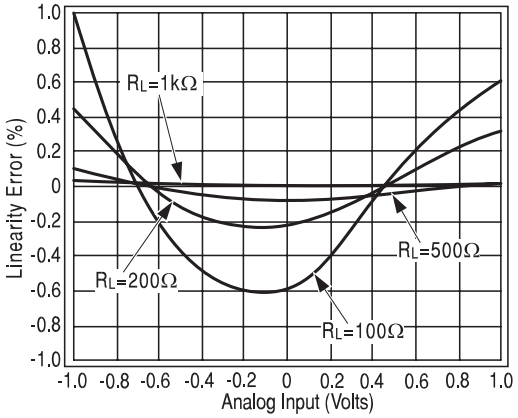
DS012722-28

Input Referred Noise



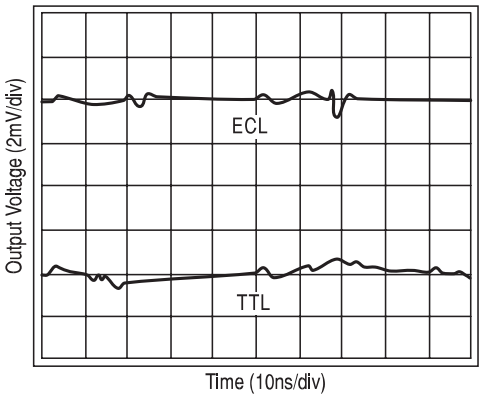
DS012722-29

Integral Linearity Error



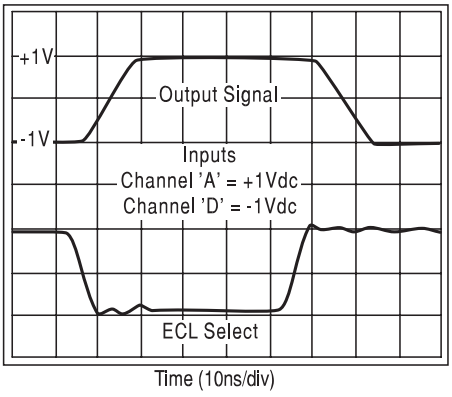
DS012722-30

Switching Transient (Grounded Inputs)



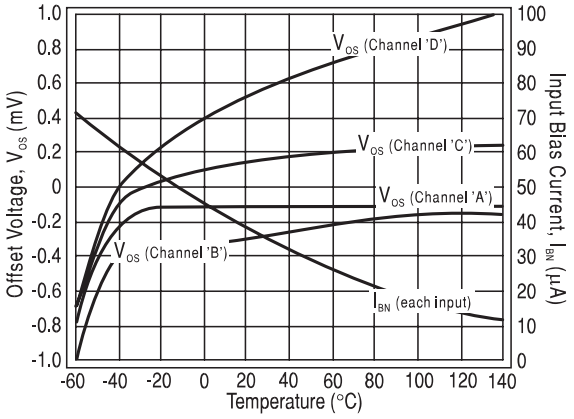
DS012722-31

Large-Signal Channel-to-Channel Switching



DS012722-32

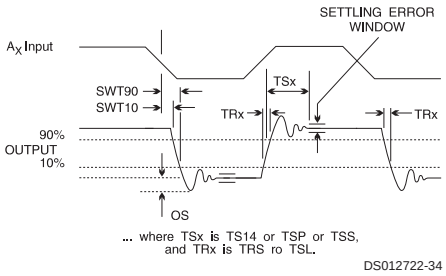
Typical DC Error vs. Temperature



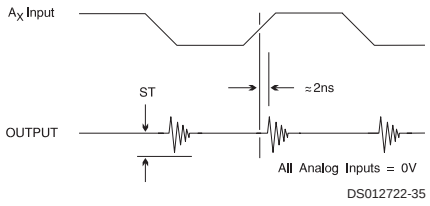
DS012722-33

Application Information

System Timing Diagram



Switching Transient Timing Diagram



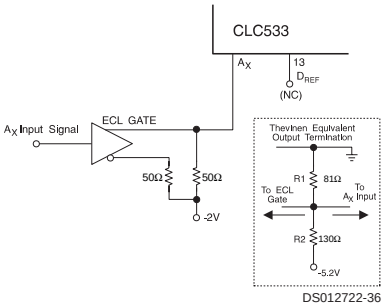


FIGURE 1. ECL Level Channel SELECT Configuration

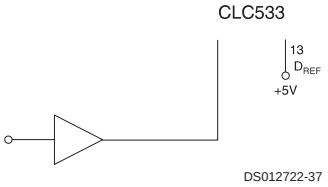


FIGURE 2. TTL/CMOS Level Channel SELECT Configuration

Description

The CLC533 is a 4:1 analog multiplexer designed with a closed loop architecture to provide very low harmonic distortion and superior channel-to-channel isolation. This low distortion, coupled with very fast switching speed makes the CLC533 an ideal multiplexer for data conversion applications. User selectable ECL or TTL select logic adds to the versatility of this device. External frequency response compensation allows the performance of the CLC533 to be optimized for each application

Digital Interface and Channel Select

The CLC533 has two channel select pins which can be used to select any one of the four inputs. These digital inputs can be configured to meet TTL, ECL or CMOS logic levels with the D_{REF} pin. If D_{REF} is left open, the A_0 and A_1 select inputs will respond to ECL 10K switching levels (*Figure 1*). For TTL or CMOS levels, D_{REF} should be tied to V_{CC} (*Figure 2*). There is an internal series resistor which makes it possible to connect D_{REF} directly to the power supply. Select pins according to the truth table shown on the front page. A more positive voltage is considered to be a logic '1'. Therefore with no connection to A_0 or A_1 the internal pullup resistors swill select the D input to be passed through to the output.

Compensation

The CLC533 is externally compensated, allowing the user to select the bandwidth that best suits the application. Decreasing bandwidth has two advantages: lower noise and lower switching transients. In a sampled system, noise at frequencies above ½ the sampling frequency will be aliased into the baseband and will corrupt the signal of interest. When the CLC533 is switched from one channel to another, the output slows rapidly until it arrives at the new signal. This high slew rate signal can capacitively couple into other nodes in the circuit and can have a detrimental effect on overall performance. Since error signal noise coupling through stray capacitance and inductances decreases with decreasing dV/dt, the slew rate should be minimized consistent with system throughput requirements.

Output Load

The final frequency response is a result of both the compensation capacitor and the load impedance that the CLC533 is driving. *Figure 3* below shows the effect that C_{COMP} has on bandwidth for a fixed load. Graphs on the preceding pages demonstrate the effect of C_{COMP} on pulse response and settling time, and the optimum value of C_{COMP} to maximize bandwidth for various amounts of resistive loading. Because there are so many factors that go into determining the optimum value of C_{COMP} it is recommended that once a value is selected, the application circuit be built up and larger and smaller compensation capacitors be tried to determine the best value for that particular circuit.

The output load that the CLC533 is driving has an effect on the harmonic distortion of the device as well as its frequency response. Distortion is minimized with a 500Ω load. When driving components with a high input impedance, addition of a load resistor can improve the performance. If the load is capacitive in nature, it should be isolated from the CLC533 output via a series resistor. The recommended series resistor R_S, for various capacitive loads C_L, can be found by referring to the "Recommended compensation Cap vs. Load" plot in the "Typical Performance" section.

Application Information (Continued)

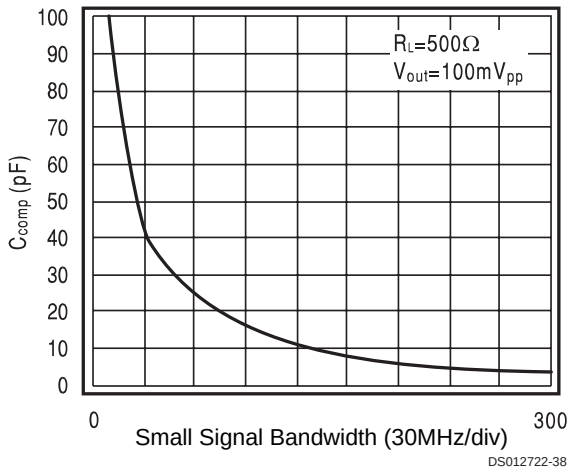


FIGURE 3. Small-Signal Bandwidth vs. C_{COMP}

Power Supplies and Grounding

In any circuit there are parasitic signal paths between components. Some of the most common of these are part of the power supply and grounding network.

To minimize DC impedance of the ground and power nets, use the heaviest possible traces and ground planes. To further reduce the supply impedance at higher frequencies, a 6 to 10µF capacitor should be placed between supply lines and ground. At very high frequencies, the inductance in the traces becomes significant and 0.01 to 0.1µF bypass capacitors need to be placed a very close to each power pin. To reduce the negative effects of ground impedances that will exist, consider the paths that ground currents must take to get from the various devices on the circuit card to the power supply. To achieve good system performance, it is vital that large currents and high speed time varying switching currents, be kept away the input signal terminal resistors. This can be achieved through layout of power and ground nets. Using a ground plane split between analog and digital sections of the circuits forces all of the ground current from the digital circuits to go directly to the power connector without straying to the analog side of the card.

Optimizing for Channel-to-Channel Isolation

Although the CLC533 has excellent channel-to-channel isolation, if there is crosstalk between the input signals before they reach the CLC533, the multiplexer will faithfully pass these corrupted signals through to its output and dutifully take the blame for poor isolation. The CLC533 evaluation board has successfully demonstrated in excess of 80dB of isolation and can be considered to be a model for the layout of boards requiring good isolation. The evaluation board has input signal traces shielded by guard rings as shown in *Figure 4*. These guard rings help to prevent ground return currents from other channels finding their way into the selected channel. If there are input termination resistors, care must be taken that the ground return currents between resistors cannot interfere with each other. Use of chip resistors allows for best isolation, and if the guard ring around the input trace is used for the termination resistor ground, then the ground currents for each input are forced to take paths away from one another.

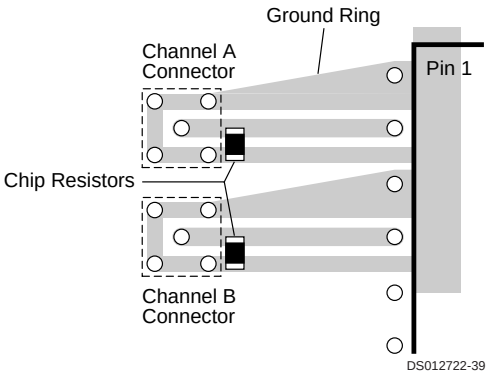


FIGURE 4. Analog Input Using Guard Ring

Uses of the CLC533 with an Analog-to-Digital Converter

To get the most out of the combination of multiplexer and ADC, a clear understanding of both converter operation and multiplexer operation is required. Careful attention to the timing of the convert signal to the ADC and the channel select signal to the CLC533 is one key to optimizing performance.

To obtain the best performance from the combination, the output of the CLC533 must be a valid representation of the selected input at the time that the ADC samples it. The time at which the ADC samples the input is determined by the type of ADC that is being used. Subranging ADCs usually have a Track-and-Hold (T/H) at the their input. For a successful combination of the multiplexer and the ADC, the multiplexer timing and the T/H timing must be compatible. When the ADC is given a convert command, the T/H transitions from Track mode to Hold mode. The delay between the convert command and the transition is usually specified as Aperture Delay or as Sampling Time Offset. To minimize the time that the multiplexer has to settle and the T/H has to acquire the signal, the multiplexer should begin its transition from one input to the other immediately after the T/H transition has taken place. However it is during this period of time that a subranging ADC is performing analog processing of the sampled signal, and high slew rate transitions on the input may feed through to the sample being converted. To minimize this interaction there are two strategies that can be taken: strategy one applies when the sample rate of the system is below the rated speed of the converter. Here the select timing is delayed so that the multiplexer transition takes place after the A/D has completed one conversion cycle and is waiting for the next converter command. As an example: a CLC935 (15Msps) A/D converter is being used at 10 MHz, the conversion takes place in the first 67ns after the convert command, the next 33ns are spent waiting for the next convert command and would be an ideal time to transition the multiplexer from one channel to the next. Strategy two involves lowering the analog input slew rate so that it has fewer high frequency components that might feedthrough to the hold capacitor while the converter's T/H is in Hold mode. This slew rate reduction can be done through the use of the external CLC533 compensation capacitors. Use of this method has the advantage of reducing the excess bandwidth that the CLC533 has compared to the ADC. This bandwidth limitation will reduce the amount of high frequency noise that is aliased back into the sampled band. *Figure 5* shows recommended C_{COMP} values that can be used as function of ADC Sample rate. Since the optimal values will change from one ADC to the next, this graph should be used as a starting point for C_{COMP} selection

Application Information (Continued)

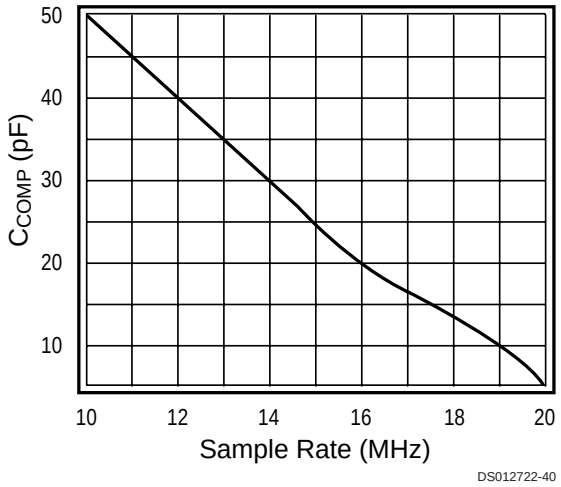


FIGURE 5.

Flash ADCs are similar to subranging ADCs in that the sampling period is very brief. The primary difference is that the acquisition time of a flash converter is much shorter than a subranging A/D. With a flash ADC the transition of the mix output should be after sampling window (Aperture delay after the converter command). The periods of time during which the internal circuitry in a flash converter is sensitive to external disruptions are relatively brief. It may be found that a slight delay between the ADC clock and the CLC533 select lines will have a positive effect on overall performance.

Mixed Mode Circuit Design

In any mixed mode circuit care must be taken to keep the high slew rate digital signals from interfering with the high precision analog signals. A successful design will take this into consideration from many angles and will account for it in digital timing, logic family selected, PCB layout, analog signal bandwidth and a myriad of other aspects. Below are a few tips that should be kept in mind when designing a circuit that involves both analog and digital circuitry.

Timing

If analog signals going through the CLC533 are to be sampled, minimize the amount of digital logic switching during the sampling period.

Logic Family Selection

When designing digital logic, there are often several logic families that will provide a solution to the problem at hand. Although they may perform equally in a digital sense, they may have varying degrees of influence on the analog circuits in the same system. Coupling of digital signals through stray capacitances is rarely a problem for the digital logic but can be detrimental to an otherwise good analog design. To minimize coupling, lay out the board to minimize the stray capacitances as much as possible: if an analog and a digital signal must cross, make them cross at right angles and avoid long parallel runs. If a 74LS00 will work in a socket, using a 74F00 will probably have no effect on the digital circuitry, but the faster edges will find it easier to corrupt analog signals. When faced with a choice between several logic families, select the slowest one possible to get the job done. Don't forget that the slew rates of digital logic depend not only on the rise and fall times, but on the output swing as well. ECL gates with a 1ns rise time have much slower rates than TTL gates with the same rise times. Do not attempt to slow logic edge rates through the addition of capacitance on the logic lines.

The negative effect that digital logic has on power supplies is not constant through different logic families. CMOS logic draws current only during transitions. The surge currents that it draws at these times can be quite significant and can be very disruptive to the power and ground networks. ECL tends to draw constant amounts of current and has a much smaller effect on the supply lines.

Gain Selection for an ADC

In many applications, such as RADAR, the dynamic range requirements are more important than the accuracy requirements. Since wide dynamic range ADCs are also typically high accuracy ADCs this often leads the designer into an ADC which is a technical overkill and a budget buster. By using the CLC533 as a selectable gain stage, a less expensive A/D can be used. For example, if an application calls for 85dB of dynamic range and 0.05% accuracy, rather than using a 16 bit converter, use a 12 bit converter with the circuit shown below. In this circuit the CLC533 is used to select between the input signal and versions of the input signal attenuated by 6, 12 and 18dB. This circuit affords better than 14 bit dynamic range, 12 bit accuracy and a 12 bit price. By using resistors of the same value, a single resistor network can be used, assuring good matching of the resistors,over temperature.

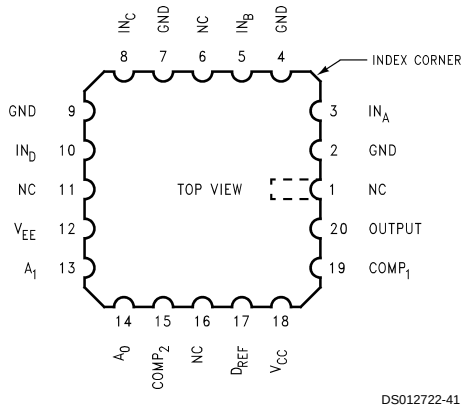
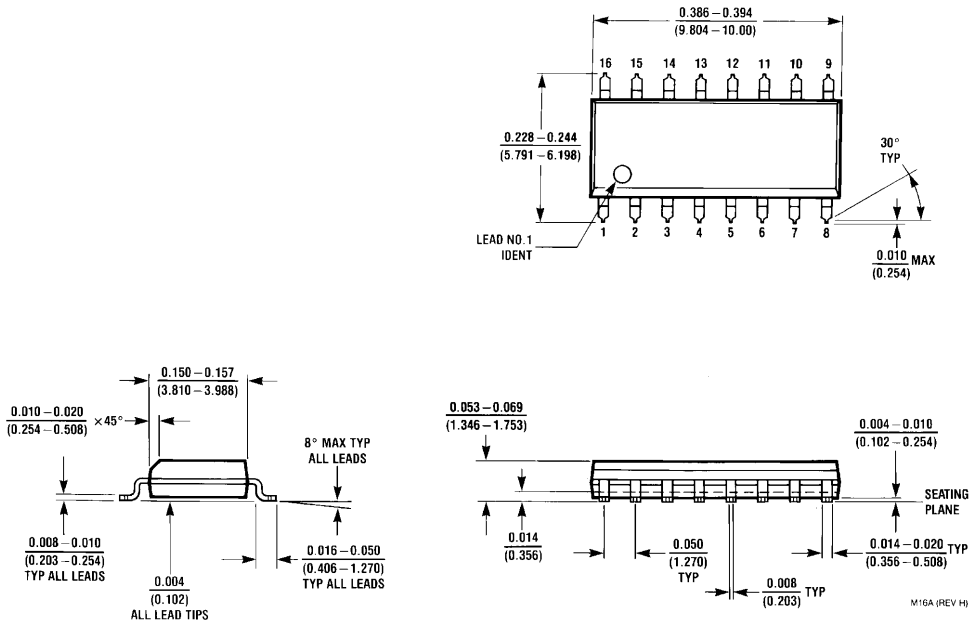


FIGURE 6.

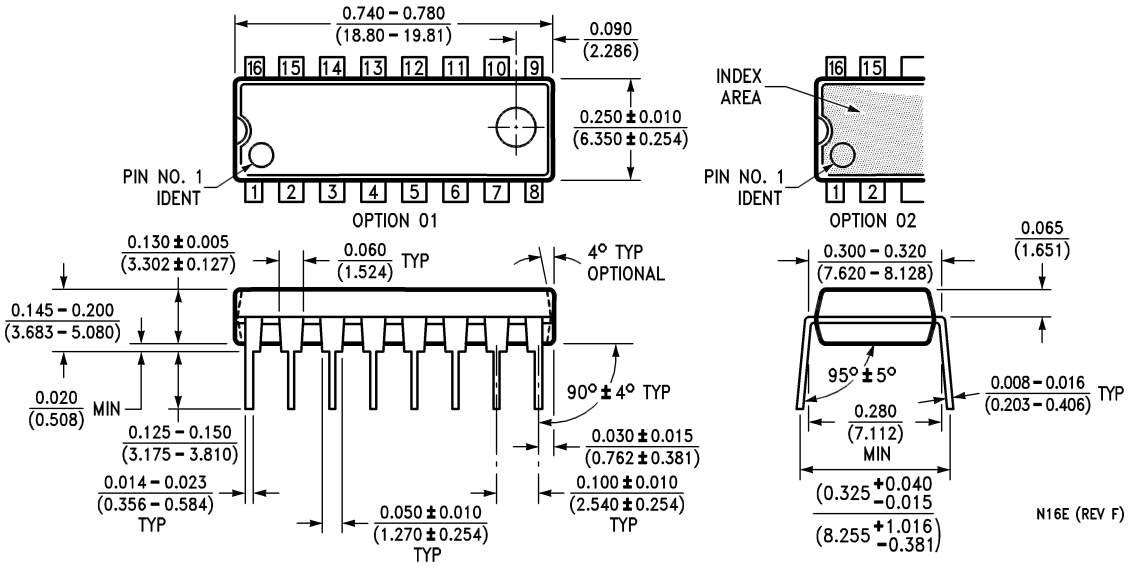
Evaluation Board

Evaluation boards are available for both the DIP version (Part number CLC730035) and SOIC version (Part number CLC730039) of the CLC533. These boards can be used for fast, trouble free evaluation and characterization of the CLC533. Additionally this board serves an example of a successful PCB layout that can be copied into application-layouts.

Physical Dimensions inches (millimeters) unless otherwise noted



NS Package Number M16A



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