# CLC418

***CLC418 Dual High-Speed, Low-Power Line Driver***


Literature Number: SNOS836

National Semiconductor

# Comlinear CLC418
# Dual High-Speed, Low-Power Line Driver

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Dual High-Speed, Low-Power Line Driver

## General Description

The Comlinear CLC418 dual high-speed current-feedback operational amplifier is designed to drive low-impedance and high capacitance loads while maintaining high signal fidelity. Operating on ±5V power supplies, each of the CLC418's amplifiers produces a continuous 96mA output current. Into a back-terminated 50Ω load, the devices produce -85/-64dBc second/third harmonic distortion ($A_V$ = +2, $V_O$ = $2V_{pp}$, f = 1MHz).

The CLC418's current-feedback architecture maintains consistent performance over a wide range of gain and signal levels. DC gain and bandwidth can be set independently. With proper resistor selection, either maximally flat gain response or linear phase response can be selected.

Requiring a mere 15mW quiescent power per amplifier, the CLC418 offers superior performance-vs-power with a 130MHz small-signal bandwidth, 350V/ms slew rate and quick 4.6ns rise/fall times (2Vstep). The combination of low quiescent power, high output current drive and high performance make the CLC418 a great choice for many battery-powered personal communication/computing systems.

Combining the CLC418's two amplifiers (shown below) results in a powerful differential line driver for driving video signals over unshielded twisted-pair (UTP). The CLC418 can also be used for driving differential-input step-up transformers for applications such as Asynchronous Digital Subscriber Lines (ADSL) or High-Bit-Rate Digital Subscriber Lines (HDSL).

The CLC418's amplifiers make excellent low-power high-resolution A-to-D converter drivers with their very fast 15ns settling time (to 0.2%) and ultra-low -85/-75dBc harmonic distortion ($A_V$ = +2, $V_O$ = $2V_{pp}$, f = 1MHz, $R_L$ = 1kΩ).

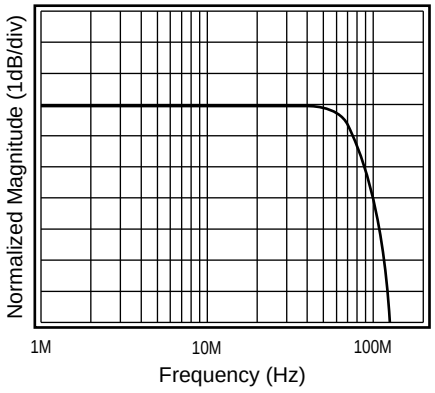
## Features

- 130MHz bandwidth ($A_V$ = +2)
- 96mA output current
- 1.5mA supply current
- -85/-75dBc HD2/HD3
- 15ns settling to 0.2%
- -74dBc input-referred crosstalk (5MHz)
- Single version available (CLC408)

## Applications

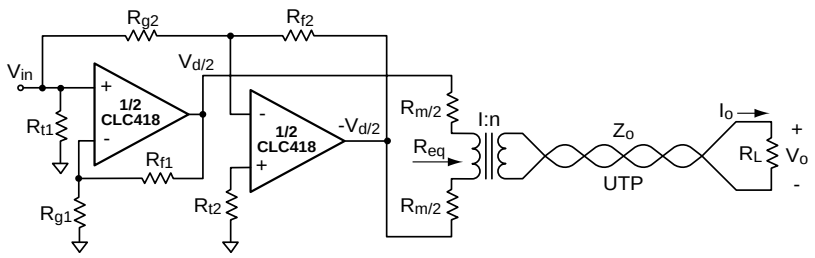
- ADSL/HDSL driver
- Coaxial cable driver
- UTP differential line driver
- Transformer/coil driver
- High capacitive-load driver
- Video line driver
- Portable/battery-powered line driver
- Differential A/D driver

**Non-Inverting Frequency Response**
**($A_V$ = +2V/V, $R_L$ = 100Ω)**




## Typical Application Diagram

**Differential Line Driver**
**with Load Impedance Conversion**




## Pinout

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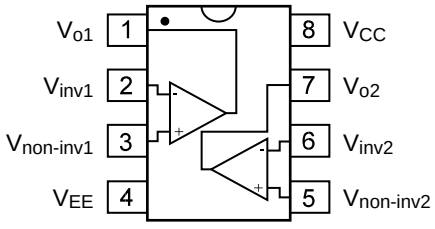


## CLC418 Electrical Characteristics ($A_V$ = +2, $R_f$ = 1kΩ, $V_{cc}$ = ± 5V, $R_L$ = 100Ω, T = 25°C; unless specified)

| PARAMETERS | CONDITIONS | TYP | MIN/MAX RATINGS | | | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Ambient Temperature | CLC418AJ | +25°C | +25°C | 0 to 70°C | -40 to 85°C | | |
| **FREQUENCY DOMAIN RESPONSE** | | | | | | | |
| -3dB bandwidth | $V_o$ < 1.0$V_{pp}$ | 130 | 80 | 80 | 75 | MHz | B |
| | $V_o$ < 4.0$V_{pp}$ | 45 | 33 | 29 | 28 | MHz | |
| -0.1dB bandwidth | $V_o$ < 1.0$V_{pp}$ | 30 | 25 | 20 | 20 | MHz | |
| gain flatness | $V_o$ < 1.0$V_{pp}$ | | | | | | |
| peaking | DC to 200MHz | 0 | 0.5 | 0.9 | 1.0 | dB | B |
| rolloff | <30MHz | 0.2 | 0.45 | 0.6 | 0.6 | dB | B |
| linear phase deviation | <30MHz | 0.2 | 0.4 | 0.5 | 0.5 | deg | |
| differential gain | NTSC, $R_L$=150Ω | 0.1 | – | – | – | % | |
| differential phase | NTSC, $R_L$=150Ω | 0.4 | – | – | – | deg | |
| **TIME DOMAIN RESPONSE** | | | | | | | |
| rise and fall time | 2V step | 4.6 | 7.0 | 7.5 | 8.0 | ns | |
| settling time to 0.2% | 2V step | 15 | 30 | 38 | 40 | ns | |
| overshoot | 2V step | 5 | 12 | 12 | 12 | % | |
| slew rate $A_V$ = +2 | 2V step | 350 | 260 | 225 | 215 | V/µs | |
| **DISTORTION AND NOISE RESPONSE** | | | | | | | |
| 2nd harmonic distortion | 2$V_{pp}$, 1MHz | -85 | – | – | – | dBc | |
| | 2$V_{pp}$, 1MHz; $R_L$ = 1kΩ | -85 | – | – | – | dBc | |
| | 2$V_{pp}$, 5MHz | -65 | -60 | -58 | -58 | dBc | B |
| 3rd harmonic distortion | 2$V_{pp}$, 1MHz | -64 | – | – | – | dBc | |
| | 2$V_{pp}$, 1MHz; $R_L$ = 1kΩ | -75 | – | – | – | dBc | |
| | 2$V_{pp}$, 5MHz | -50 | -45 | -44 | -44 | dBc | B |
| crosstalk (input-referred) | 2$V_{pp}$, 5MHz | -74 | -68 | -68 | -68 | dBc | |
| equivalent input noise | | | | | | | |
| voltage ($e_{ni}$) | >1MHz | 5 | 6.3 | 6.6 | 6.7 | nV/√Hz | |
| non-inverting current ($i_{bn}$) | >1MHz | 1.4 | 1.8 | 1.9 | 2.3 | pA/√Hz | |
| inverting current ($i_{bi}$) | >1MHz | 13 | 16 | 17 | 18 | pA/√Hz | |
| **STATIC DC PERFORMANCE** | | | | | | | |
| input offset voltage | | 2 | 8 | 11 | 11 | mV | A |
| average drift | | 25 | – | 35 | 40 | µV/°C | |
| input bias current (non-inverting) | | 2 | 8 | 11 | 15 | µA | A |
| average drift | | 60 | – | 80 | 110 | nA/°C | |
| input bias current (inverting) | | 2 | 10 | 18 | 20 | µA | A |
| average drift | | 20 | – | 90 | 110 | nA/°C | |
| power supply rejection ratio | DC | 55 | 50 | 48 | 48 | dB | B |
| common-mode rejection ratio | DC | 52 | 48 | 46 | 46 | dB | |
| supply current | $R_L$= ∞, 2 channels | 3.0 | 3.4 | 3.6 | 3.6 | mA | A |
| **MISCELLANEOUS PERFORMANCE** | | | | | | | |
| input resistance (non-inverting) | | 5 | 3 | 2.5 | 1 | MΩ | |
| input capacitance (non-inverting) | | 1 | 2 | 2 | 2 | pF | |
| common mode input range | | ±2.7 | ±2.3 | ±2.2 | ±2.0 | V | |
| output voltage range | $R_L$ = 100Ω | ±3.3 | ±2.9 | ±2.8 | ±2.6 | V | |
| output voltage range | $R_L$ = ∞ | ±4.0 | ±3.8 | ±3.7 | ±3.5 | V | |
| output current | | 96 | 96 | 96 | 60 | mA | C |
| output resistance, closed loop | DC | 0.03 | 0.15 | 0.2 | 0.3 | Ω | |

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

## Absolute Maximum Ratings

| | |
|---|---|
| supply voltage | ±7V |
| output current (see note C) | 96mA |
| common-mode input voltage | ±$V_{CC}$ |
| maximum junction temperature | +175°C |
| storage temperature range | -65°C to +150°C |
| lead temperature (soldering 10 sec) | +300°C |
| ESD rating (human body model) | 4000V |

## Notes

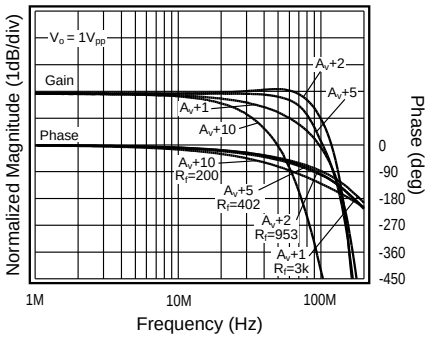
A) J-level: spec is 100% tested at +25°C, sample tested at +85°C. L-level: spec is 100% wafer probed at +25°C.

B) J-level: spec is sample tested at +25°C.

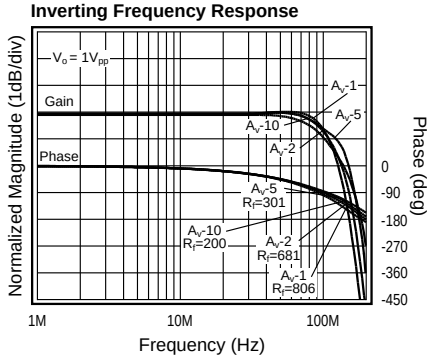
C) The output current sourced or sunk by the CLC418 can exceed the maximum safe output current limit.

# Typical Performance Characteristics ($A_V$ = +2, $R_f$ = 1kΩ, $R_L$ = 100Ω, $V_{CC}$ = + 5V, T = 25°C; CLC418AJ; unless specified)

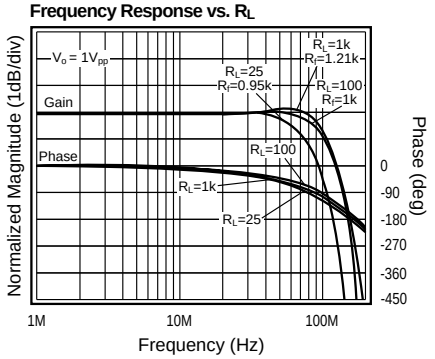
**Non-Inverting Frequency Response**



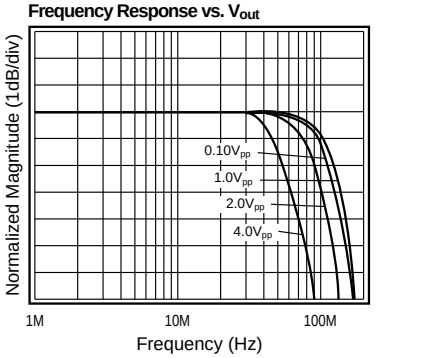

**Inverting Frequency Response**



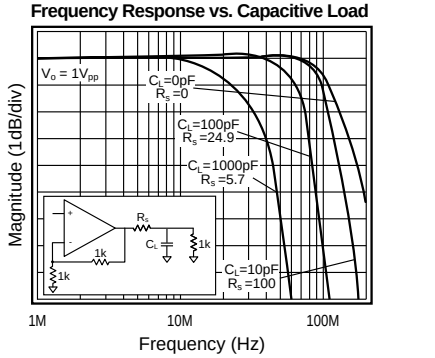

**Frequency Response vs. $R_L$**



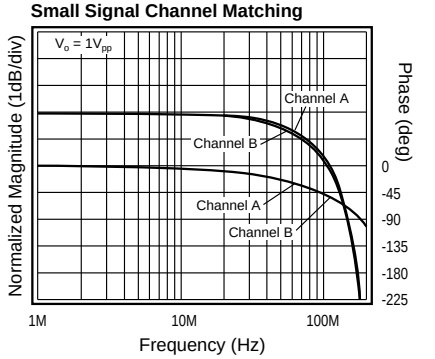

**Frequency Response vs. $V_{out}$**



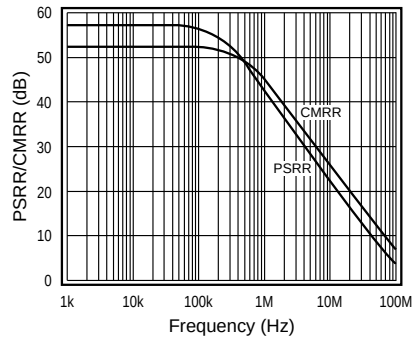

**Frequency Response vs. Capacitive Load**



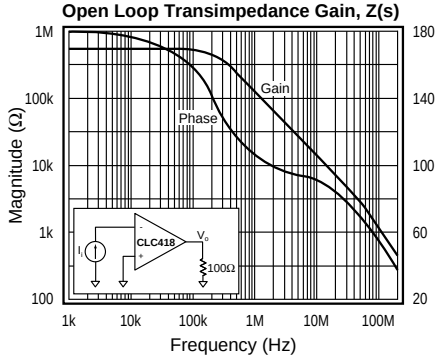

**Small Signal Channel Matching**



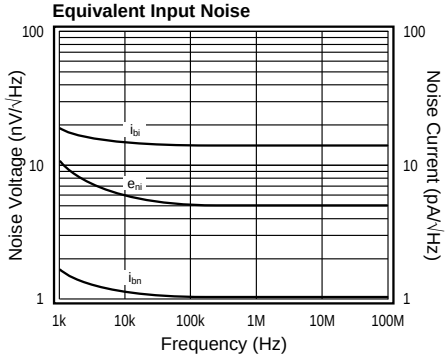

**PSRR and CMRR**



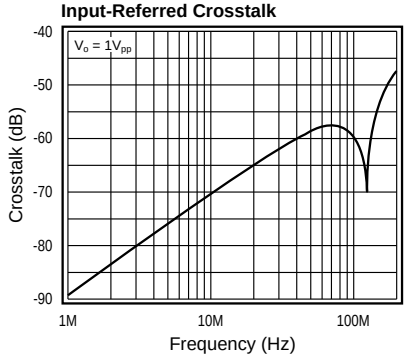

**Open Loop Transimpedance Gain, Z(s)**



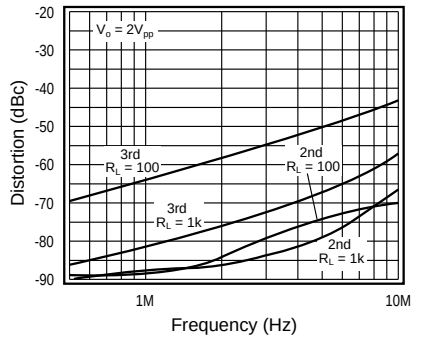

**Equivalent Input Noise**



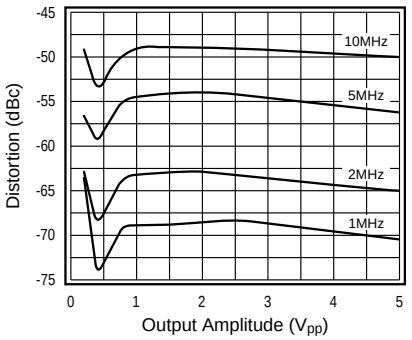

**Input-Referred Crosstalk**



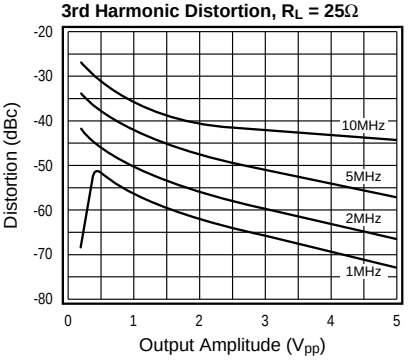

**2nd & 3rd Harmonic Distortion**



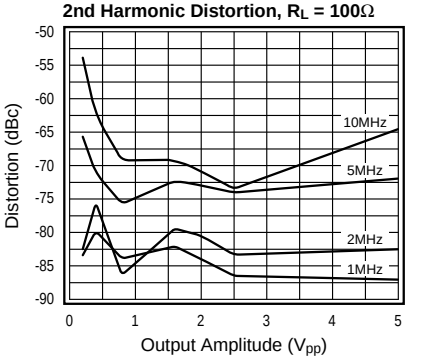

**2nd Harmonic Distortion, $R_L$ = 25Ω**



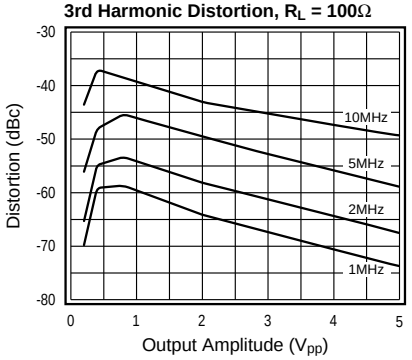

**3rd Harmonic Distortion, $R_L$ = 25Ω**




**2nd Harmonic Distortion, $R_L$ = 100Ω**

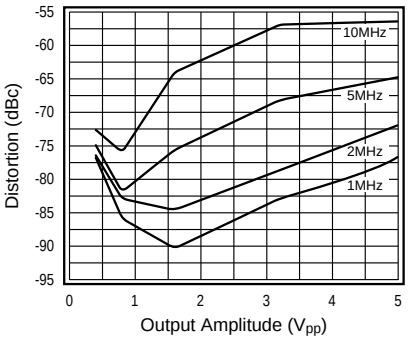



**3rd Harmonic Distortion, $R_L$ = 100Ω**

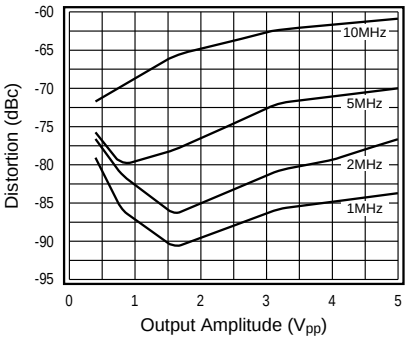


# Typical Performance Characteristics ($A_v$ = +2, $R_f$ = 1kΩ, $R_L$ = 100Ω, $V_{CC}$ = + 5V, T = 25°C; CLC418AJ; unless specified)

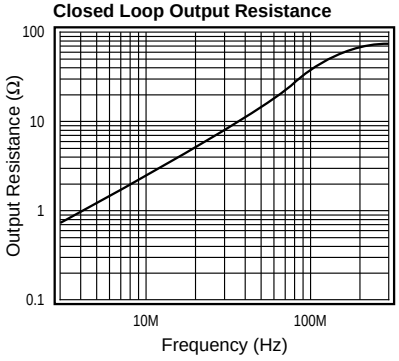
**3rd Harmonic Distortion, $R_L$ = 1kΩ**



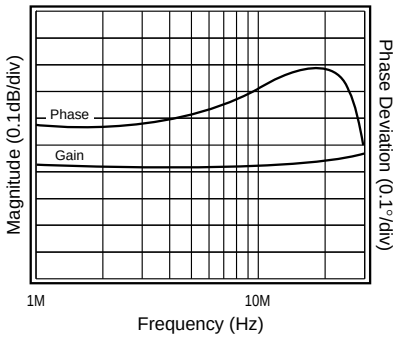

**2nd Harmonic Distortion, $R_L$ = 1kΩ**



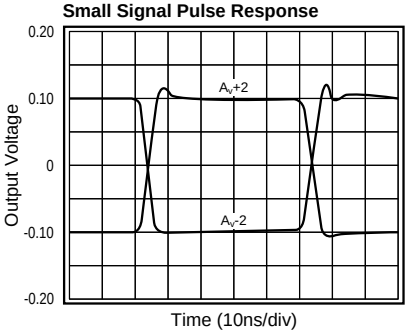

**Closed Loop Output Resistance**



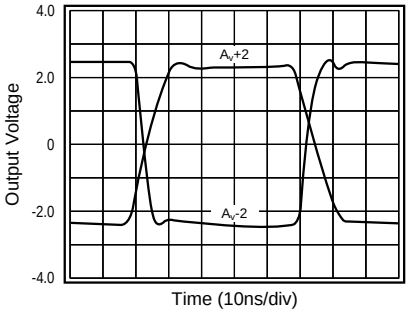

**Gain Flatness & Linear Phase Deviation**



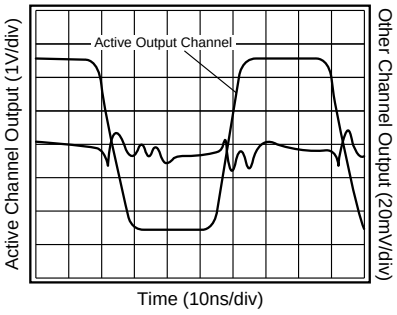

**Small Signal Pulse Response**



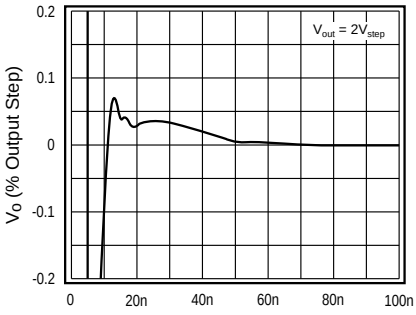

**Large Signal Pulse Response**



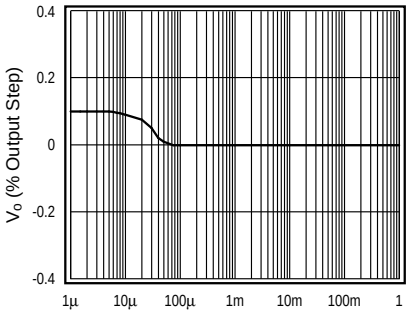

**Pulse Crosstalk**



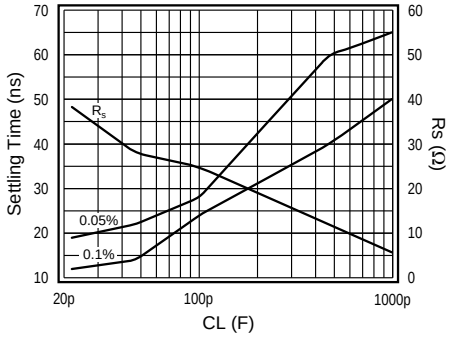

**Short Term Settling Time**



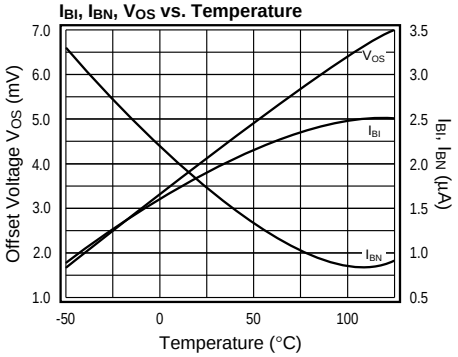

**Long Term Settling Time**




**Settling Time vs. Capacitive Load**




**$I_{BI}$, $I_{BN}$, $V_{OS}$ vs. Temperature**



# CLC418 OPERATION

The CLC418 has a current-feedback (CFB) architecture built in an advanced complementary bipolar process. The key features of current-feedback are:

- AC bandwidth is independent of voltage gain
- Inherently unity-gain stability
- Frequency response may be adjusted with feedback resistor ($R_f$ in Figures 1-3)
- High slew rate
- Low variation in performance for a wide range of gains, signal levels and loads
- Fast settling

Current-feedback operation can be explained with a simple model. The voltage gain for the circuits in Figures 1 and 2 is approximately:

$$\frac{V_o}{V_{in}} = \frac{A_v}{1+\frac{R_f}{Z(j\omega)}}$$

where:

- $A_v$ is the DC voltage gain
- $R_f$ is the feedback resistor
- $Z(j\omega)$ is the CLC418's open-loop transimpedance gain
- $\frac{Z(j\omega)}{R_f}$ is the loop gain

The denominator of the equation above is approximately 1 at low frequencies. Near the -3dB corner frequency, the interaction between $R_f$ and $Z(j\omega)$ dominates the circuit performance. Increasing $R_f$ does the following:

- Decreases loop gain
- Decreases bandwidth
- Reduces gain peaking
- Lowers pulse response overshoot
- Affects frequency response phase linearity

# CLC418 DESIGN INFORMATION

Standard op amp circuits work with CFB op amps. There are 3 unique design considerations for CFB:

- The feedback resistor ($R_f$ in Figures 1-3) sets AC performance
- $R_f$ cannot be replaced with a short or a capacitor
- The output offset voltage is not reduced by balancing input resistances

The following sub-sections cover:

- Design parameters, formulas and techniques
- Interfaces
- Application circuits
- Layout techniques
- SPICE model information

**DC Gain (non-inverting)**

The non-inverting DC voltage gain for the configuration shown in Figure 1 is: $A_v = 1+\frac{R_f}{R_g}$

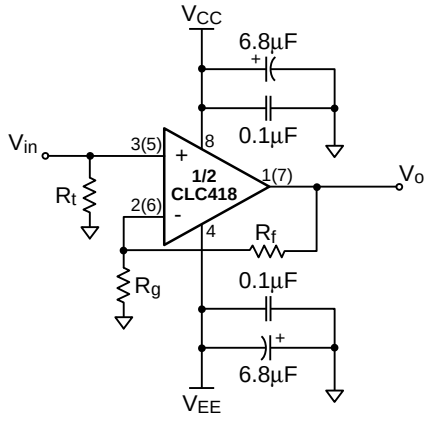



**Figure 1: Non-Inverting Gain**

The normalized gain plots in the ***Typical Performance Characteristics*** section show different feedback resistors ($R_f$) for different gains. These values of $R_f$ are recommended for obtaining the highest bandwidth with minimal peaking. The resistor $R_t$ provides DC bias for the non-inverting input.

For $A_v$ < 6, use linear interpolation on the nearest $A_v$ values to calculate the recommended value of $R_f$. For $A_v \geq 6$, the minimum recommended $R_f$ is 200Ω.

Select $R_g$ to set the DC gain: $R_g = \frac{R_f}{A_v - 1}$

DC gain accuracy is usually limited by the tolerance of $R_f$ and $R_g$.

**DC Gain (unity gain buffer)**

The recommended $R_f$ for unity gain buffers is 3kΩ. $R_g$ is left open. Parasitic capacitance at the inverting node may require a slight increase of $R_f$ to maintain a flat frequency response.

**DC Gain (inverting)**

The inverting DC voltage gain for the configuration shown in Figure 2 is: $A_v = -\frac{R_f}{R_g}$

The normalized gain plots in the ***Typical Performance Characteristics*** section show different feedback resistors ($R_f$) for different gains. These values of $R_f$ are recommended for obtaining the highest bandwidth with minimal peaking. The resistor $R_t$ provides DC bias for the non-inverting input.

For $|A_v| < 6$, use linear interpolation on the nearest $A_v$ values to calculate the recommended value of $R_f$. For $|A_v| \geq 6$, the minimum recommended $R_f$ is 200Ω.

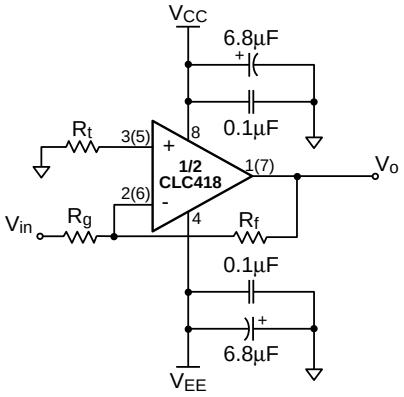



**Figure 2: Inverting Gain**

Select $R_g$ to set the DC gain: $R_g = \frac{R_f}{|A_v|}$. At large gains, $R_g$ becomes small and will load the previous stage. This can be solved by driving $R_g$ with a low impedance buffer like the CLC111, or increasing $R_f$ and $R_g$. See the ***AC Design (small signal bandwidth)*** sub-section for the tradeoffs.

DC gain accuracy is usually limited by the tolerance of $R_f$ and $R_g$.

**DC Gain (transimpedance)**

Figure 3 shows a transimpedance circuit where the current $I_{in}$ is injected at the inverting node. The current source's output resistance is much greater than $R_f$.

The DC transimpedance gain is: $A_R = \frac{V_o}{I_{in}} = -R_f$

The recommended $R_f$ is 3kΩ. Parasitic capacitance at the inverting node may require a slight increase of $R_f$ to maintain a flat frequency response.

DC gain accuracy is usually limited by the tolerance of $R_f$.

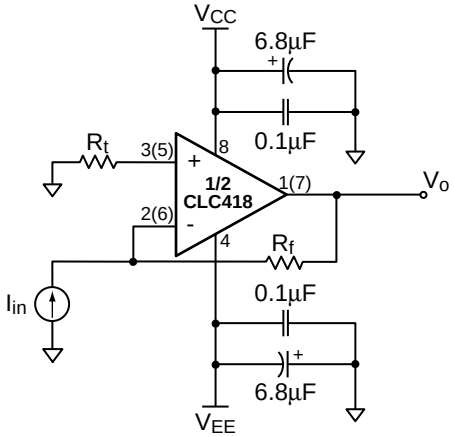



**Figure 3: Transimpedance Gain**

**DC Design (level shifting)**

Figure 4 shows a DC level shifting circuit for inverting gain configurations. $V_{ref}$ produces a DC output level shift of $-V_{ref} \cdot \frac{R_f}{R_{ref}}$, which is independent of the DC output produced by $V_{in}$.

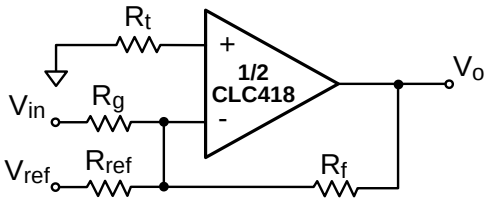



**Figure 4: Level Shifting Circuit**

**DC Design (DC offsets)**

The DC offset model shown in Fig. 5 is used to calculate the output offset voltage. The equation for output offset voltage is:

$$V_o = -\left(V_{os} + I_{BN} \cdot R_{eq1}\right) \cdot \left(1 + \frac{R_f}{R_{eq2}}\right) + \left(I_{BI} \cdot R_f\right)$$

The current offset terms, $I_{BN}$ and $I_{BI}$, ***do not track each other***. The specifications are stated in terms of magnitude only. Therefore, the terms $V_{os}$, $I_{BN}$, and $I_{BI}$ can have either polarity. Matching the equivalent resistance seen at both input pins does not reduce the output offset voltage.

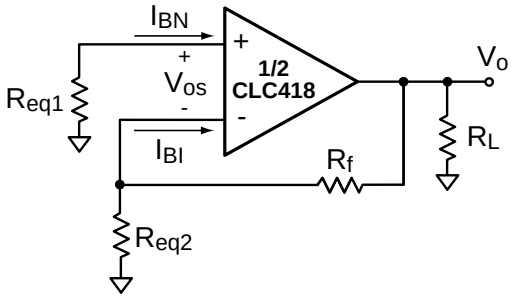



**Figure 5: DC Offset Model**

**DC Design (output loading)**

$R_L$, $R_f$, and $R_g$ load the op amp output. The equivalent load seen by the output in Figure 5 is:

$$R_{L(eq)} = \begin{cases} R_L \parallel (R_f + R_{eq2}), \text{ non-inverting gain} \\ R_L \parallel R_f, \text{ inverting and transimpedance gain} \end{cases}$$

The equivalent output load ($R_{L(eq)}$) needs to be large enough so that the output current can produce the required output voltage swing.

**AC Design (small signal bandwidth)**

The CLC418 current-feedback amplifier bandwidth is a function of the feedback resistor ($R_f$), not of the DC voltage gain ($A_V$). The bandwidth is approximately proportional to $\frac{1}{R_f}$. As a rule, if $R_f$ doubles, the bandwidth is cut in half.

Other AC specifications will also be degraded. Decreasing $R_f$ from the recommended value increases peaking, and ***for very small values of $R_f$ oscillation will occur.***

**AC Design (minimum slew rate)**

Slew rate influences the bandwidth of large signal sinusoids. To determine an approximate value of slew rate necessary to support a large sinusoid, use the

following equation:

$$SR > 5 \cdot f \cdot V_{peak}$$

where $V_{peak}$ is the peak output sinusoidal voltage.

The slew rate of the CLC418 in inverting gains is always higher than in non-inverting gains.

**AC Design (linear phase/constant group delay)**
The recommended value of $R_f$ produces minimal peaking and a reasonably linear phase response. To improve phase linearity when $|A_v| < 6$, increase $R_f$ approximately 50% over its recommended value. Some adjustment of $R_f$ may be needed to achieve phase linearity for your application. See the ***AC Design (small signal bandwidth)*** sub-section for other effects of changing $R_f$.

Propagation delay is approximately equal to group delay. Group delay is related to phase by this equation:

$$\tau_{gd}(f) = -\frac{1}{360^\circ} \cdot \frac{d\phi(f)}{df} \approx -\frac{1}{360^\circ} \cdot \frac{\Delta\phi(f)}{\Delta f}$$

where $\phi(f)$ is the phase in degrees. Linear phase implies constant group delay. The technique for achieving linear phase also produces a constant group delay.

**AC Design (peaking)**
Peaking is sometimes observed with the recommended $R_f$. If a small increase in $R_f$ does not solve the problem, then investigate the possible causes and remedies listed below:

- Capacitance across $R_f$
  - ***Do not place a capacitor across*** $R_f$
  - Use a resistor with low parasitic capacitance for $R_f$
- A capacitive load
  - Use a series resistor between the output and a capacitive load (see the ***Settling Time versus $C_L$*** plot)
- Long traces and/or lead lengths between $R_f$ and the CLC418
  - Keep these traces as short as possible

For non-inverting and transimpedance gain configurations:

- Extra capacitance between the inverting pin and ground ($C_g$)
  - See the ***Printed Circuit Board Layout*** sub-section below for suggestions on reducing $C_g$
  - Increase $R_f$ if peaking is still observed after reducing $C_g$

For inverting gain configurations:

- Inadequate ground plane at the non-inverting pin and/or long traces between non-inverting pin and ground
  - Place a 50 to 200Ω resistor between the non-inverting pin and ground (see $R_t$ in Figure 2)

**AC Design (crosstalk)**
Crosstalk performance depends on the layout. Three layout techniques that can reduce crosstalk are:

- Provide short symmetrical ground return paths for:
  - the inputs
  - the supply bypass capacitors
  - the load
- Provide a short, grounded guard trace that:
  - goes underneath the package
  - is 0.1" (3mm) from the package pins
  - is on top and bottom of the printed circuit board with connecting vias
- Try different bypass capacitors to reduce high frequency crosstalk

The CLC418's evaluation board was used to produce the ***Input-Referred Crosstalk*** plot.

**Capacitive Loads**
Capacitive loads, such as found in A/D converters, require a series resistor ($R_s$) in the output to improve settling performance. The ***Settling Time vs. Capacitive Load*** plot in the ***Typical Performance Characteristics*** section provides the information for selecting this resistor.

Using a resistor in series with a reactive load will also reduce the load's effect on amplifier loop dynamics. For instance, driving coaxial cables without an output series resistor may cause peaking or oscillation.

**Transmission Line Matching**
One method for matching the characteristic impedance of a transmission line is to place the appropriate resistor at the input or output of the amplifier. Figure 6 shows the typical circuit configurations for matching transmission lines.

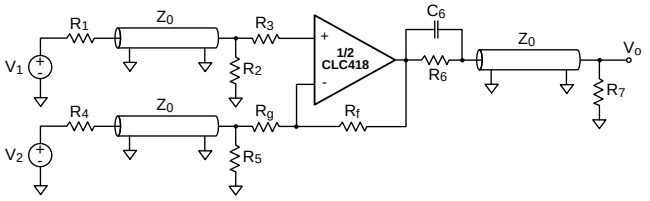



**Figure 6: Transmission Line Matching**

In non-inverting gain applications, $R_g$ is connected directly to ground. The resistors $R_1$, $R_2$, $R_6$, and $R_7$ are equal to the characteristic impedance, $Z_o$, of the transmission line or cable. Use $R_3$ to isolate the amplifier from reactive loading caused by the transmission line, or by parasitics.

In inverting gain applications, $R_3$ is connected directly to ground. The resistors $R_4$, $R_6$, and $R_7$ are equal to $Z_o$. The parallel combination of $R_5$ and $R_g$ is also equal to $Z_o$.

The input and output matching resistors attenuate the signal by a factor of 2, therefore additional gain is needed. Use $C_6$ to match the output transmission line over a greater frequency range. It compensates for the increase of the op amps output impedance with frequency.

**Thermal Design**
To calculate the power dissipation for the CLC418, follow these steps for each individual amplifier:

1) Calculate the no-load op amp power:
   $P_{amp} = I_{CC} \cdot (V_{CC} - V_{EE})$
2) Calculate the output stage's RMS power:
   $P_o = (V_{CC} - V_{load}) \cdot I_{load}$ , where $V_{load}$ and $I_{load}$ are the RMS voltage and current across the external load
3) Calculate the total op amp RMS power:
   $P_t = P_{amp} + P_o$

Now calculate the total power dissipated in the package:

4) Sum $P_t$ for both op amps to obtain $P_{tot}$

To calculate the maximum allowable ambient temperature, solve the following equation: $T_{amb} = 175 - P_{tot} \cdot \theta_{JA}$, where $\theta_{JA}$ is the thermal resistance from junction to ambient in °C/W, and $T_{amb}$ is in °C. The ***Package Thermal Resistance*** section contains the thermal resistance for various packages.

**Dynamic Range (input /output protection)**
ESD diodes are present on all connected pins for protection from static voltage damage. For a signal that may exceed the supply voltages, we recommend using diode clamps at the amplifier's input to limit the signals to less than the supply voltages.

The CLC418's output current can exceed the maximum safe output current. To limit the output current to < 96mA:

- Limit the output voltage swing with diode clamps at the input
- Make sure that $\left| R_L \right| \geq \frac{V_{o(max)}}{I_{o(max)}}$

$V_{o(max)}$ is the output voltage swing limit, and $I_{o(max)}$ is the maximum safe output current.

**Dynamic Range (input /output levels)**
The ***Electrical Characteristics*** section specifies the Common-Mode Input Range and Output Voltage Range; these voltage ranges scale with the supplies. Output Current is also specified in the ***Electrical Characteristics*** section.

Unity gain applications are limited by the Common-Mode Input Range. At greater non-inverting gains, the Output Voltage Range becomes the limiting factor. Inverting gain applications are limited by the Output Voltage Range (and by the previous amplifier's ability to drive $R_g$). For transimpedance gain applications, the sum of the input currents injected at the inverting input pin of the op amp needs to be: $\left| I_{in} \right| \leq \frac{V_{max}}{R_f}$ , where $V_{max}$ is the Output Voltage Range (see the ***DC Gain (transimpedance)*** sub-section for details).

The equivalent output load needs to be large enough so that the minimum output current can produce the required output voltage swing. See the ***DC Design (output loading)*** sub-section for details.

**Dynamic Range (noise)**
The output noise defines the lower end of the CLC418's useful dynamic range. Reduce the value of resistors in the circuit to reduce noise.

See the App Note ***Noise Design of CFB Op Amp Circuits*** for more details. Our SPICE models support noise simulations.

**Dynamic Range (distortion)**
The distortion plots in the ***Typical Performance Characteristics*** section show distortion as a function of load resistance, frequency, and output amplitude. Distortion places an upper limit on the CLC418's dynamic range.

The CLC418's output stage combines a voltage buffer with a complementary common emitter current source. The interaction between the buffer and the current source produces a small amount of crossover distortion. This distortion mechanism dominates at low output swing and low resistance loads. To avoid this type of distortion, use the CLC418 at high output swing.

Realized output distortion is highly dependent upon the external circuit. Some of the common external circuit choices that can improve distortion are:

- Short and equal return paths from the load to the supplies
- De-coupling capacitors of the correct value
- Higher load resistance

**Printed Circuit Board Layout**
High frequency op amp performance is strongly dependent on proper layout, proper resistive termination and adequate power supply decoupling. The most important layout points to follow are:

- Use a ground plane
- Bypass power supply pins with:
  - monolithic capacitors of about 0.1µF place less than 0.1" (3mm) from the pin
  - tantalum capacitors of about 6.8µF for large signal current swings or improved power supply noise rejection; we recommend a minimum of 2.2µF for any circuit
- Minimize trace and lead lengths for components between the inverting and output pins
- Remove ground plane 0.1" (3mm) from all input/output pads
- For prototyping, use flush-mount printed circuit board pins; ***never use high profile DIP sockets***.

**Evaluation Board**
Separate evaluation boards are available for proto-typing and measurements. Additional information is available in the evaluation board literature.

**SPICE Models**

SPICE models provide a means to evaluate op amp designs. Free SPICE models are available that:

- Support Berkeley SPICE 2G and its many derivatives
- Reproduce typical DC, AC, Transient, and Noise performance
- Support room temperature simulations

The ***readme*** file that accompanies the models lists the released models, and provides a list of modeled parameters. The application note ***Simulation SPICE Models for Comlinear's Op Amps*** contains schematics and detailed information.

# CLC418 Applications

**Differential Line Driver With Load Impedance Conversion**

The circuit shown in the ***Typical Application*** schematic on the front page operates as a differential line driver. The transformer converts the load impedance to a value that best matches the CLC418's output capabilities. The single-ended input signal is converted to a differential signal by the CLC418. The line's characteristic impedance is matched at both the input and the output. The schematic shows Unshielded Twisted Pair for the transmission line; other types of lines can also be driven.

Set up the CLC418 as a difference amplifier:

$$\frac{V_d}{V_{in}} = 2 \cdot \left(1 + \frac{R_{f1}}{R_{g1}}\right) = 2 \cdot \frac{R_{f2}}{R_{g2}}$$

Make the best use of the CLC418's output drive capability as follows:

$$R_m + R_{eq} = \frac{2 \cdot V_{max}}{I_{max}}$$

where $R_{eq}$ is the transformed value of the load impedance, $V_{max}$ is the Output Voltage Range, and $I_{max}$ is the maximum Output Current.

Match the line's characteristic impedance:

$$R_L = Z_o$$
$$R_m = R_{eq}$$
$$n = \sqrt{\frac{R_L}{R_{eq}}}$$

Select the transformer so that it loads the line with a value very near $Z_o$ over your frequency range. The output impedance of the CLC418 also affects the match. With an ideal transformer we obtain:

$$\text{Return Loss} \approx -20 \cdot \log_{10} \left| \frac{n^2 \cdot Z_{o(418)}(j\omega)}{Z_o} \right| , \text{dB}$$

where $Z_{o(418)}(j\omega)$ is the output impedance of the CLC418, and $|Z_{o(418)}(j\omega)| << R_m$.

The load voltage and current will fall in the ranges:

$$|V_o| \leq n \cdot V_{max}$$
$$|I_o| \leq \frac{I_{max}}{n}$$

The CLC418's high output drive current and low distortion make it a good choice for this application.

**Lowpass Anti-aliasing Filter with Delay Equalization**

The circuit shown in Figure 7 is a 5th-order Butterworth lowpass filter with group delay equalization. $V_{in}$ needs to be a voltage source with low output impedance. Section A is a simple single-pole filter. Section B provides a single-pole allpass function for group delay equalization. Sections C and D are Sallen-Key lowpass biquad sections.

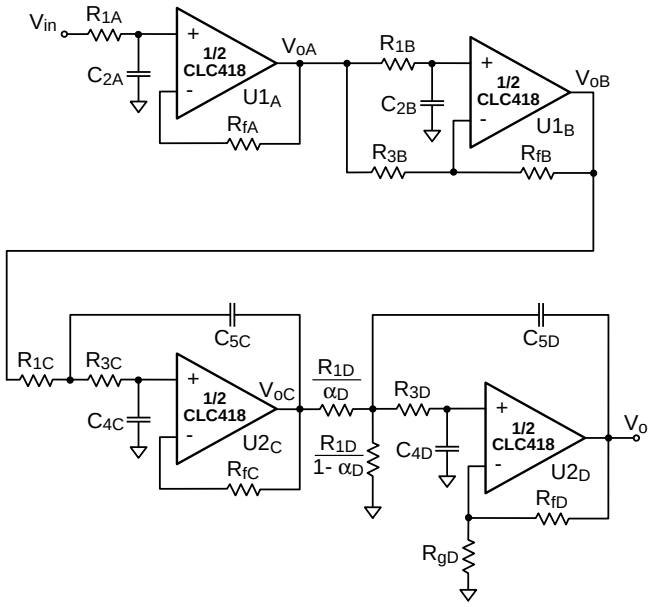



**Figure 7: Lowpass Anti-aliasing Filter**

The filter specifications we built to are:

| | |
|---|---|
| $f_c$ = 10MHz | (passband corner frequency) |
| $f_s$ = 20MHz | (stopband corner frequency) |
| $A_p$ = 3.01dB | (maximum passband attenuation) |
| $A_s$ = 30dB | (minimum stopband attenuation) |
| $H_o$ = 0dB | (DC gain) |

The designed component values are in the table below. The pre-distorted values compensate for the finite bandwidth of the CLC418.

| Component | Value | |
|---|---|---|
| | Ideal | Pre-distorted |
| $R_{1A}$ | 238Ω | 211Ω |
| $C_{2A}$ | 67pF | |
| $R_{fA}$ | 3.01kΩ | |
| $R_{1B}$ | 314Ω | 300Ω |
| $C_{2B}$ | 67pF | |
| $R_{3B}$ | 953Ω | |
| $R_{fB}$ | 953Ω | |
| $R_{1C}$ | 108Ω | 100Ω |
| $R_{3C}$ | 1.06kΩ | 1.07kΩ |
| $C_{4C}$ | 22pF | |
| $C_{5C}$ | 100pF | |
| $R_{fC}$ | 3.01kΩ | |
| $R_{1D}/\alpha_D$ | 256Ω | 227Ω |
| $R_{1D}/(1-\alpha_D)$ | 256Ω | 227Ω |
| $R_{3D}$ | 900Ω | 850Ω |
| $C_{4D}$ | 22pF | |
| $C_{5D}$ | 100pF | |
| $R_{fD}$ | 953Ω | |
| $R_{gD}$ | 953Ω | |

**Table 1: Filter Component Values**

The nearest standard values for capacitors and resistors were used to build this filter. The resistors were 1% tolerance, and the capacitors 5% tolerance. The ideal and measured gains are shown in Figure 8.

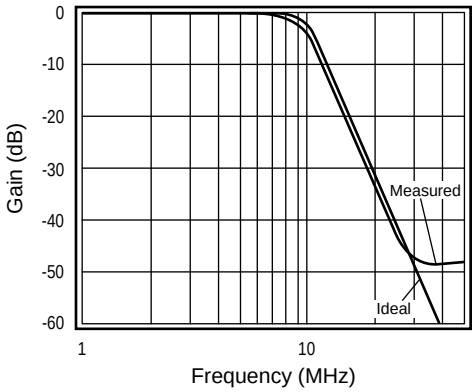



**Figure 8: Lowpass Anti-aliasing Filter Response**

To change the cutoff frequency of this filter, do the following:

- Determine the new cutoff frequency: $f_{c(new)} \le \frac{f_{3dB(418)}}{10}$, where $f_{3dB(418)}$ is the bandwidth of the CLC418
- Scale (multiply) all frequency specifications and plot axes by $f_{c(new)}/f_c$
- Make sure that your system requirements are met
- Scale (multiply) all capacitor values by $f_c/f_{c(new)}$
- Set the resistors to the Ideal Values in the table above (the pre-distorted values ***do not*** linearly scale with frequency)

For more information on the design of Sallen-Key filters and filter pre-distortion, see Comlinear's App Notes on filters.

**Precision Full-Wave Rectifier**

Figure 9 shows a precision full-wave rectifier using the CLC418. When $V_{in} > 0$, $D_1$ is on, $D_2$ is off, $V_2 = 0$ and an overall non-inverting gain is achieved. When $V_{in} < 0$, $D_1$ is off, $D_2$ is on, both $V_1$ and $V_2$ are positive, and an overall inverting gain is achieved. The output voltage of the rectifier is:

$$V_o = \begin{cases} \dfrac{\left(\dfrac{R_2+R_5+R_7}{R_1}\right)}{1+\left(\dfrac{R_2+R_5}{R_3}\right)\cdot\left(1+\dfrac{R_4}{R_6}\right)} \cdot |V_{in}|, V_{in} < 0 \\ \dfrac{R_2}{R_1}\cdot\dfrac{R_7}{R_5}\cdot|V_{in}|, V_{in} > 0 \end{cases}$$

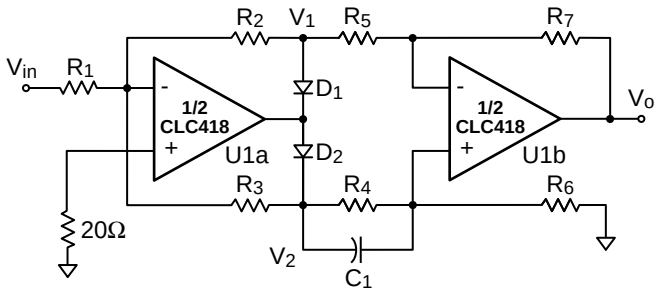



**Figure 9: Precision Full-Wave Rectifier**

Diodes $D_1$ and $D_2$ need to be Schottky or PIN diodes to minimize delay.

Select the voltage gain for U1a ($G_1 < 0$) and U1b ($G_2$). $G_2$ needs to be ≤ 1, approximately, to ensure realizable values of $R_4$. The overall gain is:

$$\frac{V_o}{|V_{in}|} = |G_1 G_2|, \quad |V_{in}| > 0$$

Set $R_2 = R_3$ to the recommended feedback resistor value for the gain $A_v = R_2$. You may need to increase $R_2$ and $R_3$ slightly to compensate for the delays through $D_1$ and $D_2$.

Set $R_7$ to the recommended feedback resistor value for the gain $A_v = (1 + G_2)$.

Calculate the ratio:

$$\frac{R_4}{R_6} = \frac{1+\dfrac{R_7}{R_2}\left(1+\dfrac{1}{G_2}\right)-\left(1+\dfrac{R_2}{R_3}\right)G_2-\dfrac{R_7}{R_3}}{\dfrac{R_7}{R_3}+\dfrac{R_2}{R_3}\cdot G_2}$$

If this ratio is negative, reduce $G_2$ and recalculate the values up to this point.

Calculate all other resistor values:

$$R_1 = \frac{R_2}{|G_1|}$$

$$R_5 = \frac{R_7}{G_2}$$

$$R_6 = \frac{R_5}{\left(1 + \frac{R_4}{R_6}\right)}$$

$$R_4 = R_5 - R_6$$

Notice that $R_4$ and $R_6$ are selected so that U1a and the diodes see a balanced load for both polarities of $V_{in}$.

The capacitor $C_1$ is optional. It helps compensate for the difference between the gains $V_o/V_1$ and $V_o/V_2$ at high frequencies. Both $R_4$ and $R_6$ must be > 0.

We built and tested a full-wave rectifier with the following values:

- $D_1 = D_2$ = Schottky Diodes, Digi-Key # SD101ACT-ND
- $R_2 = R_3 = R_7 = 1.00k\Omega$
- $R_1 = 1.00k\Omega$
- $R_5 = 1.50k\Omega$
- $R_6 = 882\Omega$
- $R_4 = 618\Omega$

The rectifier had equal inverting and non-inverting gains for frequencies less than 10MHz. The -3dB bandwidth was about 25MHz.

## Ordering Information

| Model | Temperature Range | Description |
|---|---|---|
| CLC418AJP | -40°C to +85°C | 8-pin PDIP |
| CLC418AJE | -40°C to +85°C | 8-pin SOIC |
| CLC418AJE-TR | -40°C to +85°C | 8-pin SOIC, 750pc reel |
| CLC418AJE-TR13 | -40°C to +85°C | 8-pin SOIC, 2500pc reel |
| CLC418ALC | -40°C to +85°C | dice (commercial) |

## Package Thermal Resistance

| Package | $\theta_{JC}$ | $\theta_{JA}$ |
|---|---|---|
| Plastic (AJP) | 80°C/W | 95°C/W |
| Surface Mount (AJE) | 95°C/W | 115°C/W |

## Reliability Information

| | |
|---|---|
| Transistor Count | 76 |
| MTBF (based on limited test data) | 34Mhr |

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