CLC935

CLC935 12-Bit, 15MSPS

Literature Number: SNOS863B

National Semiconductor

Comlinear CLC935
12-bit, 15MSPS A/D Converter

General Description

The Comlinear CLC935 is a high-speed high-performance 12-bit Analog-to-Digital converter. the CLC935 is a complete A/D subsystem, including 12-bit quantizer, track-and-hold, and references. The ECL compatible A/D has maximum sample rates of 15MSPS, allowing the user to digitize high-speed signals accurately.

The CLC935 has excellent dynamic performance characteristics which are thoroughly tested to insure that system performance goals will be met. Sampling at 15MSPS with a 400kHz input signal, the CLC935 achieves a typical 82dBc SFDR and an SNR of 65.5dB. Sampling a 5MHz signal can be done with 78dB of SFDR.

The CLC935 incorporates a complete two-pass architecture which is constructed from high-speed IC's on a thin-film substrate. Critical DC parameters are laser trimmed to assure accurate part-to-part matching. A CONVERT clock, power, and an analog input signal are all that are required for CLC935 operation.

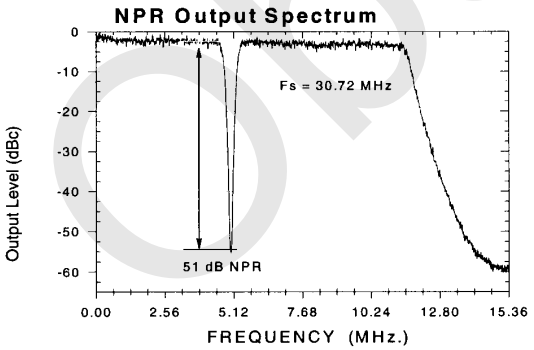
The CLC935-BC part is specified over the commercial temperature range, while the CLC935-B8C part is an extended temperature range, high reliability version. Both parts are packaged in 40-pin, 1.1 inch wide, ceramic DIPs with side-brazed leads for easy access and inspection.

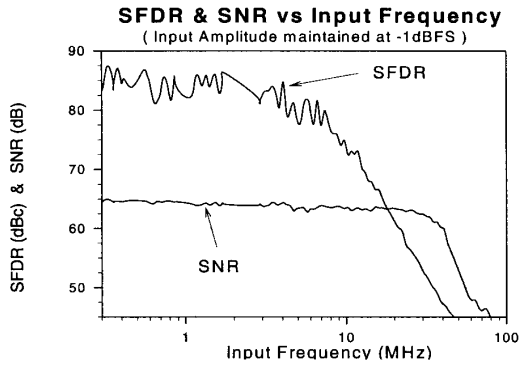
Features

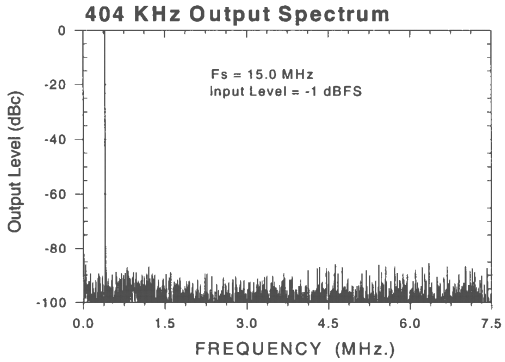
- Wide Dynamic Range
  82dB SFDR; F_{in} = 400kHz
  81dB IMD; F_{in} = 3.5MHz & 3.7MHz
  82dB SNR; F_{in} = 7MHz
- Fast recovery time
- 0.6 LSB differential linearity error

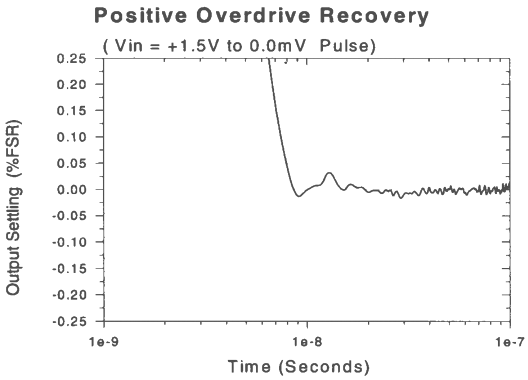
Applications

- Electronic imaging
- Digital communications
- IF sampling
- Radar processing
- FLIR processing
- Instrumentation









Printed in the U.S.A.

CLC935 Electrical Characteristics (V_{CC} = +5V, V_1 = +15V, $-V_2$ = -15V; V_{EE} = -5.2V; unless specified)

PARAMETERS	CONDITIONS	TYP	MIN/MAX RATINGS			UNITS	NOTES
	CLC935	25°	25°	0° to +70°	-55° to +125°		
DYNAMIC CHARACTERISTICS							
small signal bandwidth	VIN = 1/4 FS	150	100	100	100	MHz	
large signal bandwidth	VIN = FS	130	80	80	80	MHz	
slew rate		450	300	300	300	V/ms	
overvoltage recovery time	VIN = 2FS	14	25	25	25	ns	
effective aperture delay		-0.4	-1.5	-2.0	-2.0	ns	
aperture jitter		1.67	2.5	3.0	3.0	ps(rms)	
NOISE and DISTORTION (15MSPS)							
signal-to-noise ratio (not including harmonics)							
404kHz;	FS	65.6	63	63	61	dB	
4.984MHz;	FS	65.4	63	63	61	dB	A,B
7.225MHz; FS		65.2	63	63	61	dB	A,B
in-band harmonics							
404kHz;	FS-1dB	-82.3	-74	-72	-70	dBc	
4.984MHz;	FS-1dB	-78.1	-70	-68	-64	dBc	A
7.225MHz;	FS-1dB	-74.2	-68	-66	-62	dBc	A
intermodulation distortion							
f_1 = 3.49MHz @ FS-7dB; f_2 = 3.7MHz @ FS-7dB		-81.2				dBc	
noise-power-ratio	FS-12dB						
dc to 5MHz white noise; 2.7MHz notch		51.0				dB	
DC ACCURACY and PERFORMANCE							
differential non-linearity	dc; FS	0.6	1.0	1.0	1.0	LSB	
integral non-linearity	dc; FS	1.3	3.0	3.0	3.0	LSB	
missing codes		0	0	0	0	codes	
bipolar offset error		3.0	15	25	40	mV	
temperature coefficient				250	250	mV/°C	
bipolar gain error		2.0	5.0	5.0	5.0	%FS	
temperature coefficient				0.05	0.05	%FS/°C	
ANALOG INPUT PERFORMANCE							
analog input bias current		10	25	35	45	mA	
temperature coefficient		100		250	250	nA/°C	
analog input resistance		80	25	25	25	kW	
analog input capacitance		3.5	5.5	5.5	5.5	pF	
DIGITAL INPUTS							
input voltage	logic LOW		-1.5	-1.5	-1.5	V	
	logic HIGH		-1.1	-1.1	-1.1	V	
input current	logic LOW		1.0	1.0	1.0	mA	
	logic HIGH		1.0	1.0	1.0	mA	
DIGITAL OUTPUTS							
output voltage	logic LOW		-1.5	-1.5	-1.5	V	
	logic HIGH			-1.1	-1.1	-1.1	V
TIMING							
maximum conversion rate		15	15	15	15	MSPS	A,B,C
minimum conversion rate		0	0	0	0	MSPS	
data hold time		6.0	4.0	3.0	3.0	ns	
POWER REQUIREMENTS							
supply current (+V_{CC} = +5.0V)	15MSPS	146	175	175	175	mA	A,B,C
supply current (-V_{EE} = -5.2V)	15MSPS	647	750	750	750	mA	A,B,C
supply current (+V_1 = +15.0V)	15MSPS	16	20	20	20	mA	A,B,C
supply current (-V_2 = -15.0V)	15MSPS	28	35	35	35	mA	A,B,C
nominal power dissipation	15MSPS	4.75				W	PD

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Test Notes

A) Specification is 100% tested.
Military units are tested at -55°C, +25°C, +125°C;
Commercial units are tested at 25°C, guaranteed at 0° & 70°C.
B) Specifications are GROUP A inspection test.
C) Specification is 100% tested.
Military units are tested at -55°C, +25°C, +125°C.

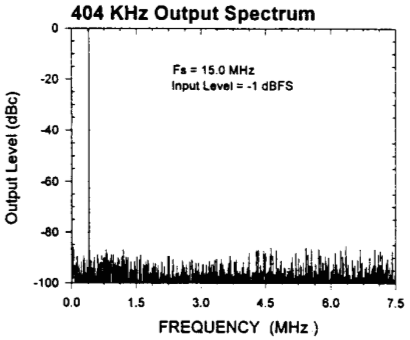
Test Level

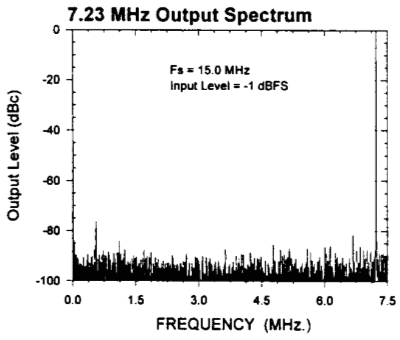
Test levels are derived from mil spec SUBGROUPS.

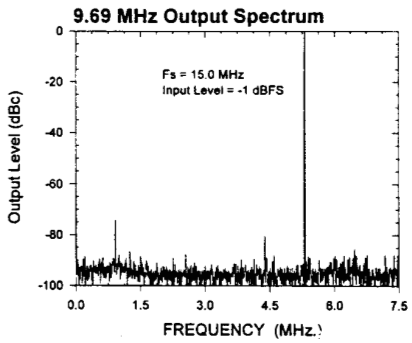
Static Tests	1) +25°C	2) +125°C	3) -55°C
Dynamic Tests	4) +25°C	5) +125°C	6) -55°C
Functional Tests	7) +25°C	8) +125°C and -55°C	
Switching Tests	9) +25°C	10) +125°C	11) -55°C

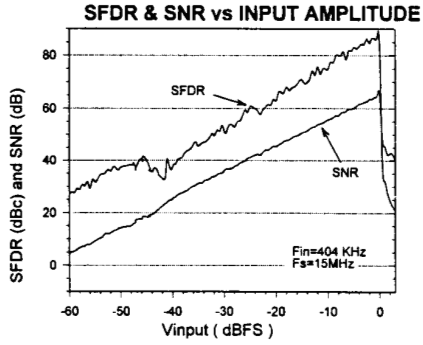
Note: Junction temperature rise above case = 16°C; θ_{CA} = 16°C/W; θ_{CA} = 7°C/W @ 500LFPM. Use of a CHO-THERM® #T274, or similar product from Chemetrics (1-800-225-1936), can lower case-to-ambient rise.

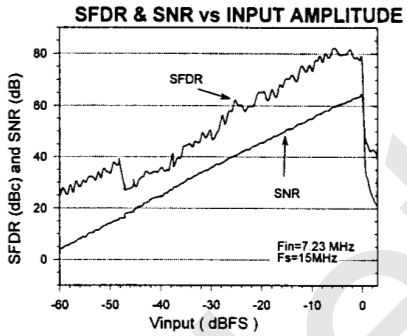
CLC935 Typical Performance Characteristics (T_C = 35°C; 15MSPS)

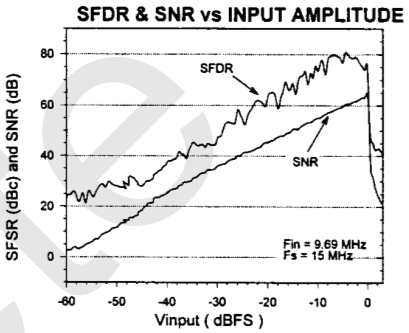


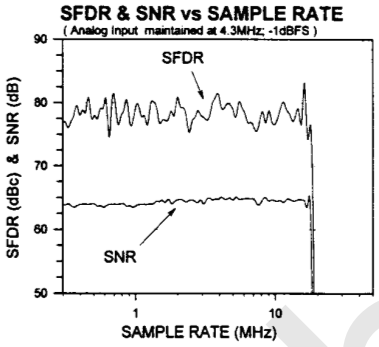


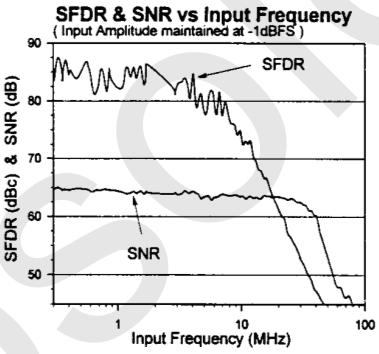


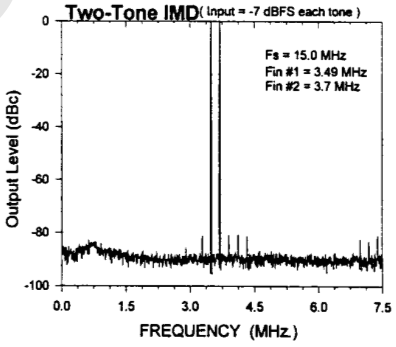


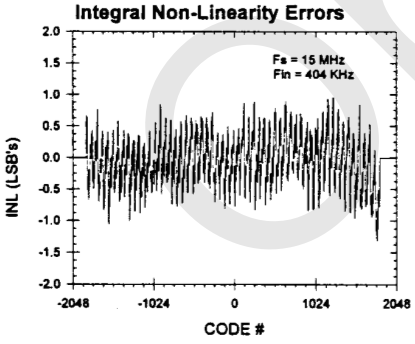


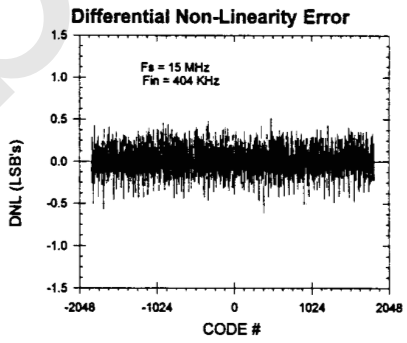


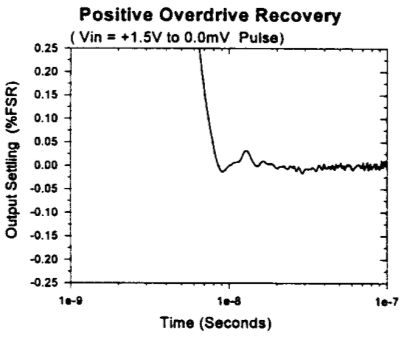


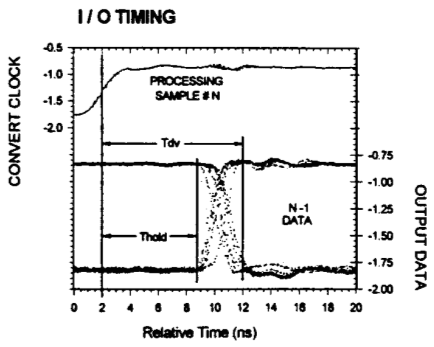


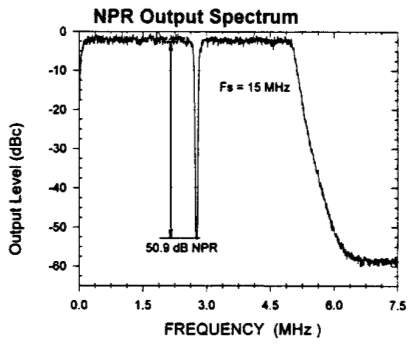


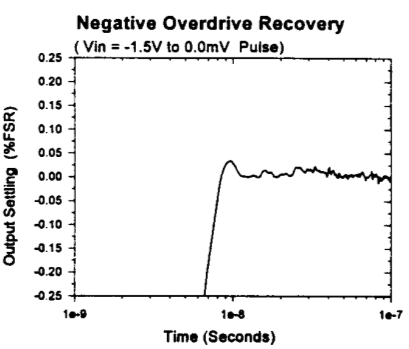












Recommended Operation Conditions

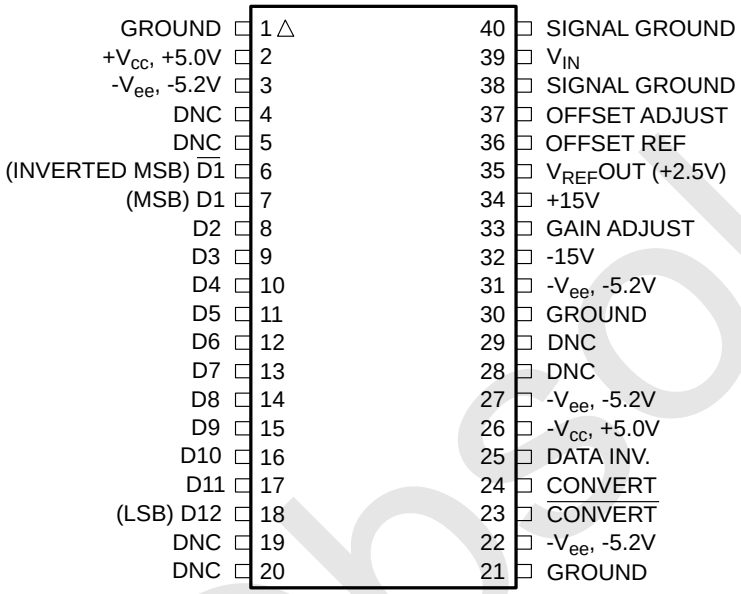
positive supply voltage ($+V_{CC}$)	+5V ±5%
positive supply voltage ($+V_1$)	+15V ±5%
negative supply voltage ($-V_{EE}$)	-5.2V ±5%
negative supply voltage ($-V_1$)	-15V ±5%
differential voltage between any two GND's	<10mV
analog input voltage range (Full Scale)	±1.0V
digital input voltage range	-2.0V to 0.0V

*Note: Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to maximum ratings for extended periods may affect device reliability.

Absolute Maximum Ratings*

positive supply voltage ($+V_{CC}$)	-0.5 to +7.0V
positive supply voltage ($+V_1$)	-0.5 to +18V
negative supply voltage ($-V_{EE}$)	+0.5 to -7.0V
negative supply voltage ($-V_1$)	+0.5 to -18.0V
differential voltage between any two GND's	200mV
analog input voltage range	$-V_{EE}$ to $+V_{CC}$
digital input voltage range	+0.5V to $-V_{EE}$
gain adjust voltage range	$-V_{EE}$ to $+V_{CC}$
output short circuit duration (one pin to ground)	Infinite
junction temperature	+175°C
operating temperature range	
CLC935-BC	0°C to +70°C
CLC935-B8C	-55°C to +125°C
storage temperature range	-65°C to +150°C
lead solder duration (+300°C)	10 sec

Pinout & Pin Description and Usage



ECL-Level Digital Inputs

- **CONVERT, $\overline{\text{CONVERT}}$** (Pins 23, 24) : "Differential Convert Command" initiates a new conversion cycle on the rising edge of CONVERT.
- DATA INV (Pin 25): DATA INVERT is an active HIGH (grounded) ECL input which causes the data outputs [D1 to D12] to be inverted. In normal operation, DATA INV is left floating or tied to ECL logic LOW.

ECL-Level Digital Outputs (Note: all ECL digital outputs have internal series resistances such that Z_{out} = 50Ω ±3Ω)

- (MSB) D1-D12 (Pins 7 to 18): Digital Data Outputs. D1 is the MSB; D12 is the LSB. In their normal state, the digital outputs offer Offset Binary output coding.
- **$\overline{\text{(MSB) D1}}$** (Pin 6): Inverted version of the MSB, used for 2's Complement coding.

Analog Input

- **V_{IN}** (Pin 39): Analog input with a $2.0V_{pp}$ input range from +1.00V to -1.00V.
- **GAIN ADJUST** (Pin 33): The GAIN ADJUST has a +4V to +1V input range and scales the analog input full-scale range by -10% to +10% respectively. If unused, Gain Adjust should be left floating.

Miscellaneous

- **V_{REF}** (+2.5V) (Pin 35): V_{REF} is a highly stable +2.500V voltage reference. (Recommended current drain ≤ 2mA.)
- **D.N.C** (Pins 4, 5, 19, 20, 28, 29): Do Not Connect.
- **OFFSET ADJUST** (Pin 36): OFFSET ADJUST has a GROUND to OFFSET REFERENCE input range and scales the analog input offset by Ò0.1V. If unused, OFFSET ADJUST should be left floating.
- **OFFSET REFERENCE** (Pin 37): OFFSET REFERENCE tracks gain adjustments and is used for offset voltage adjustment.

Power and Ground

- **+5V**, Pins 2,26; **+15V**, Pin 34; **-5.2V**, Pins 3, 22, 27, 31; **-15V**, Pin 32; **GROUND**, Pins 1, 21, 30, 38, 40.

Discussion of CLC935 Plots and Specifications

Some of the preceding performance plots require more explanation than is feasible in the caption. This section goes into more detail as to how these plots were generated, and how they might be utilized. Additional information can be found in the application note AD-01 ... "Designing with High-Performance A/D converters".

Spectral Plots

Three frequency spectrum plots are shown for the CLC935 ADC. Low and High "Nyquist - band" (<Fs/2) single tone input frequencies were selected along with a "super - Nyquist" (>Fs/2) tone. FFT analysis were performed using 4K point (4096), rectangular windowed data. Valid ADC input frequencies were chosen to land within the center of a prime numbered FFT frequency bin.

SFDR and SNR vs. Input level Plots

Fixed frequency input amplitude sweeps were run and the 4K point FFT analysis summary plotted for the three Spectral Plot input frequencies. Signal to Noise Ratio (SNR) is the power ratio between the fundamental and the spectral noise (the first 10 harmonics are excluded from the noise power calculation). As the signal level is reduced from full scale, the noise power remains relatively constant. This results in a backward declining straight line shown as SNR vs Input Amplitude. In some converters the 'noise' is not independent of the input signal level and hence the line's slope may vary.

The Spur-Free Dynamic Range (SFDR) performance is less uniform. SFDR is the magnitude ratio of the fundamental to the next largest spectral line. ADC differential & integral linearity, along with sample to sample step magnitude, create a unique spectral response for each ADC and operating condition. Because sub-ranging ADCs are susceptible to conversion errors at their "coarse-quantization" thresholds (see Principle of Operation), spectral variations become less predictable at these operating points. Special care has been taken in the design of these converters to minimize the characteristic SFDR performance dip in the -20 to -40 dBFS input amplitude ranges.

SNR and SFDR vs. Conversion Rate

The CLC935 converter has an asynchronous timing schemes which are triggered by the rising edge of the CONVERT clock. When the conversion cycle is complete, the T/H amplifier resumes its "track" mode of operation. Because of this timing scheme, ADC performance is relatively independent of sample rate.

SNR, and SFDR vs. Input Frequency

These plots show the variation in converter performance relative to analog input frequency. Input frequencies to about 65MHz (the Large Signal Bandwidth) are included, and can be useful for under-sampled applications. Beyond the Large Signal Bandwidth, performance for large signals degrades quickly. The small-signal-bandwidth (measured with analog inputs below $500mV_{pp}$) performance does not degrade until around 135MHz.

Two Tone Linearity Spectrum

In a linear system, the input signal can be viewed mathematically as a superposition of sinusoids (Fourier Transform). The system output can be predicted by the superpositioning of the individual effects on each of the sinusoid inputs. For example, if a linear network is presented with a single tone signal F_1 and the result is an attenuation by a factor A_1, and it is then presented with another frequency F_2 attenuated by A_2 through the system, then the expected output for an input of F_1+F_2 would be $A_1F_1 + A_2F_2$. If the network is not linear, the output will contain frequency components in addition to those present at the input. The most common products likely to be present in the output are at $MF_1 \pm NF_2$, where M and N are integers, and F1 and F2 are the two input frequencies.

In the ***Two-Tone IMD*** plots, two sinusoids are passively filtered and summed to comprise the ADC input. The V_{in} peak-to-peak magnitude is set so that the ADC is operating at -1dBFS and the test tone frequencies are shown on the various plots.

Differential & Integral Linearity plots

Differential Non-Linearity (DNL) is computed by collecting a large data series and calculating the difference between its code density and the code density of an ideal sine-wave. The ADC is sampled at its rated maximum conversion rate with a low frequency (approx 400kHz), -1dBFS sine-wave input. The Integral Non-Linearity (INL) is computed by fitting the summed DNL data to a straight line. Deviations of either DNL or INL are usually specified in fractional Quantization levels (LSBs). DNL describes the code to code uniformity.

Digital I/O Timing plot

The digital outputs make their transition and become valid TDVns after the rising edge of the CONVERT signal. The actual time to this transition varies slightly from output bit to output bit. The amount of this variation is small and well within the timing needs of most systems. In the I/O Timing plot, the transition of the 6 most significant output bits are shown with reference to the CONVERT clock.

Noise Power Ratio (NPR) plots

NPR testing simulates multichannel communication applications. The ADC input is comprised of broadband random noise (Nyquist band limited) with a deep, narrow band of noise notched out. The NPR is simply the depth of the notch in the FFT spectrum. The non-coherent nature of the input signal requires that the data be windowed in order to minimize spectral "leakage" into adjacent FFT filter bins. A four term window function similar to Blackman-Harris was used on 4K point data sets and 10 FFT results were averaged. The input power is varied until a peak NPR figure is found. Distortion products from outside the notched band fall into the FFT notch and degrade NPR. Thus, channel to channel isolation can be determined.

Overdrive Recovery Plots

These plots indicate ADC time domain settling from a 50% overdrive condition. A very fast, +1.5V or -1.5V to 0.00V pulse, with a period slightly shorter (100ps) than that of the CONVERT clock, is used as the input source. The ADC is therefore “slipped” through the input wave form and the output data is plotted after being smoothed using a 5 point sliding average. The slip rate (period difference between clock and input) and data point number are used to generate the time axis. For the sake of plot resolution, only fine settling is shown.

Understanding A/D Dynamic Specifications

Analog-to-Digital converters are specified in many ways. As a component achieves higher performance, its specifications and their definitions can become more critical. Fortunately, the vast number of converter applications can generally be placed into one of two classes. These are processed data and non-processed data applications. The distinction seems quite simple but the split implies a completely different approach in specifying A/D converters for a given application.

The processed data area includes the frequency domain applications which employ Fourier processing (FFT). Also in this category are the highly averaged applications, usually concerned with low noise. In each case, the converter’s data is averaged or convolved mathematically. This processing reduces the apparent noise level in the output data. For FFTs, the noise is simply spread over a large number of frequency bins. For simple averaging approaches, the Gaussian distribution of noise is greatly reduced, appearing to increase the converter’s resolution. Processed applications include radar, network and spectrum analyzers, communications receivers, etc.

The non-processed applications tend to take the converter’s data in its original form with very little processing. This means that the noise reduction benefits of the processed applications are not seen. The non-processed area is composed primarily of time domain applications like imaging, DSO’s, ultrasound, etc.

The processed vs. non-processed issue has several implications in terms of converter specifications. For the non-processed (time domain) systems the dominant converter specifications deal with noise (SNR) and converter accuracy (DNL). The converter’s quantization noise and input stage noise dominate converter accuracy . The harmonic distortion (primarily INL) of the converter is generally of little interest given that most time domain applications present data for visual analysis and tend to focus on “local” accuracy rather than over the full input range. “Local” accuracy is best described through the standard noise measurements, such as SNR and DNL.

In the frequency domain application areas, the noise of the converter is processed to the point where, for almost all systems, it is no longer of issue. This is manifested as a reduction in the apparent noise floor. The actual RMS noise is not reduced, but is spread over more and more frequency bins as processing levels are increased. Unfortunately, the harmonic distortion performance of the converter is not affected by increased processing. This makes the harmonic performance, or more specifically the spurious performance, the dominant error source for frequency domain applications. SFDR becomes the dominant specification for determining converter performance in the frequency domain.

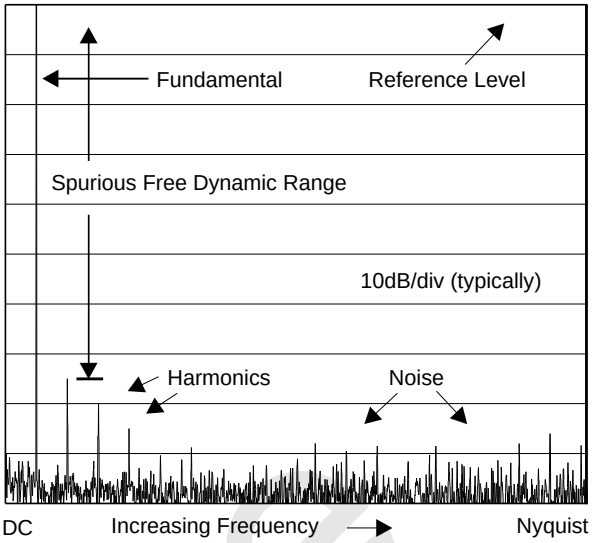
Signal-to-Noise Ratio (SNR) is the ratio of the power contained in the fundamental signal compared to the power contained in the entire noise floor. That is to say all individual noise components are added together to arrive at an integrated noise power. For SNR, harmonic power is excluded from the noise measurement. SNR is particularly important in time domain applications like digital image processing and infrared imaging, where conversion accuracy can be heavily degraded by integrated noise.

Signal-to-Noise-and-Distortion (SINAD) is the ratio of the fundamental signal power to the power at all other frequencies. This includes all noise as well as all harmonics. SINAD is a worst case specification for A/D converters, combining variables from both frequency and time domains. The value of SINAD in high-performance converter applications is not clear since it does not accurately predict the best converter for a given application. Because data converter applications tend to fall into either noise-sensitive time-domain applications or distortion-sensitive frequency-domain applications, SINAD is not specified for the CLC935 data converter.

Total Harmonic Distortion (THD) is the combined power of a specified number of harmonics, compared to the power of the fundamental signal. Harmonics are located at predictable frequencies, spaced at integer multiples of the fundamental signal. For example, a 1MHz fundamental would generate harmonics at 2MHz, 3MHz, 4MHz, ... and so on. In practice, only the first five harmonics contribute significantly to THD, although more may be included in the measurement. THD does not tend to apply well in frequency domain applications which are by their nature very SFDR oriented. In time domain applications, THD is indicative of full-scale input range distortion, however the high-performance time domain applications are generally most interested in local distortion performance. Local distortion and accuracy is dominated by DNL. The use of THD for applications requiring local performance is not likely to yield accurate or repeatable results and therefore THD does not appear in the CLC935 specifications.

Spurious-Free-Dynamic-Range (SFDR) is the "clean" dynamic range of the converter, free from harmonic and spurious signals. SFDR is ratio of the power of the fundamental compared to the power of the next largest component in the frequency spectrum. The SFDR specification is especially important to frequency domain applications which perform Fourier transforms to analyze the converter's output data. Processed applications like radar and network analyzers are typical areas where SFDR offers a direct prediction of converter's performance at both the system and component levels. SFDR is the single best specification for selecting a converter to be used in a frequency domain application.

In-Band Harmonics (IBH) is the ratio of the power of the fundamental compared to the power of the single largest harmonic. This specification is very similar to SFDR, but since it only considers a fairly limited number of harmonics, it is potentially an incomplete gauge of converter performance. SFDR is more stringent and should be used whenever possible in lieu of IBH.



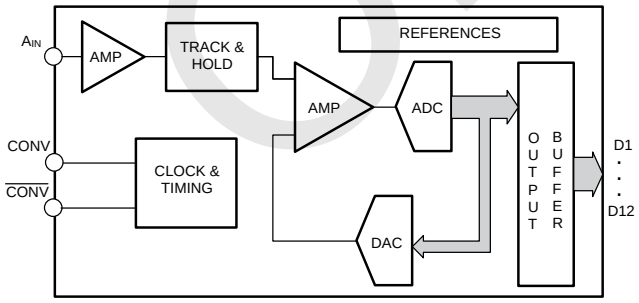
Typical Frequency Spectrum and its Components

CLC935 Applications Information

In high-speed data acquisition systems, overall performance is often determined by the A/D converter. Accordingly, special attention should be given to the data converter, its operation, and its environment. To assist in this process, information on these critical items has been included in this data sheet. Additional information on using high-performance A/D converters can also be found in application note AD-01.

Principle of Operation

The CLC935 is a complete two step, sub-ranging A/D converter, with input buffering, internal track-and-hold, quantizer, and all necessary voltage references. The block diagram for the CLC935 data converter is shown below.

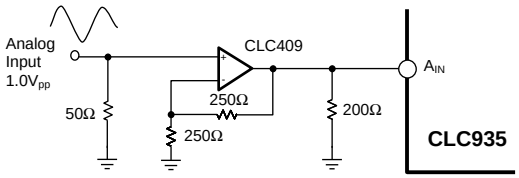


CLC935 Functional Block Diagram

The conversion cycle is initiated on the rising edge of the CONVERT signal. The analog input is sampled by the track-and-hold amplifier and is then digitized with an 8-bit digitizer. The 6 MSBs of this conversion are the "coarse-quantization", which drive a 14-bit accurate DAC to match the input level. The DAC output is then subtracted from the original analog input to generate an error signal, which is then digitized. The two digitized results are combined to form the 12-Bit accurate output. Error correction and ECL output buffering is also provided by the CLC935 converter.

Analog Input Driving Circuits

The high dynamic range of the CLC935 places high demands on any analog processing circuitry that precedes the data converter. This is particularly true in the area of harmonic distortion where the A/Ds' performance often exceeds -80dBc. Fortunately, the each employs an internal buffer for the analog input, and external buffering circuits are usually not required. Both the CLC207 and the CLC409 amplifiers can be configured for better than -80dBc harmonic distortion (note that the CLC207 does support 12-bit settling performance necessary for "time domain" applications). This makes them ideal choices for any analog signal conditioning or buffering that may be required.



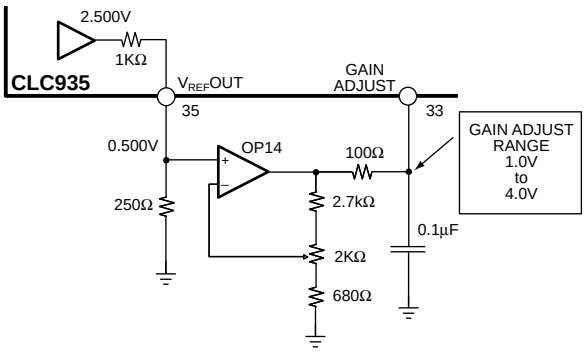
Analog Input Buffering

Gain Adjust

The CLC935 data converter's input range can be adjusted ±10% from its nominal ±1V range. The input range is controlled by adjusting the gain of the internal input buffer. This gain is controlled by the applied voltage at the GAIN ADJUST (pin33). The relationship between applied voltage at pin 33 and the analog input range is:

analog input range =
$\pm [2V + (0.129)(V_{GAIN\ ADJUST} - 2.5V)]$

GAIN ADJUST pin(33) Voltage	Analog Input Range
1.0V	$1.8V_{pp}$
2.5V or open	$2.0V_{pp}$
4.0V	$2.2V_{pp}$

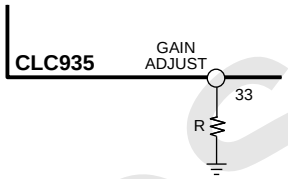


Analog Input Range Adjust Circuit

A resistor from GAIN ADJUST to ground provides a second method of adjusting the analog input range. This technique will decrease the data converter's gain and increase the analog input range.

$$R = \frac{774 - 4{,}800\,\Delta}{\Delta}$$

Where Δ is the gain change factor, i.e 0.01 equals 1% change.



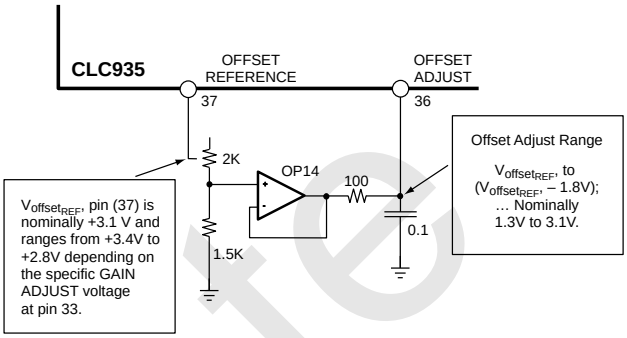
Alternate Input Range Adjust Circuit

Offset Adjust

Typically the center of the ±1V analog input range is laser trimmed to 0V during construction. By applying a voltage at the OFFSET ADJUST (pin 36), the analog input offset can be adjusted approximately ±100mV around ground. The applied voltage at pin 36 can range from GROUND to $V_{OFFSET\ REFERENCE}$. If the OFFSET REFERENCE (pin 37) voltage is used to generate the applied OFFSET ADJUST voltage, adjustments in the analog input range offset will track any adjustments made to the analog input range gain. Analog input range gain and offset adjustments are tightly coupled when the OFFSET REFERENCE is used to generate the OFFSET ADJUST applied voltage. Self-calibration techniques for adjusting offset and gain should use OFFSET REFERENCE in adjusting the offset.

Analog input offset and gain adjustments can be made independent of each other if the VREF OUT (pin 35) is used to generate the applied OFFSET ADJUST voltage instead of the OFFSET REFERENCE voltage. If the VREF OUT approach is adopted, the CLC935 offset and gain will be independent of each other, but will likely need an iterative adjustment approach where both offset and gain are successively adjusted until the desired result is obtained.

Offset Adjust Range pin (36)	Analog Input Offset
$V_{OFFSET\ REFERENCE}$	+100mV
open	0mV
GROUND	-100mV



Offset Adjust Circuit

The OFFSET ADJUST and GAIN ADJUST pins are sensitive to noise; and should be bypassed to ground with 0.1µF ceramic capacitors. If the OFFSET ADJUST and GAIN ADJUST pins are not used, then they should be left floating.

CONVERT Clock Generation

All high-speed high-resolution A/D converters are sensitive to the CONVERT clock quality. With a full scale 7MHz analog input signal, the slew rate at the 0V crossing is 90LSB/ns. An error (jitter) of as little as 5ps in the clock edge will yield a 0.5LSB error at the A/D output. This is as great or greater than any other error source likely to be present. This type of clock error or clock jitter is most easily seen in the form of poor SNR (signal-to-noise ratio). If the SNR is below expectations, clock jitter should be investigated.

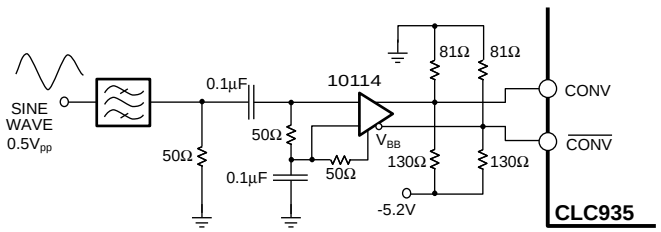
$$SNR_{MAX} = 20\log\left[\frac{1}{2\pi f_{in} jitter_{RMS}}\right]$$

where:

$$jitter_{RMS} = \sqrt{\left(clock\ jitter_{RMS}\right)^2 + \left(analog\ jitter_{RMS}\right)^2}$$

It should also be noted that jitter in the analog input source will have the same detrimental effect on SNR. Analog input signal jitter is usually only a problem in evaluation setups, and does not generally present a problem in full systems.

Low-jitter crystal controlled oscillators make the best CONVERT clock sources. If the CONVERT clock is generated from another type of source, by gating, dividing or other method, it should be registered by the original clock as the last step. This should keep jitter terms from compounding.



Sine to ECL Conversion Circuit

For variable frequency CONVERT clocks, low-phase-noise frequency synthesizers like the Fluke 6080A or the HP8662 are good choices. Sinusoidal sources of this type will require a sine-to-ECL conversion circuit, such as the one above. This circuit operates consistently with low level inputs (0dBm), but is sensitive to noise (jitter) from the synthesizer. Maintaining a larger input level (> +6dBm), greatly reduces this jitter contribution.

Output Coding

The CLC935 data converter is capable of producing four possible digital output formats: offset binary, two's complement, and their inverted versions. In offset binary the outputs count from 000h to FFFh, as the input varies from -FS (full-scale) to +FS. For two's complement output coding, the MSB in the offset binary format is inverted. On the CLC935 converter, this is achieved by using the $\overline{D1}$ ($\overline{MSB}$) (pin 6) output rather than the D1(MSB) (pin 7). When using inverted coding formats, the data outputs D2 - D12(LSB) are inverted by tying DATA INV (pin 25) to an ECL logic HIGH (or grounding). For non-inverted operation DATA INV should be left floating, or tied to an ECL logic LOW.

Analog Input	Offset Binary	Two's Complement
+FS - 1 LSB	1111 1111 1111	0111 1111 1111
+FS - 2 LSBs	1111 1111 1110	0111 1111 1110
+FS - 3 LSBs	1111 1111 1101	0111 1111 1101
-	-	-
-	-	-
mid-scale + 1/2 LSB	1000 0000 0000	0000 0000 0000
mid-scale - 1/2 LSB	0111 1111 1111	1111 1111 1111
-	-	-
-	-	-
-FS + 2 LSBs	0000 0000 0010	1000 0000 0010
-FS + 1 LSB	0000 0000 0001	1000 0000 0001
-FS	0000 0000 0000	1000 0000 0000

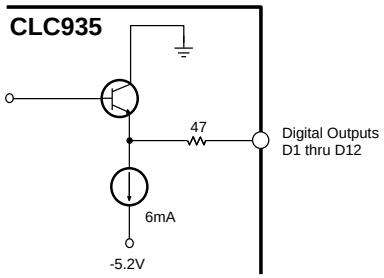
Output Data and "Data Ready"

The CLC935 has data latency of one clock cycle. This means that a sample taken on the rising edge of CONVERT (t_N) will appear at the output on the t_{N+1} clock cycle of the CLC935. The internally latched data from the previous conversion (t_{N-1} CLC935) is latched to the digital outputs on the rising edge of CONVERT. The previous output data is guaranteed to be valid for at least tHLD after the rising edge of CONVERT and the new output data will be stable t_{DV} after the rising edge of CONVERT (see timing diagram).

Since the output data is synchronous with the rising edge of the CONVERT, its falling edge should be used to generate the output latch clock, or DATA READY signal, if the system so requires. This will limit the bulk of the digital switching noise to a period well away from the sensitive analog processing inside the data converter. The use of the rising edge of CONVERT for Data Ready, and buffer clocking signals, is not recommended. Separate drivers for CONVERT and output latch strobing should be used to minimize corruption and jitter in the CONVERT signal.

Digital Interface and Termination Differences

All high-resolution A/D converters are susceptible to performance degradation if interference from the digital outputs is allowed to couple back to the analog input. Capacitive coupling back to the A/D input can result in increased harmonic distortion, or an elevated noise floor. This "noise" tends to be highly correlated to the input signal, and is difficult to remove through standard DSP noise reduction techniques. To minimize this effect, the CLC935 data converter employs ECL "compatible" outputs rather than larger swing TTL compatible outputs. Additional measures to reduce output-to-input coupling have resulted in some slight differences when interfacing to the data converter outputs as compared with true ECL. Significant system power and digital noise reduction for the CLC935 data converter results from the use of on chip ECL pull-down sources for each of the twelve bit lines as illustrated in the figure below. As shown, series termination resistors are included on each data bit in order to drive external 50Ω transmission lines (i.e. PCB traces with Zo = 50Ω).

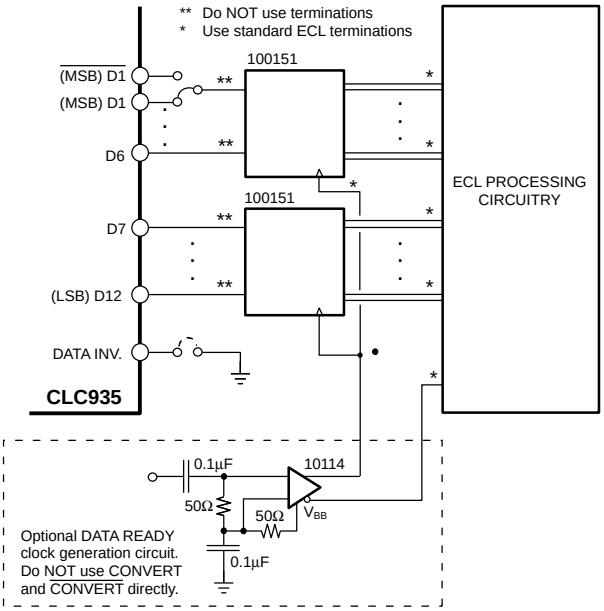


Internal ECL Termination Circuit

The CLC935 data converter outputs are 10KH ECL logic compatible with internal constant-current pull-downs, and are designed to be connected directly to 10KH level inputs with no external termination. The power dissipation in each termination is the 6mA standing current, multiplied by the 5.2V supply, or 31mW per output. For a 12-bit data converter, this represents 375mW. When compared to external (50Ω/-2V) Thevenin terminations, the power savings is 1.2W.

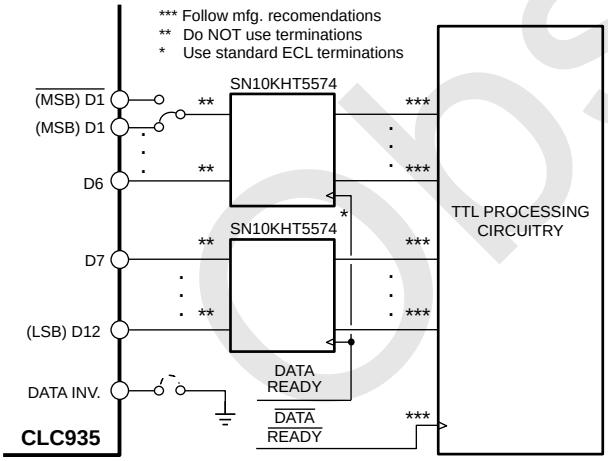
Output Latching and Level Translation

Parasitic capacitances and inductances should be minimized, when interfacing to the CLC935 outputs. Output latches (10176) or buffers should be placed as close as practical to the output pins. If these output latches drive a significant trace load on the same board as the data converter, differential output latches (100151) and trace routing should be used.



Recommended Output Buffering Circuits

In many systems, DSP and other forms of processing will employ TTL or CMOS circuitry. The output logic levels of the CLC935 data converter will need to be translated to match those of the processing circuitry. Several options and translators exist to perform this task. Special care must be used if "10125" type circuits are used since these devices are not particularly suited to a high-resolution, low-noise, analog environment. Other options include TI's 105574 Latched Translator.



ECL to TTL/CMOS Level Translator Options

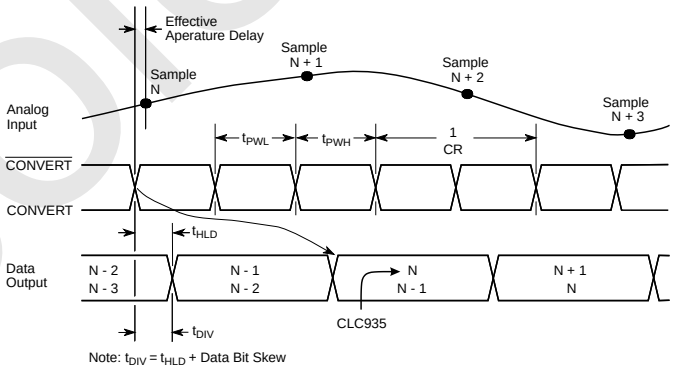
Power Supplies, Grounding, and Bypassing

To obtain the best possible performance from any high-speed device, the design engineer must pay close attention to power supplies, grounding and bypassing. This applies not only to the A/D data converter itself but throughout the system as well.

The recommended supply decoupling scheme is as follows: One 0.01µF to 0.033µF chip capacitor at every supply pin, with a +6.8µF to +10µF tantalum for each of the four main supply feeds (within a few inches of the ADC). Note that supply feeds with excessive digital switching noise may require separate filtering using ferrite beads, additional capacitance, or split supplies. Proper bypassing of all other integrated circuits, especially logic circuits, should minimize power supply and ground transients.

All of the CLC935 data converter grounds are internally connected. A single low-impedance ground plane is recommended. Split analog and digital grounds are not recommended. The SIGNAL GND is used internally for the track-and-hold and buffering amplifiers, while the other GROUND pins are essentially power supply returns.

The SIGNAL GND pins (pins 39 & 40) are very sensitive nodes, and should have a solid, low-impedance, ground connection. The path that the input signal and its return currents follow must be isolated from other circuitry. Single-point grounding at the data converter should minimize common impedance paths which would allow other signals to directly couple into the analog input, affecting accuracy.



CLC935 Timing Diagram

Thermal Considerations

The following strategies can be applied to minimize junction temperatures:

a) A thick copper ground plane ... an appreciable amount of heat is conducted out of the A/D through its leads.

b) A copper or aluminum stand-off between the ground plane and the bottom of the data converter package (thermal paste may be useful).

c) A CHO-THERM® pad between the ground plane and the bottom of the data converter package. To maximize heat conduction leave a patch of exposed (no solder mask) ground plane under the data converter.

d) Moving air over the A/D converter.

e) Heat sink attached to the converter available from National Semiconductor.

Evaluation Board and Printed Circuit Board Layout

The keys to a successful CLC935 layout are a substantial low-impedance ground plane, short connections (in and out of the data converter), and proper power supply decoupling. The use of a socket for the CLC935 data converter is specifically not recommended in the final system design.

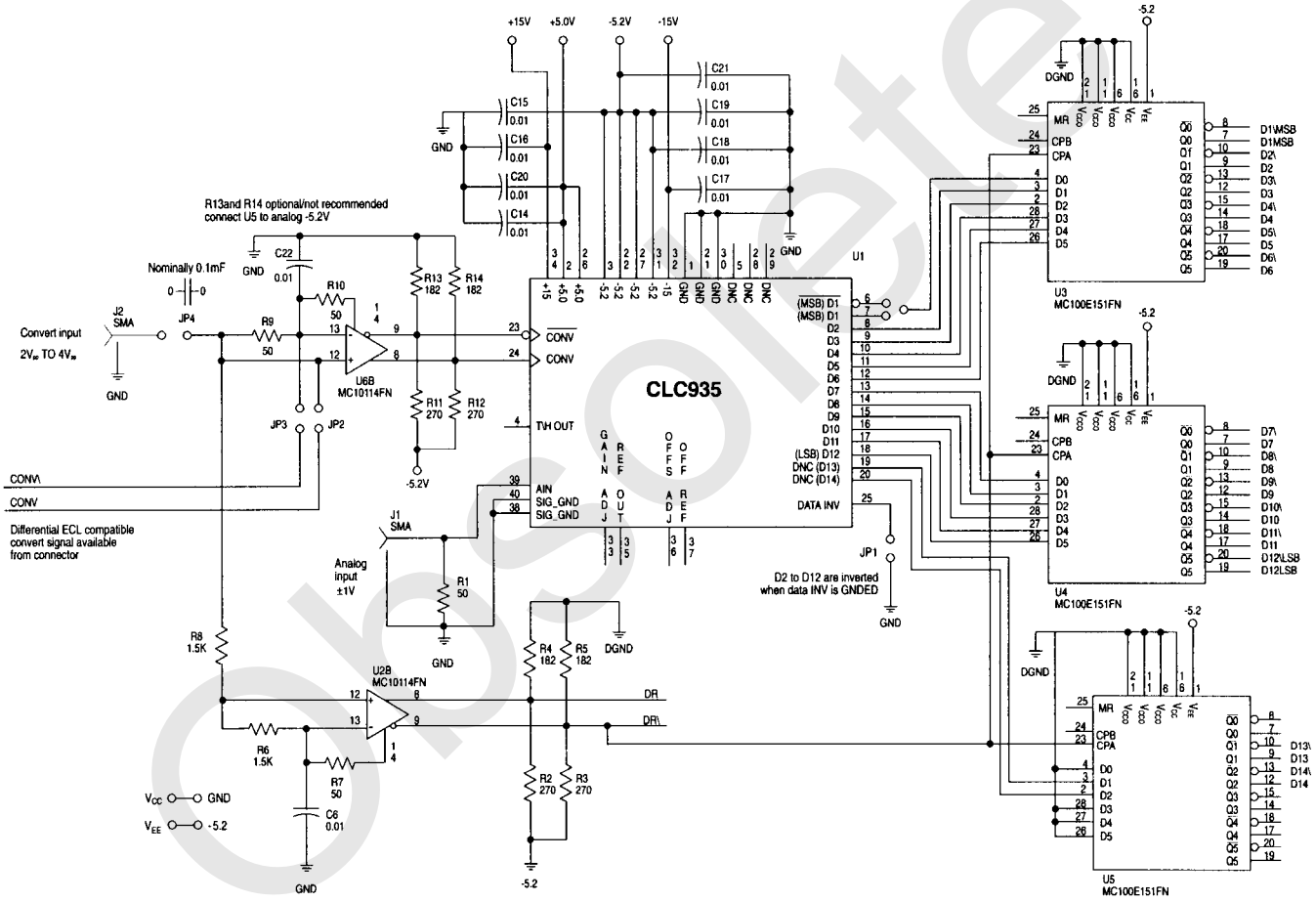
The CONVERT clock line traces should be equal length. If they are not equal, the edges may not arrive at the A/D at the same time, which may allow the clock signals to more easily couple into the analog input.

Evaluation boards are available for the CLC935 (assembled - "E935PCASM"). The boards can be used to quickly evaluate the performance of the CLC935 data converter. Use of the evaluation board as a model is highly recommended.

Ordering Information

Model	Temperature Range	Description
CLC935BC	0°C to +70°C	Commercial
CLC935B8C	-55°C to +125°C	MIL-STD-833, class B

*Note: operating temperature range is -55°C to +125°C, however, the devices are specified over the above listed temperature ranges.



CLC935 Complete System Circuit

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