

## 1.8V Low Voltage Comparator with Rail-to-Rail Input

Check for Samples: [LMV7251](#), [LMV7255](#)

### FEATURES

- ( $V_S = 1.8V$ ,  $T_A = 25^\circ C$ , Typical Values Unless Specified).
- Single or Dual Supplies
- Low Supply Voltage 1.8V to 5.0V
- Ultra Low Supply Current 11 $\mu A$
- Low Input Bias Current 14nA
- Low Input Offset Current 200pA
- Low Input Offset Voltage  $\pm 0.3mV$
- Response Time 670ns (20mV Overdrive)
- Input Common Mode Voltage 0.1V Beyond Rails

### APPLICATIONS

- Mobile Communications
- Laptops and PDA's
- Battery Powered Electronics
- General Purpose Low Voltage Applications

### Typical Circuit

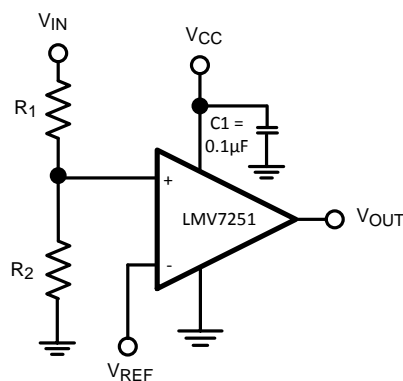


Figure 1. Threshold Detector

### DESCRIPTION

The LMV7251/LMV7255 are rail-to-rail input low voltage comparators, which can operate at supply voltage range of 1.8V to 5.0V. The LMV7251/LMV7255 are available in space saving SC-70 or SOT-23-5 packages. These comparators are ideal for low voltage and space critical designs.

The LMV7251 features a push-pull output stage. This feature allows operation with minimum power consumption when driving a load.

The LMV7255 features an open drain output. This allows the connection of an external resistor at the output. The output of the comparator can be used as a level shifter.

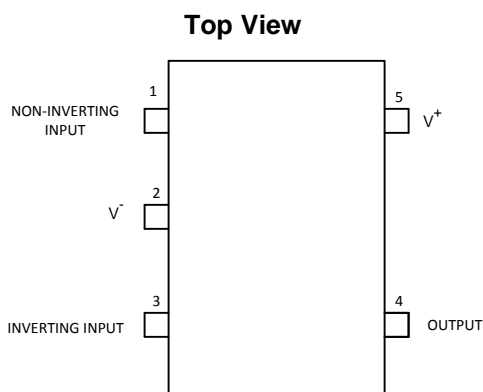
The IC's are built with Texas Instruments's advance Submicron Silicon-Gate BiCMOS process. The LMV7251/LMV7255 have bipolar inputs for improved noise performance and CMOS outputs for better rail-to-rail output performance.



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## Connection Diagram



**Figure 2.**



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### ABSOLUTE MAXIMUM RATINGS<sup>(1)(2)</sup>

ESD Tolerance		1 <sup>(3)</sup>
		200 <sup>(4)</sup>
$V_{IN}$ Differential		+/-Supply Voltage
Supply Voltage ( $V^+ - V^-$ )		5.5V
Voltage at Input/Output pins		$V^+ +0.1V, V^- -0.1V$
Soldering Information	Infrared or Convection (20 sec.)	235°C
	Wave Soldering (10 sec.)	260°C
Storage Temperature Range		-65°C to +150°C
Junction Temperature <sup>(5)</sup>		+150°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
- (3) Human body model, 1.5k $\Omega$  in series with 100pF.
- (4) Machine Model, 0 $\Omega$  in series with 200pF.
- (5) Typical values represent the most likely parametric norm.

### OPERATING RATINGS<sup>(1)</sup>

Supply Voltage $V^+$		1.8 to 5.0V
Junction Temperature Range <sup>(2)</sup>		-40 to +85°C
Package Thermal Resistance <sup>(2)</sup>	SOT-23-5	325°C/W
	SC-70	265°C/W

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
- (2) The maximum power dissipation is a function of  $T_{J(max)}$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{J(max)} - T_A)/\theta_{JA}$ . All numbers apply for packages soldered directly into a PC board.

## 1.8V ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 1.8\text{V}$ ,  $V^- = 0\text{V}$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ <sup>(1)</sup>	Limits <sup>(2)</sup>	Units
$V_{OS}$	Input Offset Voltage		0.3	<b>6</b> <b>8</b>	mV max
TC $V_{OS}$	Input Offset Average Drift	$V_{CM} = 0.9\text{V}$ <sup>(3)</sup>	10		$\mu\text{V}/\text{C}$
$I_B$	Input Bias Current		14		nA
$I_{OS}$	Input Offset Current		200		$\mu\text{A}$
$I_S$	Supply Current		11	<b>15</b> <b>17</b>	$\mu\text{A}$ max
$I_{SC}$	Output Short Circuit Current	Sourcing, $V_O = 0.9\text{V}$ (LMV7251 only)	8	4	mA min
		Sinking, $V_O = 0.9\text{V}$	11.6	5	
$I_{LEAKAGE}$	Output Leakage Current	$V_O = 1.8\text{V}$ (LMV7255 only)	300		$\mu\text{A}$
$V_{OH}$	Output Voltage High	$I_O = 1.5\text{mA}$ (LMV7251 only)	1.72	1.675	V min
$V_{OL}$	Output Voltage Low	$I_O = -1.5\text{mA}$	65	125	mV max
$V_{CM}$	Input Common Voltage Range	CMRR > 45 dB		1.9	V max
				-0.1	V min
CMRR	Common Mode Rejection Ratio	$0 < V_{CM} < 1.8\text{V}$	72	47	dB min
PSRR	Power Supply Rejection Ratio	$V^+ = 1.8\text{V}$ to 5V	79	55	dB min

(1) Typical values represent the most likely parametric norm.

(2) All limits are specified by testing or statistical analysis.

(3) Offset Voltage average drift determined by dividing the change in  $V_{OS}$  at temperature extremes into the total temperature change.

## 1.8V AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 1.8\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = 0.5\text{V}$ ,  $V_O = V^+/2$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ <sup>(1)</sup>	Limits <sup>(2)</sup>	Units
$t_{PHL}$	Propagation Delay (High to Low)	Input Overdrive = 20mV Load = 50pF//5k $\Omega$	720		ns
		Input Overdrive = 50mV Load = 50pF//5k $\Omega$	380		ns
$t_{PLH}$	Propagation Delay (Low to High)	Input Overdrive = 20mV Load = 50pF//5k $\Omega$	670		ns
		Input Overdrive = 50mV Load = 50pF//5k $\Omega$	400		ns

(1) All limits are specified by testing or statistical analysis.

(2) Machine Model, 0 $\Omega$  in series with 200pF.

## 2.7V ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 2.7\text{V}$ ,  $V^- = 0\text{V}$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ <sup>(1)</sup>	Limits <sup>(2)</sup>	Units
$V_{OS}$	Input Offset Voltage		0.03	<b>6</b> <b>8</b>	mV max
TC $V_{OS}$	Input Offset Average Drift	$V_{CM} = 1.35\text{V}^{(3)}$	10		$\mu\text{V}/\text{C}$
$I_B$	Input Bias Current		15		nA
$I_{OS}$	Input offset Current		210		pA
$I_S$	Supply Current		11	<b>18</b> <b>22</b>	$\mu\text{A}$ max
$I_{SC}$	Output Short Circuit Current	Sourcing, $V_O = 1.35\text{V}$ (LMV7251 only)	28	15	mA
		Sinking, $V_O = 1.35\text{V}$	28	15	
$I_{LEAKAGE}$	Output Leakage Current	$V_O = 2.7\text{V}$ , (LMV7255 only)	320		pA
$V_{OH}$	Output Voltage High	$I_O = 2\text{mA}$ (LMV7251 only)	2.63	2.575	V min
$V_{OL}$	Output Voltage Low	$I_O = -2\text{mA}$	61	125	mV max
$V_{CM}$	Input Common Voltage Range	CMRR > 45dB		2.8	V max
				-0.1	V min
CMRR	Common Mode Rejection Ratio	$0 < V_{CM} < 2.7\text{V}$	75	46	dB min
PSRR	Power Supply Rejection Ratio	$V^+ = 1.8\text{V}$ to 5V	79	55	dB min

(1) All limits are specified by testing or statistical analysis.

(2) Machine Model, 0 $\Omega$  in series with 200pF.

(3) Offset Voltage average drift determined by dividing the change in  $V_{OS}$  at temperature extremes into the total temperature change.

## 2.7V AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 2.7\text{V}$ ,  $V^- = 0\text{V}$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ <sup>(1)</sup>	Limits <sup>(2)</sup>	Units
$t_{PHL}$	Propagation Delay (High to Low)	Input Overdrive = 20mV Load = 50pF//5k $\Omega$	830		ns
		Input Overdrive = 50mV Load = 50pF//5k $\Omega$	430		ns
$t_{PLH}$	Propagation Delay (Low to High)	Input Overdrive = 20mV Load = 50pF//5k $\Omega$	730		ns
		Input Overdrive = 50mV Load = 50pF//5k $\Omega$	410		ns

(1) All limits are specified by testing or statistical analysis.

(2) Machine Model, 0 $\Omega$  in series with 200pF.

## 5V ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ ,  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ . **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ <sup>(1)</sup>	Limits <sup>(2)</sup>	Units
$V_{OS}$	Input Offset Voltage		0.03	<b>6</b> <b>8</b>	mV max
TC $V_{OS}$	Input Offset Average Drift	$V_{CM} = 2.5\text{V}^{(3)}$	10		$\mu\text{V}/\text{C}$
$I_B$	Input Bias Current		16		nA
$I_{OS}$	Input Offset Current		220		pA
$I_S$	Supply Current		12	<b>20</b> <b>25</b>	$\mu\text{A}$ max
$I_{SC}$	Output Short Circuit Current	Sourcing, $V_O = 2.5\text{V}$ (LMV7251 only)	82	50	mA min
		Sinking, $V_O = 2.5\text{V}$	78	50	
$I_{LEAKAGE}$	Output Leakage Current	$V_O = 5\text{V}$ , (LMV7255 only)	375		pA
$V_{OH}$	Output Voltage High	$I_O = 4\text{mA}$	4.9	4.82	V min
$V_{OL}$	Output Voltage Low	$I_O = -4\text{mA}$	90	180	mV max

(1) All limits are specified by testing or statistical analysis.

(2) Machine Model,  $0\Omega$  in series with 200pF.

(3) Offset Voltage average drift determined by dividing the change in  $V_{OS}$  at temperature extremes into the total temperature change.

### TYPICAL PERFORMANCE CHARACTERISTICS

( $T_A = 25^\circ\text{C}$ , Unless otherwise specified).

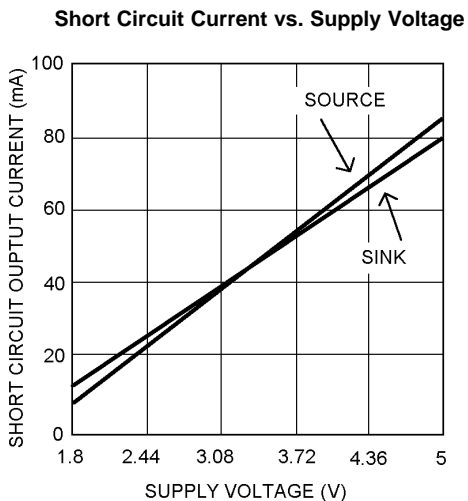


Figure 3.

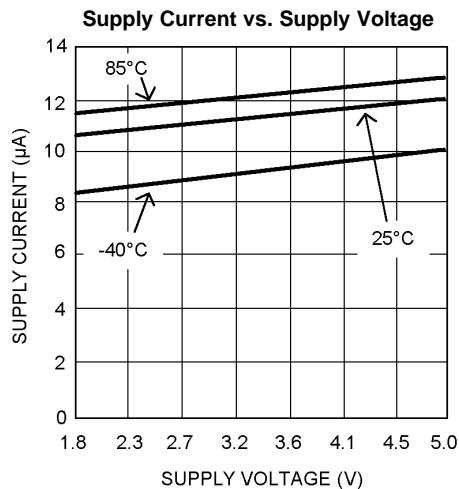


Figure 4.

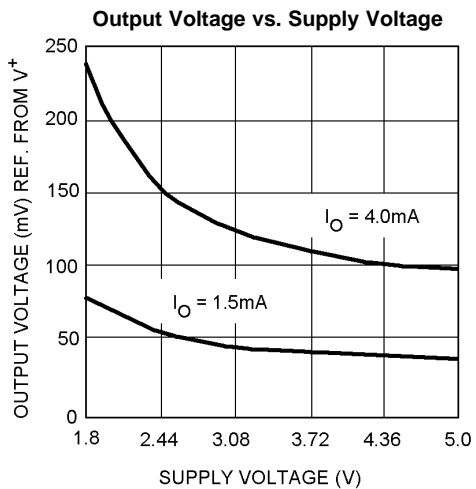


Figure 5.

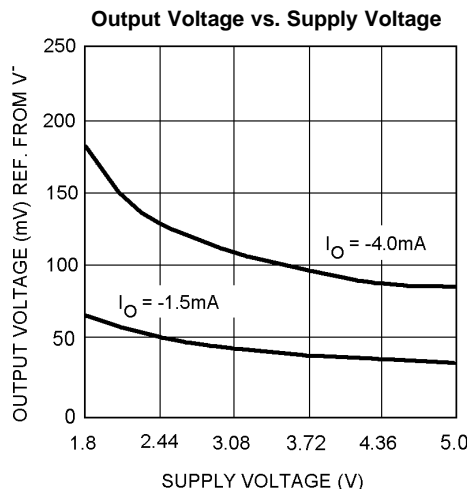


Figure 6.

**Output Voltage vs. Output Current @ 1.8V Supply Voltage**

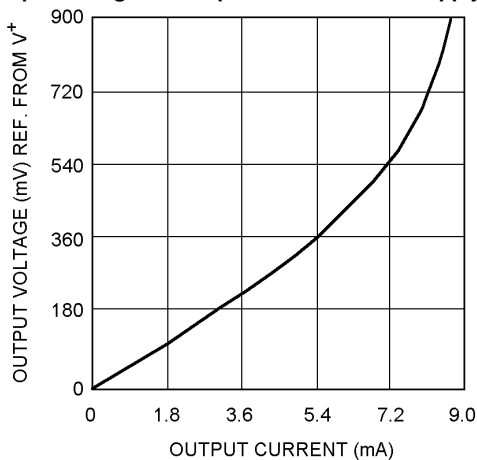


Figure 7.

**Output Voltage vs. Output Current @ 1.8V Supply Voltage**

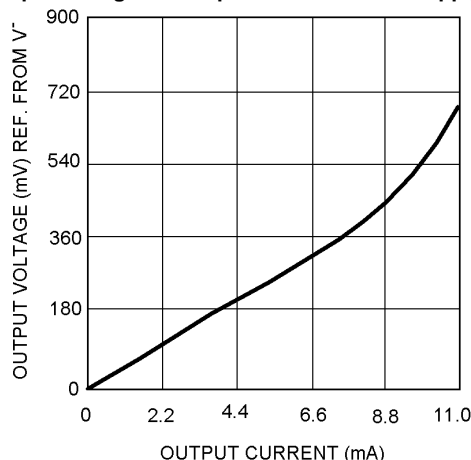
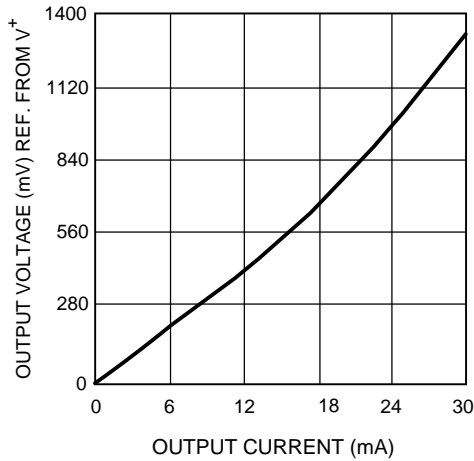


Figure 8.

**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

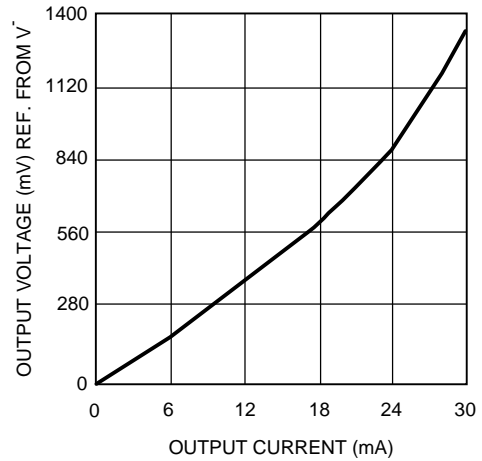
( $T_A = 25^\circ\text{C}$ , Unless otherwise specified).

**Output Voltage vs. Output Current @2.7V Supply Voltage**



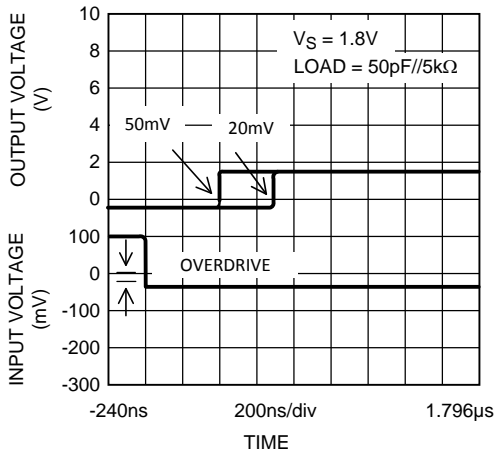
**Figure 9.**

**Output Voltage vs. Output Current @2.7V Supply Voltage**



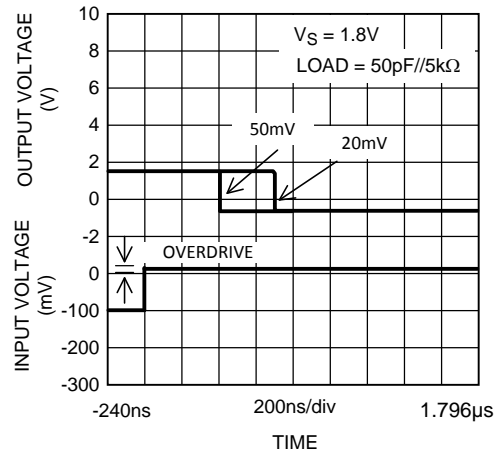
**Figure 10.**

**Response Time for Various Input Overdrives -  $t_{PLH}$**



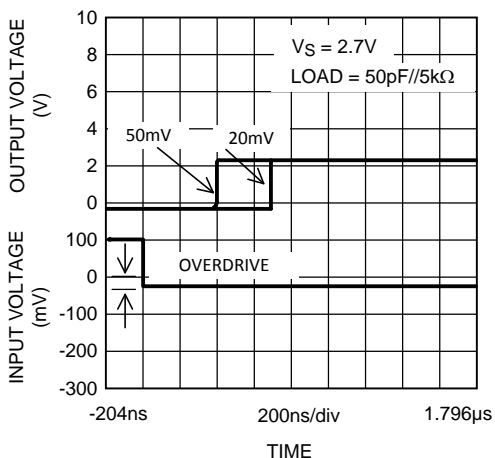
**Figure 11.**

**Response Time for Various Input Overdrives -  $t_{PHL}$**



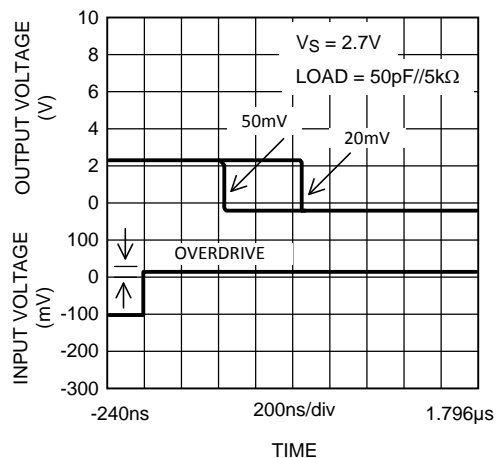
**Figure 12.**

**Response Time for Various Input Overdrives -  $t_{PLH}$**



**Figure 13.**

**Response Time for Various Input Overdrives -  $t_{PHL}$**



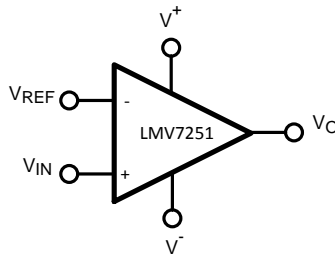
**Figure 14.**

## APPLICATION INFORMATION

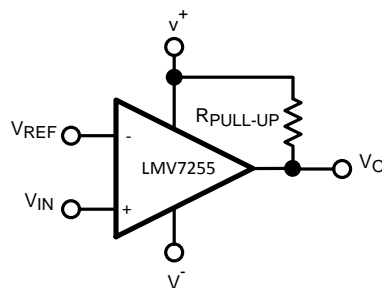
### BASIC COMPARATORS

A comparator is quite often used to convert an analog signal to a digital signal. The comparator compares an input voltage ( $V_{IN}$ ) at the non-inverting pin to the reference voltage ( $V_{REF}$ ) at the inverting pin. If  $V_{IN}$  is less than  $V_{REF}$  the output ( $V_O$ ) is low ( $V_{OL}$ ). However, if  $V_{IN}$  is greater than  $V_{REF}$ , the output voltage ( $V_O$ ) is high ( $V_{OH}$ ).

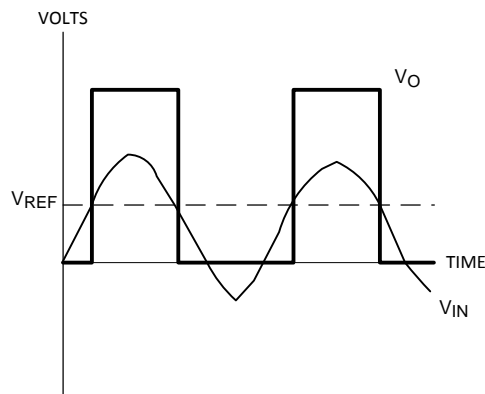
**LMV7251**



**LMV7255**



**Input/Output**



**Figure 15. Basic Comparator**

### HYSTERESIS

The basic comparator configuration may oscillate or produce a noisy output if the applied differential input is near the comparator's input offset voltage. This tends to occur when the voltage on the input is equal or very close to the other input voltage. Adding hysteresis can prevent this problem. Hysteresis creates two switching thresholds (one for the rising input voltage and the other for the falling input voltage). Hysteresis is the voltage difference between the two switching thresholds. When both inputs are nearly equal, hysteresis causes one input to effectively move quickly past the other. Thus, effectively moving the input out of region that oscillation may occur.



Hysteresis can easily be added to a comparator in a non-inverting configuration with two resistors and positive feedback **Figure 16**. The output will switch from low to high when  $V_{IN}$  rises up to  $V_{IN1}$ , where  $V_{IN1}$  is calculated by

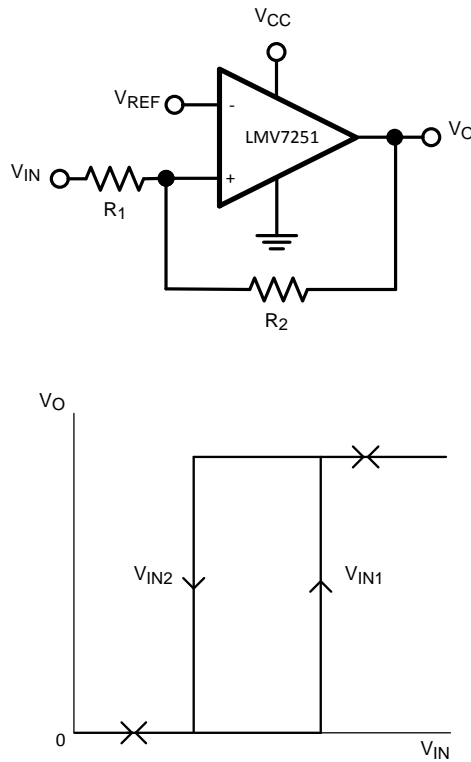
$$V_{IN1} = (V_{REF} (R1 + R2)) / R2 \quad (1)$$

The output will switch from high to low when  $V_{IN}$  falls to  $V_{IN2}$ , where  $V_{IN2}$  is calculated by

$$V_{IN2} = (V_{REF} (R1 + R2) - V_{CC} R1) / R2 \quad (2)$$

The Hysteresis is the difference between  $V_{IN1}$  and  $V_{IN2}$ .

$$\Delta V_{IN} = V_{IN1} - V_{IN2} = ((V_{REF} (R1 + R2)) / R2) - ((V_{REF} (R1 + R2) - V_{CC} R1) / R2) = V_{CC} R1 / R2. \quad (3)$$



**Figure 16. Non-Inverting Comparator Configuration — LMV7251**

For an inverting configured comparator, hysteresis can be added with a three resistor network and positive feedback. When input voltage ( $V_{IN}$ ) at the inverting node is less than non-inverting node ( $V_T$ ), the output is high. The equivalent circuit for the three resistor network is  $R1$  in parallel with  $R3$  and in series with  $R2$ . The lower threshold voltage  $V_{T1}$  is calculated by:

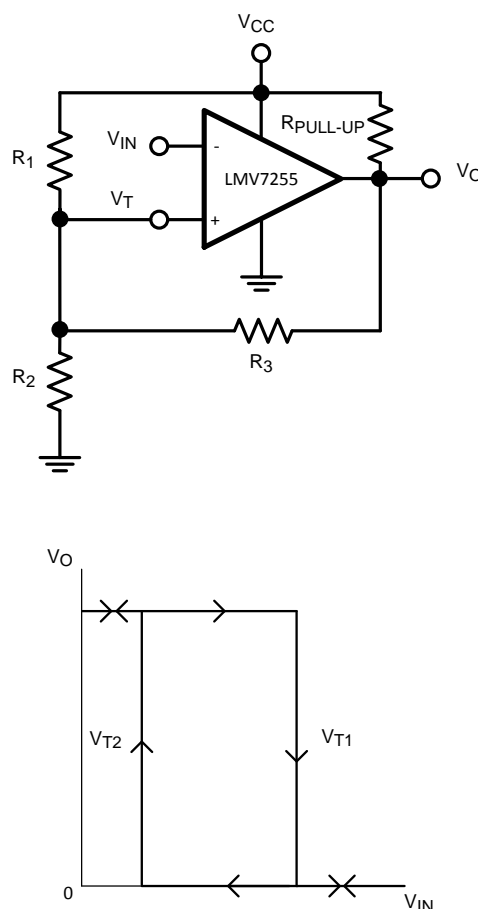
$$V_{T1} = ((V_{CC} R2) / ((R1 R3) / (R1 + R3)) + R2) \quad (4)$$

When  $V_{IN}$  is greater than  $V_T$ , the output voltage is low. The equivalent circuit for the three resistor network is  $R2$  in parallel with  $R3$  and in series with  $R1$ . The upper threshold voltage  $V_{T2}$  is calculated by:

$$V_{T2} = V_{CC} ((R2 R3) / (R2 + R3)) / ((R1 + ((R2 R3) / (R2 + R3))) \quad (5)$$

The hysteresis is defined as

$$\Delta V_{IN} = V_{T1} - V_{T2} = ((V_{CC} R2) / ((R1 R3) / (R1 + R3)) + R2) - (V_{CC} ((R2 R3) / (R2 + R3)) / ((R1 + ((R2 R3) / (R2 + R3)))) \quad (6)$$



**Figure 17. Inverting Configured Comparator — LMV7255**

## INPUT STAGE

The LMV7251 and LMV7255 have rail-to-rail input stages. The input common mode voltage range is from  $-100\text{mV}$  to  $(V_{CC} + 100\text{mV})$ .

## OUTPUT STAGE

The LMV7251 has a push-pull CMOS output stage. Large push-pull output drivers allows rail-to-rail output swings with load currents in the milliampere range.

The LMV7255 has a open drain CMOS output stage. This requires an external pull-up resistor connected between the positive supply voltage and the output. The external pull-up resistor should be high enough resistance so to avoid excessive power dissipation. In addition, the pull-up resistor should be low enough resistance to enable the comparator to switch with the load circuitry connected.

## POWER SUPPLY CONSIDERATIONS

The LMV7251/LMV7255 are well suited for many battery-powered applications. The LMV7251/LMV7255 can operate from single power supply of  $+1.8\text{V}$  to  $+5\text{V}$ . The device typically consumes only  $11\mu\text{A}$  with a  $2.7\text{V}$  supply. With a high power supply rejection ratio (PSRR) of  $79\text{ dB}$  (typical), the comparator is well suited for operating under conditions of a decaying battery voltage.

Power supply decoupling is critical and improves stability. Place decoupling capacitors  $0.1\mu\text{F}$  as close as possible to the  $V^+$  pin. For split supply applications, place decoupling capacitors  $0.1\mu\text{F}$  on both the  $V^+$  and  $V^-$  pins. The decoupling capacitors will help keep the comparator from oscillating under various load conditions.

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**REVISION HISTORY**

<b>Changes from Revision D (April 2013) to Revision E</b>	<b>Page</b>
<hr/> <ul style="list-style-type: none"><li>• Changed layout of National Data Sheet to TI format .....</li></ul>	<hr/> <a href="#">10</a>

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DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
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RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
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### Applications

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