LMS75ALS176A Differential Bus Transceivers

Check for Samples: LMS75ALS176A

FEATURES

- **Bidirectional Transceiver**
- **Meet ANSI Standard RS-485-A and RS-422-B**
- **Low Skew, 2ns**
- **Low Supply Current, 8mA (max.)**
- **Wide Input and Output Voltage Range**
- **High Output Drive Capacity ±60mA**
- **Thermal Shutdown Protection**
- **Open Circuit Fail-Safe for Receiver**
- **Receiver Input Sensitivity ±200mV**
- **Receiver Input Hysteresis 10mV (min.)**
- **Single Supply Voltage Operation, 5V**
- **Glitch Free Power-Up and Power-Down Operation**
- **Data Rates up to 35 Mbaud**
- **Pin and Functional Compatible with TI's SN75ALS176A**
- **8-Pin SOIC**

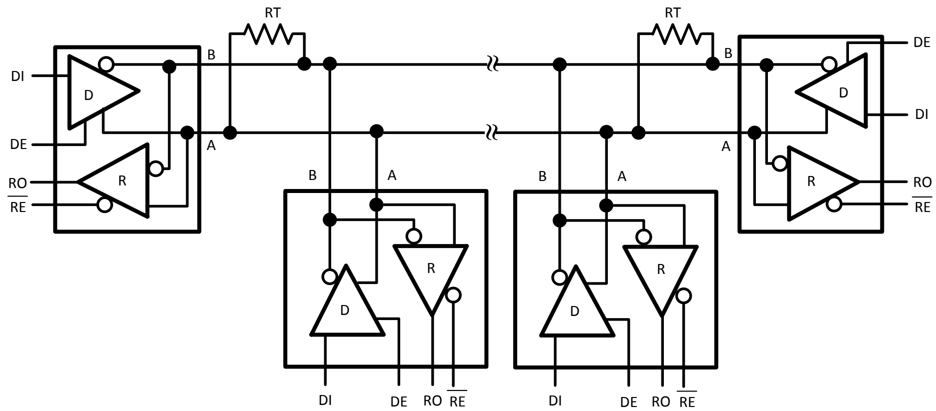
APPLICATIONS

- **Network Hubs, Bridges, and Routers**
- **Point of Sales Equipment (ATM, Barcode Readers,…)**
- **Industrial Programmable Logic Controllers**
- **High Speed Parallel and Serial Applications**
- **Multipoint Applications with Noisy Environment**

DESCRIPTION

The LMS75ALS176A is a differential bus/line transceiver designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines. It meets ANSI Standards TIA/EIA RS422-B, TIA/EIA RS485-A and ITU recommendation V.11 and X.27. The LMS75ALS176A combines a Tri-State differential line driver and differential input receiver, both of which operate from a single 5.0V power supply. The driver and receiver have an active high and active low enable, respectively, that can be externally connected to function as a direction control. The driver and receiver differential inputs are internally connected to form differential input/output (I/O) bus ports that are designed to offer minimum loading to bus whenever the driver is disabled or when V_{CC} = 0V. These ports feature wide positive and negative common mode voltage ranges, making the device suitable for multipoint applications in noisy environments. The LMS75ALS176A is available in a 8-Pin SOIC package. It is a drop-in socket replacement to TI's SN75ALS176A.

Typical Application



A Typical multipoint application is shown in the above figure. Terminating resistors, RT, are typically required but only located at the two ends of the cable. Pull up and pull down resistors maybe required at the end of the bus to provide failsafe biasing. The biasing resistors provide a bias to the cable when all drivers are in Tri-State, See Texas Instruments Application Note, SNLA031 for further information.

Connection Diagram

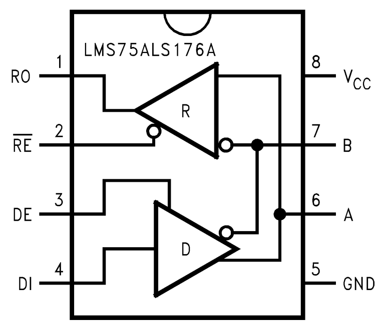


Figure 1. 8-Pin SOIC (Top View)
See D Package

TRUTH TABLE(1)

DRIVER SECTION				
RE	**DE**	**DI**	**A**	**B**
X	H	H	H	L
X	H	L	L	H
X	L	X	Z	Z
RECEIVER SECTION				
RE	**DE**	**A-B**		**RO**
L	L	≥ +0.2V		H
L	L	≤ −0.2V		L
H	X	X		Z
L	L	OPEN *		H

(1) * = Non Terminated, Open Input only
X = Irrelevant
Z = Tri-State
H = High level
L = Low level

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS[1][2]

Supply Voltage, V_{CC} [3]		7V
Voltage Range at Any Bus Terminal		−7V to 12V
Input Voltage, V_{IN} (DI, DE, or $\overline{RE}$)		−0.3V to V_{CC} + 0.3V
Package Thermal Impedance, θ_{JA}		125C/W
Junction Temperature[4]		150°C
Operating Free-Air Temperature Range, T_A		0°C to 70°C
Storage Temperature Range		−65°C to 150°C
Soldering Information	Infrared or Convection (20 sec.)	235°C
ESD Rating[5]		2KV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the ELECTRICAL CHARACTERISTICS section.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.
(5) ESD rating based upon human body model, 100pF discharged through 1.5kΩ.

OPERATING RATINGS

		Min	Nom	Max	
Supply Voltage, V_{CC}		4.75	5.0	5.25	V
Voltage at any Bus Terminal (Separately or Common Mode)				12	V
V_{IN} or V_{IC}				−7	
High-Level Input Voltage, V_{IH} [1]		2			V
Low-Level Input Voltage, V_{IL} [1]				0.8	V
Differential Input Voltage, V_{ID} [2]				±12	V
High-Level Output	Driver, I_{OH}			−60	mA
	Receiver, I_{OH}			−400	µA
Low-Level Output	Driver, I_{OL}			60	mA
	Receiver, I_{OL}			8	mA

(1) Voltage limits apply to DI, DE, $\overline{RE}$ pins.
(2) Differential input/output bus voltage is measured at the non-inverting terminal A with respect to the inverting terminal B.

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, T_A = 0°C to 70°C

Symbol	Parameter	Conditions		Min	Typ	Max	Units
Driver Section							
V_{CL}	Input Clamp Voltage	I_I = −18mA				−1.5	V
V_O	Output Voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential Output Voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential Output Voltage	R_L = 100Ω,		2			V
		R_L = 54Ω		1.5	1.9	5	
V_{OD3}	Differential Output Voltage	V_{TEST} = −7V to 12 V		1.5		5	V
ΔV_{OD}	Change in Magnitude of Differential Output Voltage (1)	R_L = 54Ω or 100Ω				±0.2	V
V_{OC}	Common-Mode Output Voltage	R_L = 54Ω or 100Ω				3	V
						−1	
ΔV_{OC}	Change in Magnitude of Differential Output Voltage (1)	R_L = 54Ω or 100Ω				±0.2	V
I_O	Output Current	Output Disabled (2)	V_O = 12V			1	mA
			V_O = −7V			−0.8	
I_{IH}	High-Level Input Current	V_{IN} = 2.4V				20	μA
I_{IL}	Low-Level Input Current	V_{IN} = 0.4V				−400	μA
I_{OSD}	Short-Circuit Output Current	V_O = −7V				−250	mA
		V_O = 0				−150	
		V_O = V_{CC}				250	
		V_O = 8V				250	
I_{CC}	Supply Current	No Load	Outputs Enabled or Disabled		4.8	8	mA
Switching Characteristics							
t_d (OD)	Differential Output Delay Time	R_L = 54Ω , C_L = 50pF		3	7	14	ns
t_t (OD)	Differential Output Transition Time	R_L = 54Ω, C_L = 50pF			8		ns
$t_{sk(p)}$	Pulse Skew, ($\|t_{d(ODH} - t_{d(ODL}\|$)	R_L = 54Ω, C_L = 50pF			0	3	ns
$t_{sk(lim)}$	Pulse Skew	R_L = 54Ω, C_L = 50pF (3)			4		ns
t_{PZH}	Output Enable Time to High Level	R_L = 110Ω, C_L = 50pF			18	50	ns
t_{PZL}	Output Enable Time to Low Level	R_L = 110Ω, C_L = 50pF			18	35	ns
t_{PHZ}	Output Disable Time from High Level	R_L = 110Ω, C_L = 50pF			9	35	ns
t_{PLZ}	Output Disable Time from Low Level	R_L = 110Ω, C_L = 50pF			10	17	ns
Receiver Section							
V_{TH+}	Positive-Going Input Threshold Voltage	V_O = 2.7V, I_O = −0.4mA				0.2	V
V_{TH-}	Negative-Going Input Threshold Voltage	V_O = 0.5V, I_O = 8mA		−0.2			V
ΔV_{TH}	Hysteresis Voltage (V_{TH+} - V_{TH-})			10			mV
V_{CL}	Enable-Input Clamp Voltage	I_I = −18mA				1.5	V

(1) $|\Delta V_{OD}|$ and $|\Delta V_{OC}|$ are changes in magnitude of V_{OD} and V_{OC}, respectively when the input changes from high to low levels.
(2) Applies to both power on and off (ANSI Standard RS-485 conditions). Does not apply to TIA/EIA-422-B for a combined driver and receiver combination.
(3) Skew limit is the maximum difference in propagation delay between any two channels of any two devices.

ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 5V, T_A = 0°C to 70°C

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OH}	High-Level Output Voltage	V_{ID} = 200mV, I_{OH} = −400µA		2.7			V
V_{OL}	Low-Level Output Voltage	V_{ID} = −200mV, I_{OL} = 8mA				0.45	V
I_{OZ}	High-Impedance-State Output Current	V_O = 0.4V to 2.4V				±20	µA
I_{IN}	Line Input Current	Other Input = 0V,(4)	V_{IN} = 12V			1	mA
			V_{IN} = −7V			−0.8	
I_{IH}	High-Level Enable-Input Current	V_{IH} = 2.7V				20	µA
I_{IL}	Low-Level Enable-Input Current	V_{IL} = 0.4V				−100	µA
R_{IN}	Input Resistance			12	20		kΩ
I_{OSR}	Short-Circuit Output Current	V_{ID} = 200mV, V_O = 0V		−15		−85	mA
I_{CC}	Supply Current	No Load	Outputs Enabled or Disabled		4.8	8	mA
Switching Characteristics							
t_{PD}	Propagation Delay Time	V_{ID} = −1.5V to 1.5V, C_L = 15pF		8	18	30	ns
$t_{sk(p)}$	Pulse Skew ($\|t_{PLH}$ - $t_{PHL}\|$)	V_{ID} = −1.5V to 1.5V, C_L = 15pF			2		ns
$t_{sk(lim)}$	Pulse Skew	R_L = 54Ω , C_L = 50pF(5)			7.5		ns
t_{PZH}	Output Enable Time to High Level	C_L = 15pF			5	35	ns
t_{PZL}	Output Enable Time to Low Level	C_L = 15pF			5	35	ns
t_{PHZ}	Output Disable Time from High Level	C_L = 15pF			20	35	ns
t_{PLZ}	Output Disable Time from Low Level	C_L = 15pF			10	17	ns

(4) Voltage limits apply to DI, DE, $\overline{RE}$ pins.
(5) Skew limit is the maximum difference in propagation delay between any two channels of any two devices.

TYPICAL PERFORMANCE CHARACTERISTICS

Driver High-Level Output Voltage vs. High-Level Output Current

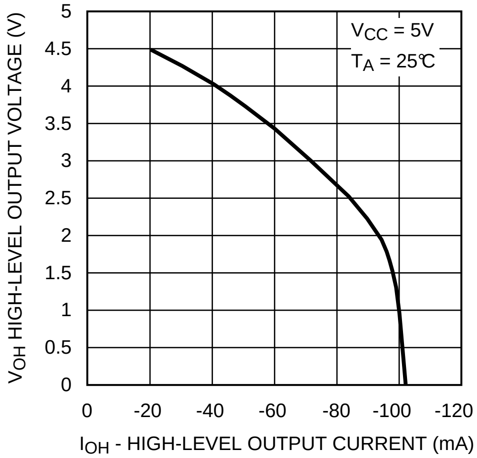


Figure 2.

Driver Low-Level Output Voltage vs. Low-Level Output Current

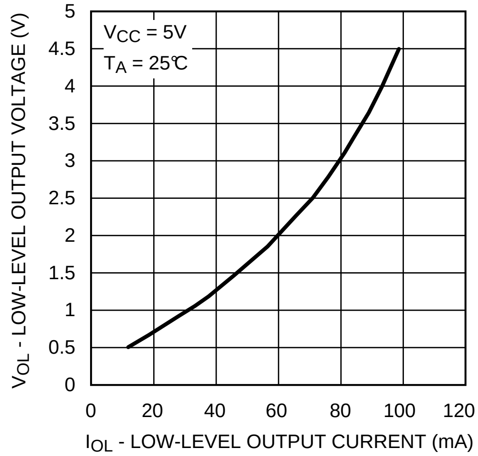


Figure 3.

Driver Differential Output Voltage vs. Output Current

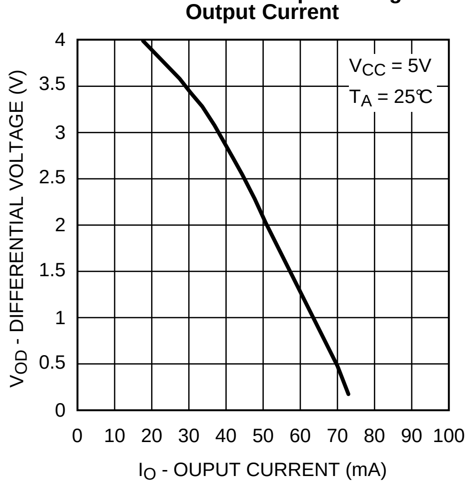


Figure 4.

Receiver High-Level Output Voltage vs. High-Level Output Current

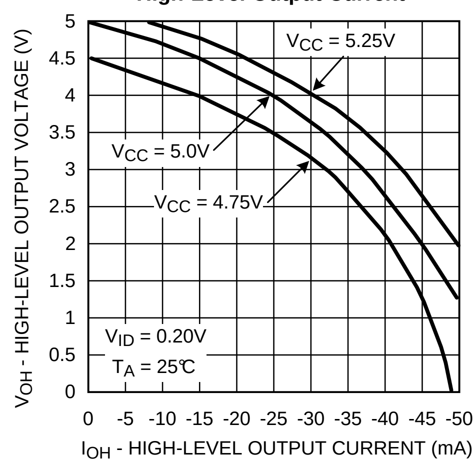


Figure 5.

Receiver High-Level Output Voltage vs. Free-Air Temperature

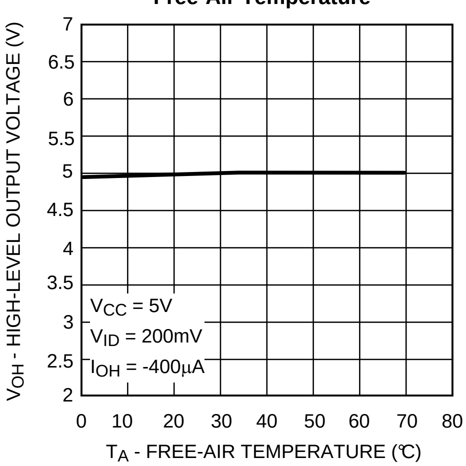


Figure 6.

Receiver Low-Level Output Voltage vs. Low-Level Output Current

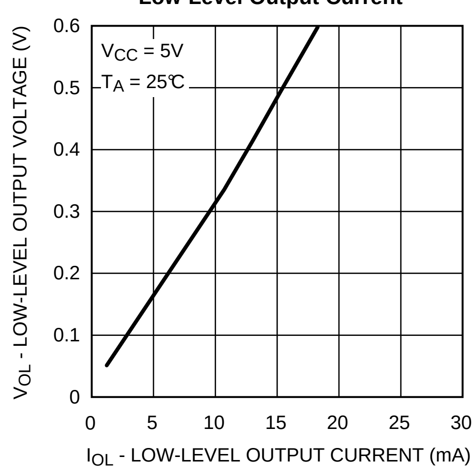


Figure 7.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Receiver Low-Level Output Voltage vs. Free-Air Temperature

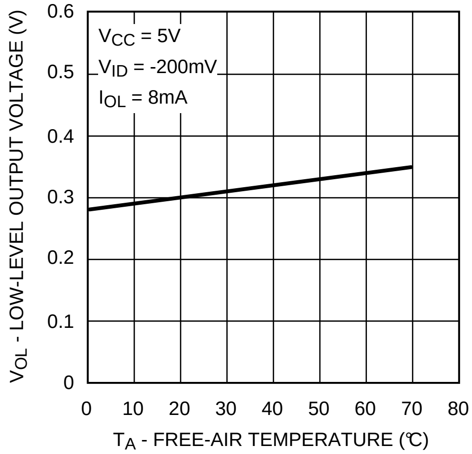


Figure 8.

Receiver Output Voltage vs. Enable Voltage

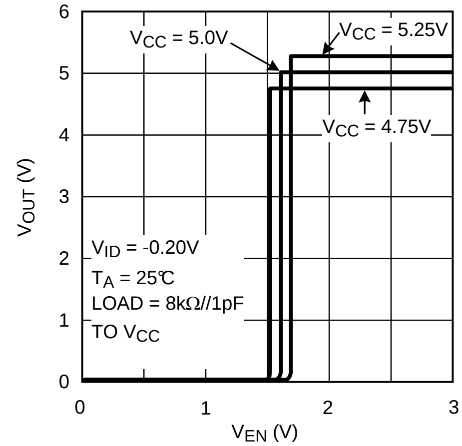


Figure 9.

Receiver Output Voltage vs. Enable Voltage

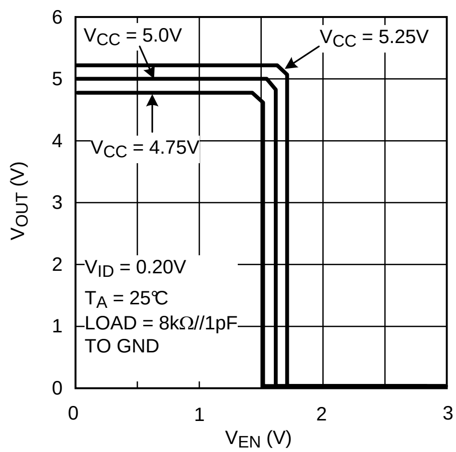


Figure 10.

PARAMETER MEASURING INFORMATION

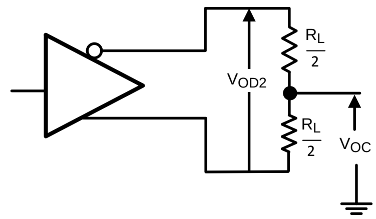


Figure 11. Test Circuit for V_{OD2} and V_{OC}

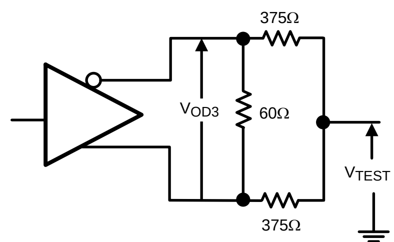


Figure 12. Test Circuit for V_{OD3}

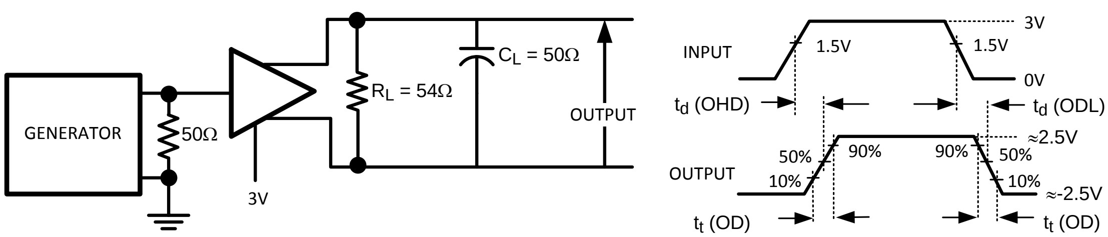


Figure 13. Test Circuit for Driver Differential Output Delay and Transition Times

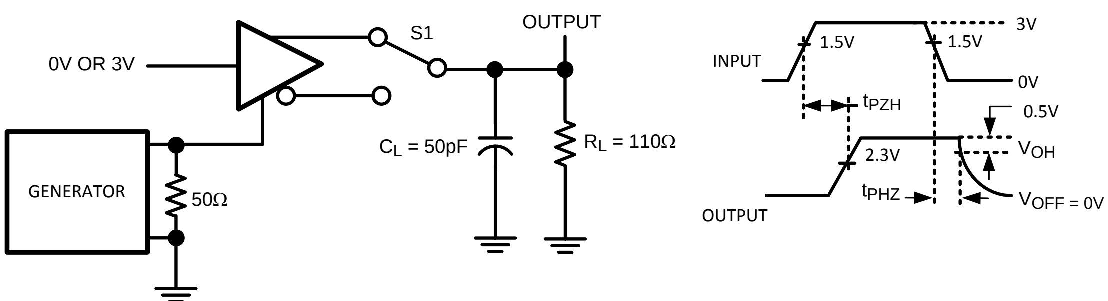


Figure 14. Test Circuit for Driver T_{PZH} and T_{PHZ}

PARAMETER MEASURING INFORMATION (continued)

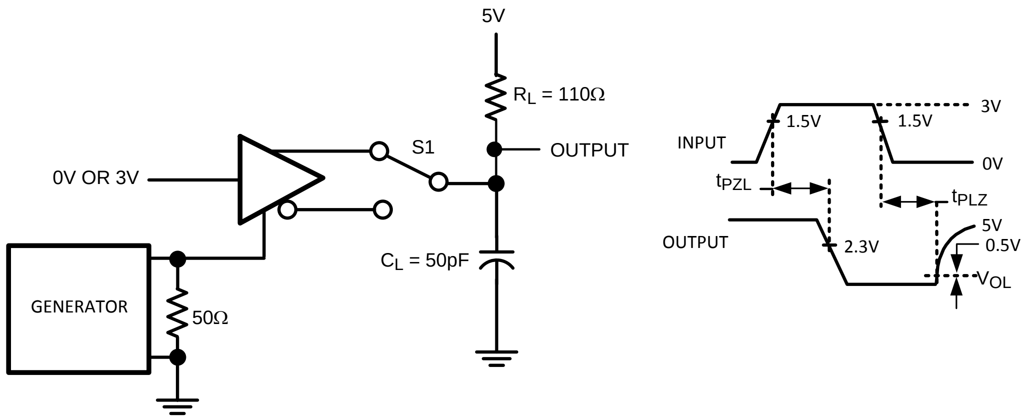


Figure 15. Test Circuit for T_{PZL} and T_{PLZ}

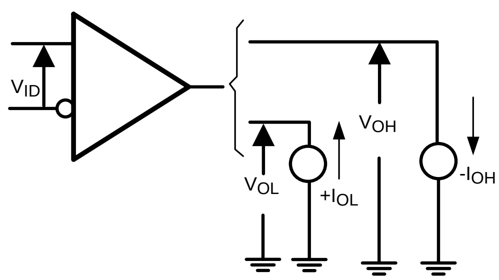


Figure 16. Test Circuit for Receiver V_{OH} and V_{OL}

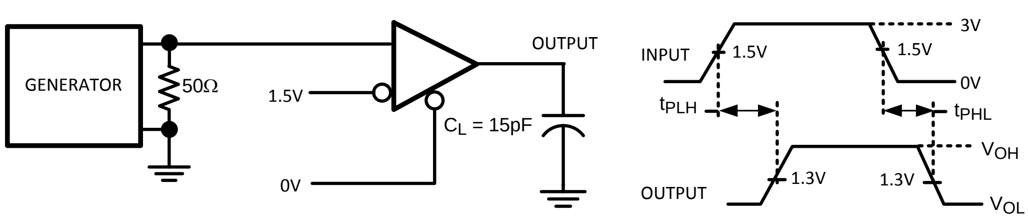
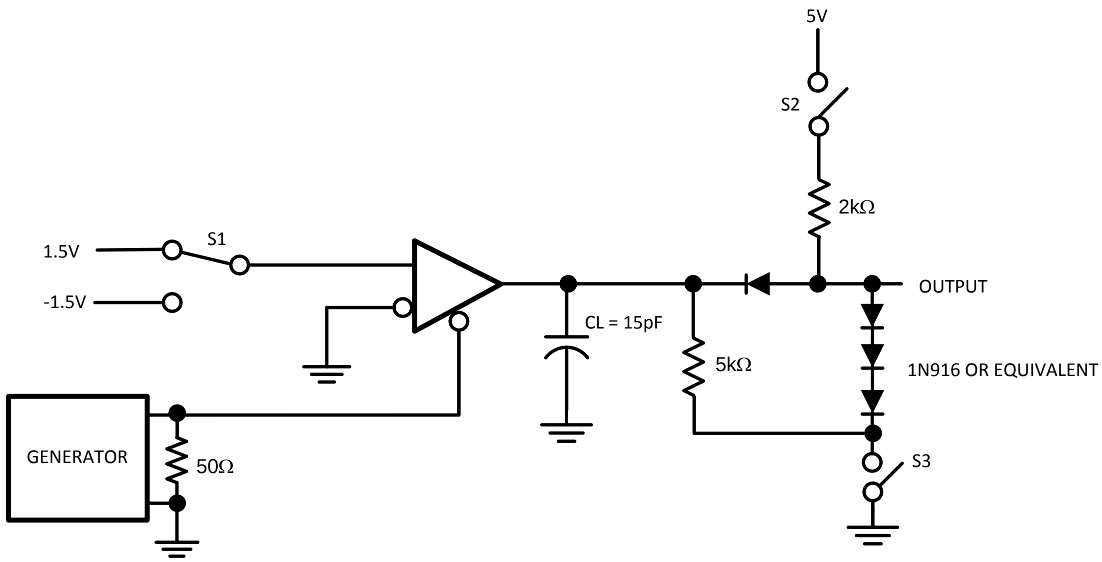


Figure 17. Test Circuit for T_{PLH} and T_{PHL}

PARAMETER MEASURING INFORMATION (continued)

Test Circuit



Voltage Waveforms

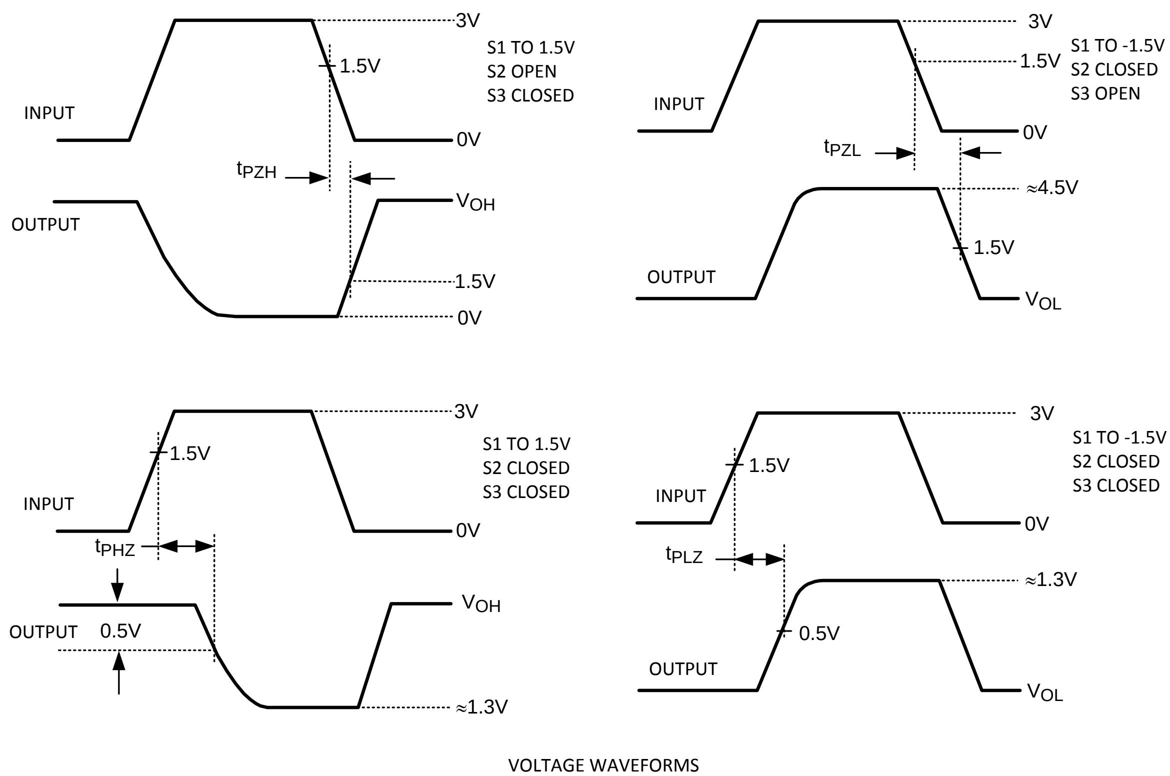


Figure 18. Test Circuit for Receiver T_{PZH}/ T_{PZL} and T_{PHZ}/T_{PLZ}

APPLICATION INFORMATION

Power Line Noise Filtering

A factor to consider in designing power and ground is noise filtering. A noise filtering circuit is designed to prevent noise generated by the integrated circuit (IC) as well as noise entering the IC from other devices. A common filtering method is to place by-pass capacitors (C_{bp}) between the power and ground lines.

Placing a by-pass capacitor (C_{bp}) with the correct value at the proper location solves many power supply noise problems. Choosing the correct capacitor value is based upon the desired noise filtering range. Since capacitors are not ideal, they may act more like inductors or resistors over a specific frequency range. Thus, many times two by-pass capacitors may be used to filter a wider bandwidth of noise. It is highly recommended to place a larger capacitor, such as 10µF, between the power supply pin and ground to filter out low frequencies and a 0.1µF to filter out high frequencies.

By pass-capacitors must be mounted as close as possible to the IC to be effective. Long leads produce higher impedance at higher frequencies due to stray inductance. Thus, this will reduce the by-pass capacitor's effectiveness. Surface mounted chip capacitors are the best solution because they have lower inductance.

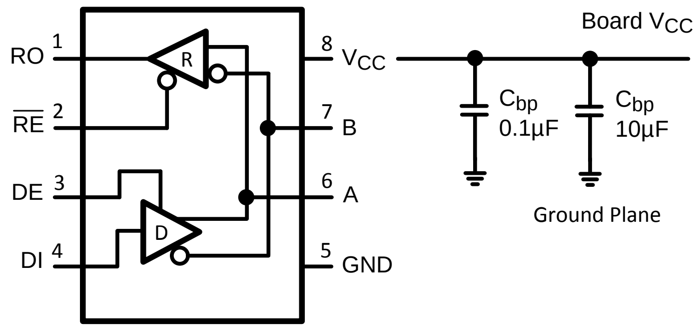


Figure 19. Placement of By-Pass Capacitors, C_{bp}

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C **Page**

- Changed layout of National Data Sheet to TI format 11

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