LMH6624/LMH6626 Single/Dual Ultra Low Noise Wideband Operational Amplifier

Check for Samples: LMH6624

FEATURES

- **V_S = ±6V, T_A = 25°C, A_V = 20, (Typical values unless specified)**
- **Gain Bandwidth (LMH6624) 1.5GHz**
- **Input Voltage Noise 0.92nV/√Hz**
- **Input Offset Voltage (limit over temp) 700µV**
- **Slew Rate 350V/µs**
- **Slew Rate (A_V = 10) 400V/µs**
- **HD2 @ f = 10MHz, R_L = 100Ω −63dBc**
- **HD3 @ f = 10MHz, R_L = 100Ω −80dBc**
- **Supply Voltage Range (dual supply) ±2.5V to ±6V**
- **Supply Voltage Range (single supply) +5V to +12V**
- **Improved Replacement for the CLC425 (LMH6624)**
- **Stable for Closed Loop $|A_V| \geq 10$**

APPLICATIONS

- **Instrumentation Sense Amplifiers**
- **Ultrasound Pre-amps**
- **Magnetic Tape & Disk Pre-amps**
- **Wide band active filters**
- **Professional Audio Systems**
- **Opto-electronics**
- **Medical Diagnostic Systems**

DESCRIPTION

The LMH6624/LMH6626 offer wide bandwidth (1.5GHz for single, 1.3GHz for dual) with very low input noise (0.92nV/√Hz, 2.3pA/√Hz) and ultra low dc errors (100µV V_{OS}, ±0.1µV/°C drift) providing very precise operational amplifiers with wide dynamic range. This enables the user to achieve closed-loop gains of greater than 10, in both inverting and non-inverting configurations.

The LMH6624 (single) and LMH6626's (dual) traditional voltage feedback topology provide the following benefits: balanced inputs, low offset voltage and offset current, very low offset drift, 81dB open loop gain, 95dB common mode rejection ratio, and 88dB power supply rejection ratio.

The LMH6624/LMH6626 operate from ± 2.5V to ± 6V in dual supply mode and from +5V to +12V in single supply configuration.

LMH6624 is offered in SOT-23-5 and SOIC-8 packages.

The LMH6626 is offered in SOIC-8 and VSSOP-8 packages.

Connection Diagram

LMH6624 5-Pin SOT-23

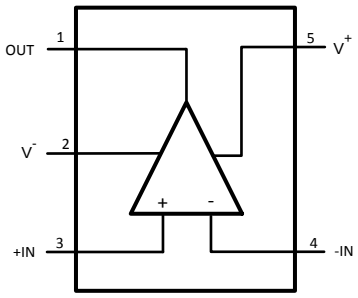


Figure 1. Top View

LMH6624 8-Pin SOIC

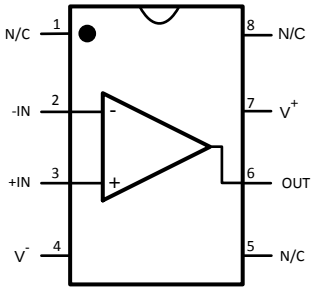


Figure 2. Top View

LMH6626 8-Pin SOIC/VSSOP

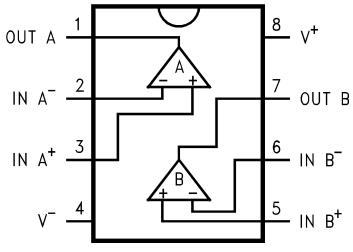


Figure 3. Top View

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

ESD Tolerance	
Human Body Model	2000V (2)
Machine Model	200V (3)
V_{IN} Differential	±1.2V
Supply Voltage (V^+ - V^-)	13.2V
Voltage at Input pins	V^+ +0.5V, V^- −0.5V
Soldering Information	
Infrared or Convection (20 sec.)	235°C
Wave Soldering (10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (4), (5)	+150°C

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) Human body model, 1.5kΩ in series with 100pF.
(3) Machine Model, 0Ω in series with 200pF.
(4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(5) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings (1)

Operating Temperature Range (2), (3)	−40°C to +125°C
Package Thermal Resistance (θ_{JA})(3)	
SOIC-8	166°C/W
SOT23–5	265°C/W
VSSOP-8	235°C/W

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

±2.5V Electrical Characteristics

Unless otherwise specified, all limits ensured at T_A = 25°C, V^+ = 2.5V, V^- = −2.5V, V_{CM} = 0V, A_V = +20, R_F = 500Ω, R_L = 100Ω. **Boldface** limits apply at the temperature extremes. See (1).

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
Dynamic Performance						
f_{CL}	−3dB BW	V_O = 400mV$_{PP}$ (LMH6624)		90		MHz
		V_O = 400mV$_{PP}$ (LMH6626)		80		
SR	Slew Rate (4)	V_O = 2V$_{PP}$, A_V = +20 (LMH6624)		300		V/µs
		V_O = 2V$_{PP}$, A_V = +20 (LMH6626)		290		
		V_O = 2V$_{PP}$, A_V = +10 (LMH6624)		360		
		V_O = 2V$_{PP}$, A_V = +10 (LMH6626)		340		
t_r	Rise Time	V_O = 400mV Step, 10% to 90%		4.1		ns
t_f	Fall Time	V_O = 400mV Step, 10% to 90%		4.1		ns
t_s	Settling Time 0.1%	V_O = 2V$_{PP}$ (Step)		20		ns
Distortion and Noise Response						
e_n	Input Referred Voltage Noise	f = 1MHz (LMH6624)		0.92		nV/√Hz
		f = 1MHz (LMH6626)		1.0		
i_n	Input Referred Current Noise	f = 1MHz (LMH6624)		2.3		pA/√Hz
		f = 1MHz (LMH6626)		1.8		
HD2	2nd Harmonic Distortion	f_C = 10MHz, V_O = 1V$_{PP}$, R_L 100Ω		−60		dBc
HD3	3rd Harmonic Distortion	f_C = 10MHz, V_O = 1V$_{PP}$, R_L 100Ω		−76		dBc
Input Characteristics						
V_{OS}	Input Offset Voltage	V_{CM} = 0V	−0.75 **−0.95**	−0.25	+0.75 **+0.95**	mV
	Average Drift (5)	V_{CM} = 0V		±0.25		µV/°C
I_{OS}	Input Offset Current	V_{CM} = 0V	−1.5 **−2.0**	−0.05	+1.5 **+2.0**	µA
	Average Drift (5)	V_{CM} = 0V		2		nA/°C
I_B	Input Bias Current	V_{CM} = 0V		13	+20 **+25**	µA
	Average Drift (5)	V_{CM} = 0V		12		nA/°C
R_{IN}	Input Resistance (6)	Common Mode		6.6		MΩ
		Differential Mode		4.6		kΩ
C_{IN}	Input Capacitance (6)	Common Mode		0.9		pF
		Differential Mode		2.0		
CMRR	Common Mode Rejection Ratio	Input Referred,				dB
		V_{CM} = −0.5 to +1.9V **V_{CM} = −0.5 to +1.75V**	87 **85**	90		
Transfer Characteristics						
A_{VOL}	Large Signal Voltage Gain	(LMH6624) R_L = 100Ω, V_O = −1V to +1V	75 **70**	79		dB
		(LMH6626) R_L = 100Ω, V_O = −1V to +1V	72 **67**	79		
X_t	Crosstalk Rejection	f = 1MHz (LMH6626)		−75		dB

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. Absolute maximum ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing or statistical analysis.
(3) Typical Values represent the most likely parametric norm.
(4) Slew rate is the slowest of the rising and falling slew rates.
(5) Average drift is determined by dividing the change in parameter at temperature extremes into the total temperature change.
(6) Simulation results.

±2.5V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured at T_A = 25°C, V^+ = 2.5V, V^- = −2.5V, V_{CM} = 0V, A_V = +20, R_F = 500Ω, R_L = 100Ω. **Boldface** limits apply at the temperature extremes. See (1).

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
Output Characteristics						
V_O	Output Swing	R_L = 100Ω	±1.1 **±1.0**	±1.5		V
		No Load	±1.4 **±1.25**	±1.7		
R_O	Output Impedance	f ≤ 100KHz		10		mΩ
I_{SC}	Output Short Circuit Current	(LMH6624) Sourcing to Ground ΔV_{IN} = 200mV (7), (8)	90 **75**	145		mA
		(LMH6624) Sinking to Ground ΔV_{IN} = −200mV (7), (8)	90 **75**	145		
		(LMH6626) Sourcing to Ground ΔV_{IN} = 200mV (7),(8)	60 **50**	120		
		(LMH6626) Sinking to Ground ΔV_{IN} = −200mV (7),(8)	60 **50**	120		
I_{OUT}	Output Current	(LMH6624) Sourcing, V_O = +0.8V Sinking, V_O = −0.8V		100		mA
		(LMH6626) Sourcing, V_O = +0.8V Sinking, V_O = −0.8V		75		
Power Supply						
PSRR	Power Supply Rejection Ratio	V_S = ±2.0V to ±3.0V	82 **80**	90		dB
I_S	Supply Current (per channel)	No Load		11.4	16 **18**	mA

(7) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

(8) Short circuit test is a momentary test. Output short circuit duration is 1.5ms.

±6V Electrical Characteristics

Unless otherwise specified, all limits ensured at T_A = 25°C, V^+ = 6V, V^- = −6V, V_{CM} = 0V, A_V = +20, R_F = 500Ω, R_L = 100Ω. **Boldface** limits apply at the temperature extremes. See (1).

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
Dynamic Performance						
f_{CL}	−3dB BW	V_O = 400mV$_{PP}$ (LMH6624)		95		MHz
		V_O = 400mV$_{PP}$ (LMH6626)		85		
SR	Slew Rate (4)	V_O = 2V$_{PP}$, A_V = +20 (LMH6624)		350		V/µs
		V_O = 2V$_{PP}$, A_V = +20 (LMH6626)		320		
		V_O = 2V$_{PP}$, A_V = +10 (LMH6624)		400		
		V_O = 2V$_{PP}$, A_V = +10 (LMH6626)		360		
t_r	Rise Time	V_O = 400mV Step, 10% to 90%		3.7		ns
t_f	Fall Time	V_O = 400mV Step, 10% to 90%		3.7		ns
t_s	Settling Time 0.1%	V_O = 2V$_{PP}$ (Step)		18		ns
Distortion and Noise Response						
e_n	Input Referred Voltage Noise	f = 1MHz (LMH6624)		0.92		nV/√Hz
		f = 1MHz (LMH6626)		1.0		
i_n	Input Referred Current Noise	f = 1MHz (LMH6624)		2.3		pA/√Hz
		f = 1MHz (LMH6626)		1.8		
HD2	2nd Harmonic Distortion	f_C = 10MHz, V_O = 1V$_{PP}$, R_L 100Ω		−63		dBc
HD3	3rd Harmonic Distortion	f_C = 10MHz, V_O = 1V$_{PP}$, R_L 100Ω		−80		dBc
Input Characteristics						
V_{OS}	Input Offset Voltage	V_{CM} = 0V	−0.5 **−0.7**	±0.10	+0.5 **+0.7**	mV
	Average Drift (5)	V_{CM} = 0V		±0.2		µV/°C
I_{OS}	Input Offset Current Average Drift (5)	(LMH6624) V_{CM} = 0V	−1.1 **−2.5**	0.05	1.1 **2.5**	µA
		(LMH6626) V_{CM} = 0V	−2.0 **−2.5**	0.1	2.0 **2.5**	
		V_{CM} = 0V		0.7		nA/°C
I_B	Input Bias Current	V_{CM} = 0V		13	+20 **+25**	µA
	Average Drift (5)	V_{CM} = 0V		12		nA/°C
R_{IN}	Input Resistance (6)	Common Mode		6.6		MΩ
		Differential Mode		4.6		kΩ
C_{IN}	Input Capacitance (6)	Common Mode		0.9		pF
		Differential Mode		2.0		
CMRR	Common Mode Rejection Ratio	Input Referred,				dB
		V_{CM} = −4.5 to +5.25V **V_{CM} = −4.5 to +5.0V**	90 **87**	95		
Transfer Characteristics						
A_{VOL}	Large Signal Voltage Gain	(LMH6624) R_L = 100Ω, V_O = −3V to +3V	77 **72**	81		dB
		(LMH6626) R_L = 100Ω, V_O = −3V to +3V	74 **70**	80		

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No ensured specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. Absolute maximum ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing or statistical analysis.
(3) Typical Values represent the most likely parametric norm.
(4) Slew rate is the slowest of the rising and falling slew rates.
(5) Average drift is determined by dividing the change in parameter at temperature extremes into the total temperature change.
(6) Simulation results.

±6V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured at T_A = 25°C, V^+ = 6V, V^- = −6V, V_{CM} = 0V, A_V = +20, R_F = 500Ω, R_L = 100Ω. **Boldface** limits apply at the temperature extremes. See (1).

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
X_t	Crosstalk Rejection	f = 1MHz (LMH6626)		−75		dB
Output Characteristics						
V_O	Output Swing	(LMH6624) R_L = 100Ω	±4.4 **±4.3**	±4.9		V
		(LMH6624) No Load	±4.8 **±4.65**	±5.2		
		(LMH6626) R_L = 100Ω	±4.3 **±4.2**	±4.8		
		(LMH6626) No Load	±4.8 **±4.65**	±5.2		
R_O	Output Impedance	f ≤ 100KHz		10		mΩ
I_{SC}	Output Short Circuit Current	(LMH6624) Sourcing to Ground ΔV_{IN} = 200mV (7), (8)	100 **85**	156		mA
		(LMH6624) Sinking to Ground ΔV_{IN} = −200mV (7), (8)	100 **85**	156		
		(LMH6626) Sourcing to Ground ΔV_{IN} = 200mV (7), (8)	65 **55**	120		
		(LMH6626) Sinking to Ground ΔV_{IN} = −200mV (7), (8)	65 **55**	120		
I_{OUT}	Output Current	(LMH6624) Sourcing, V_O = +4.3V Sinking, V_O = −4.3V		100		mA
		(LMH6626) Sourcing, V_O = +4.3V Sinking, V_O = −4.3V		80		
Power Supply						
PSRR	Power Supply Rejection Ratio	V_S = ±5.4V to ±6.6V	82 **80**	88		dB
I_S	Supply Current (per channel)	No Load		12	16 **18**	mA

(7) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.
(8) Short circuit test is a momentary test. Output short circuit duration is 1.5ms.

Typical Performance Characteristics

Voltage Noise vs. Frequency

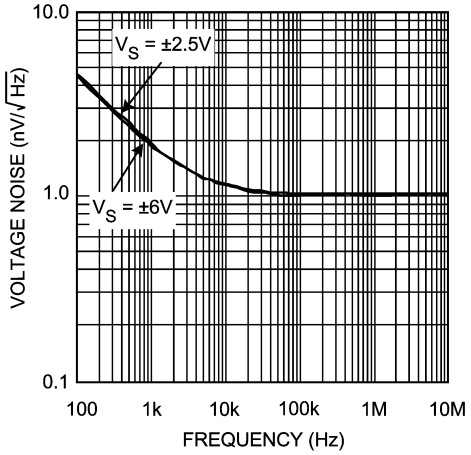


Figure 4.

Current Noise vs. Frequency

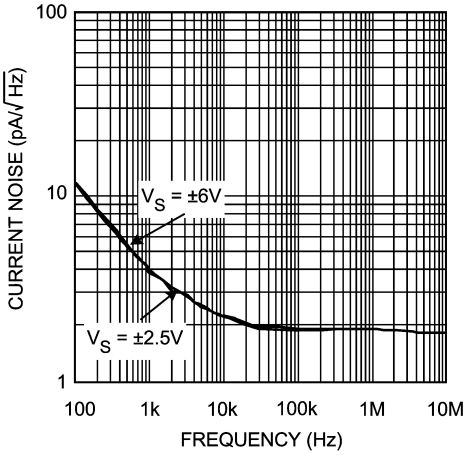


Figure 5.

Inverting Frequency Response

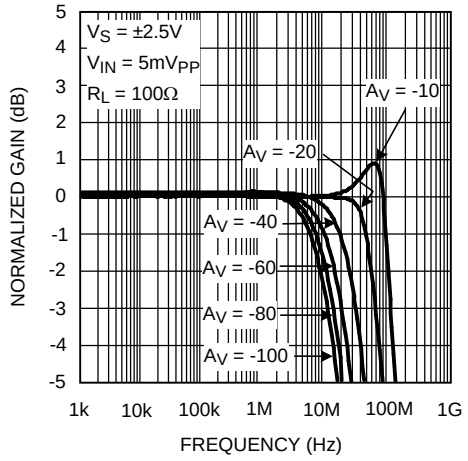


Figure 6.

Inverting Frequency Response

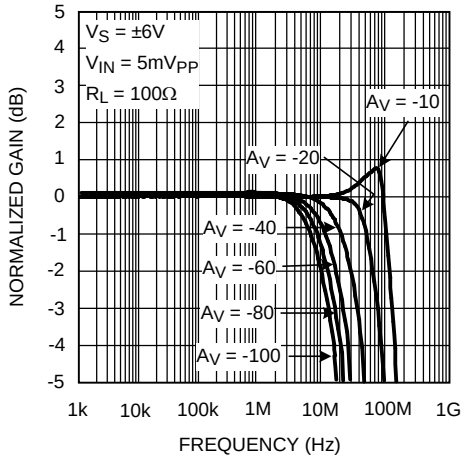


Figure 7.

Non-Inverting Frequency Response

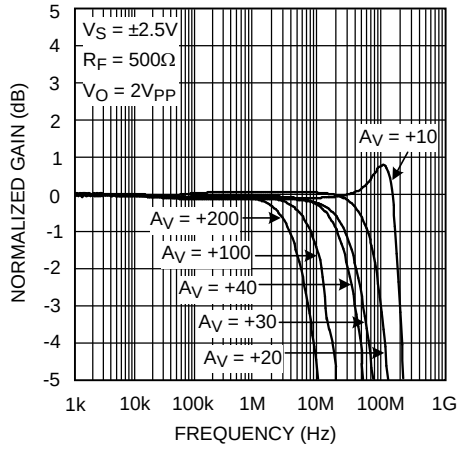


Figure 8.

Non-Inverting Frequency Response

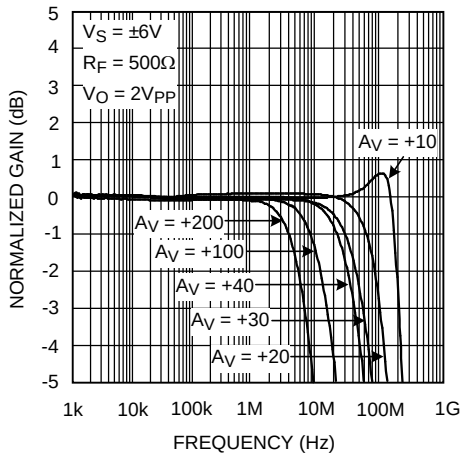


Figure 9.

Typical Performance Characteristics (continued)

Open Loop Frequency Response Over Temperature

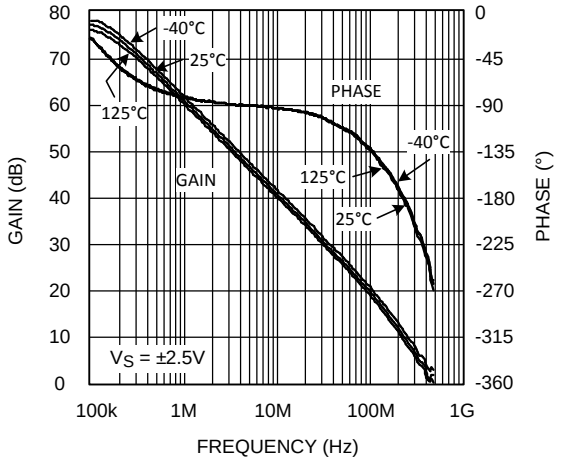


Figure 10.

Open Loop Frequency Response Over Temperature

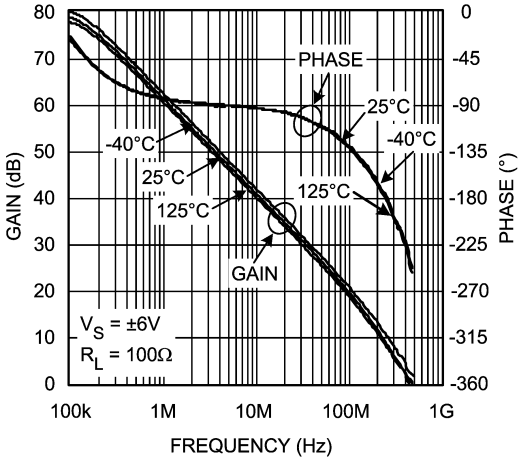


Figure 11.

Frequency Response with Cap. Loading

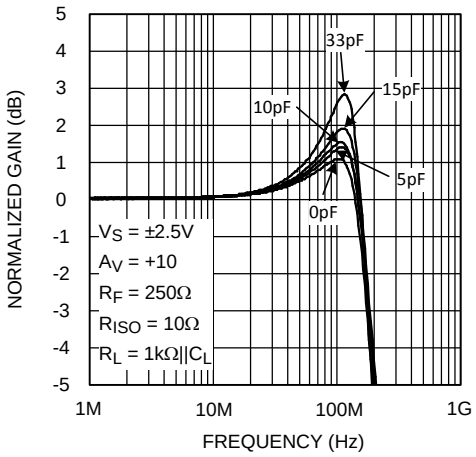


Figure 12.

Frequency Response with Cap. Loading

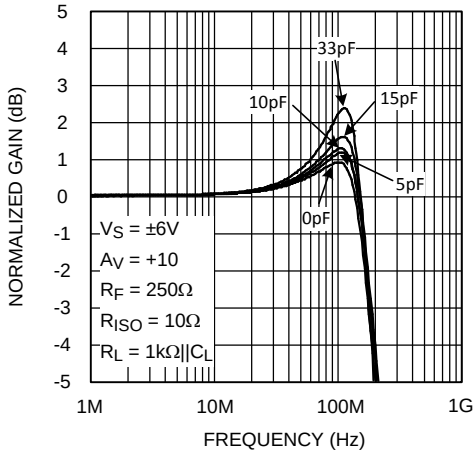


Figure 13.

Frequency Response with Cap. Loading

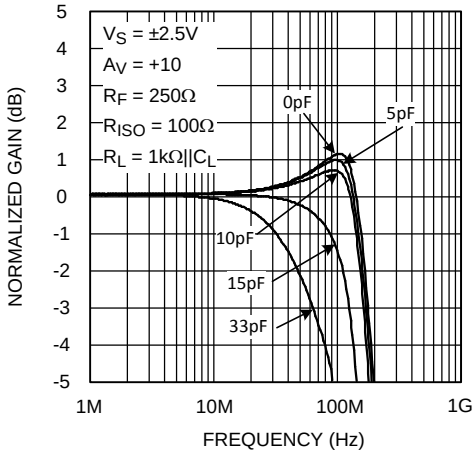


Figure 14.

Frequency Response with Cap. Loading

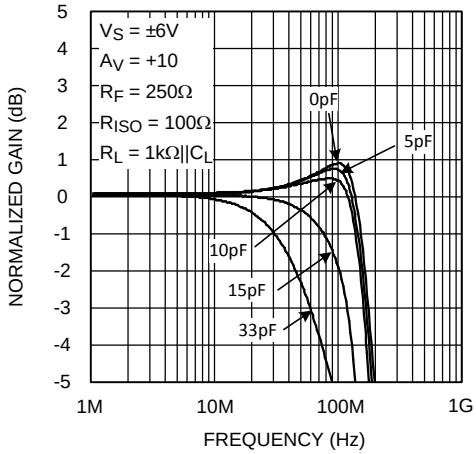


Figure 15.

Typical Performance Characteristics (continued)

Non-Inverting Frequency Response Varying V_{IN}

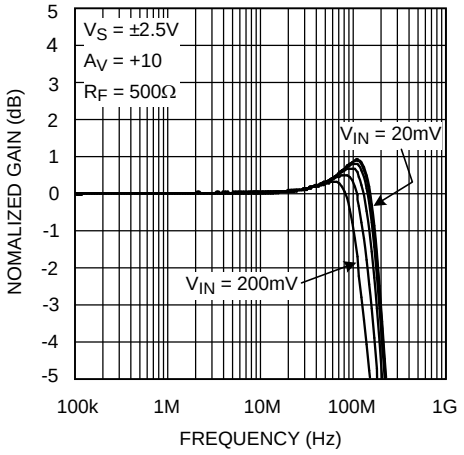


Figure 16.

Non-Inverting Frequency Response Varying V_{IN}

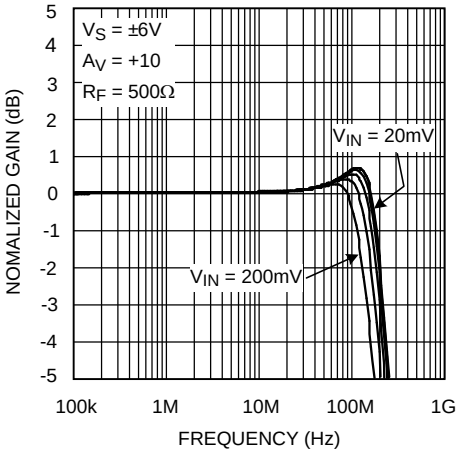


Figure 17.

Non-Inverting Frequency Response Varying V_{IN} (LMH6624)

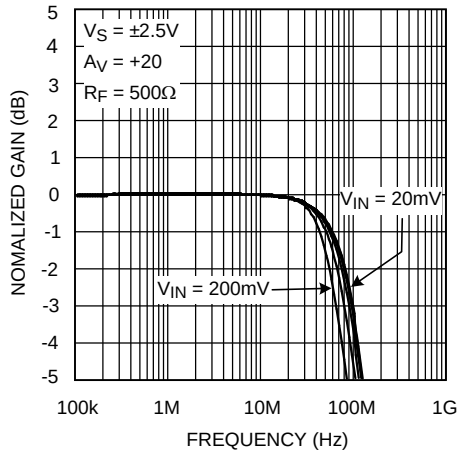


Figure 18.

Non-Inverting Frequency Response Varying V_{IN} (LMH6626)

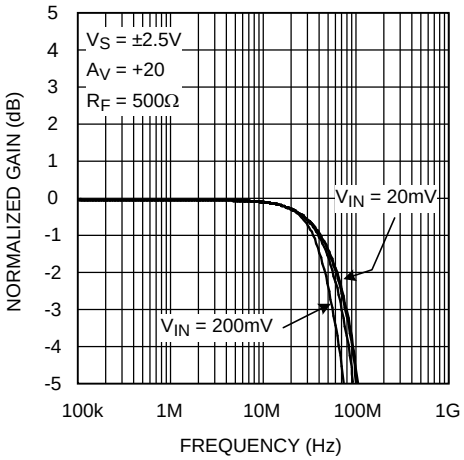


Figure 19.

Non-Inverting Frequency Response Varying V_{IN} (LMH6624)

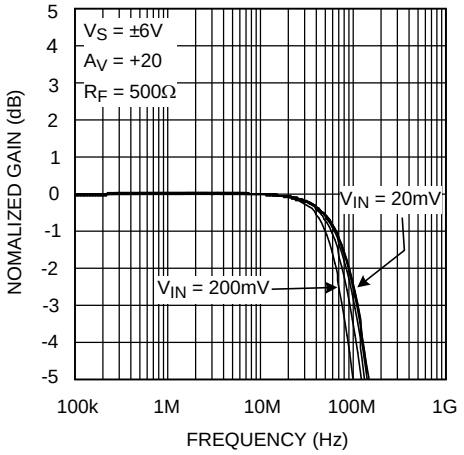


Figure 20.

Non-Inverting Frequency Response Varying V_{IN} (LMH6626)

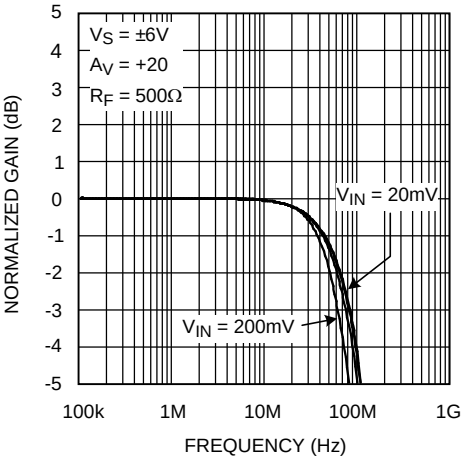


Figure 21.

Typical Performance Characteristics (continued)

Sourcing Current vs. V_{OUT} (LMH6624)

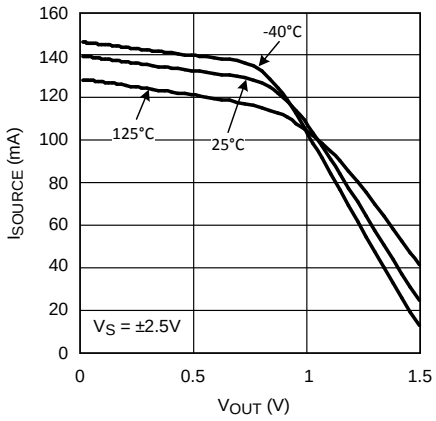


Figure 22.

Sourcing Current vs. V_{OUT} (LMH6626)

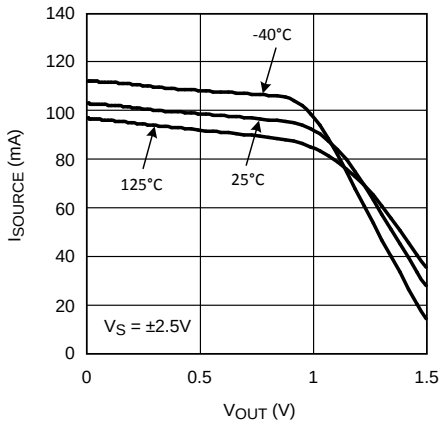


Figure 23.

Sourcing Current vs. V_{OUT} (LMH6624)

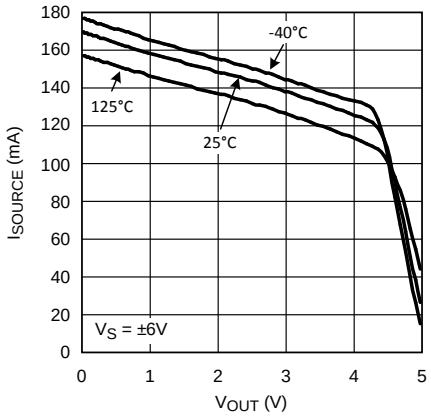


Figure 24.

Sourcing Current vs. V_{OUT} (LMH6626)

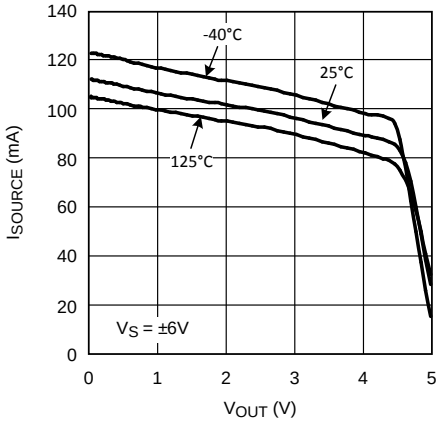


Figure 25.

V_{OS} vs. V_{SUPPLY} (LMH6624)

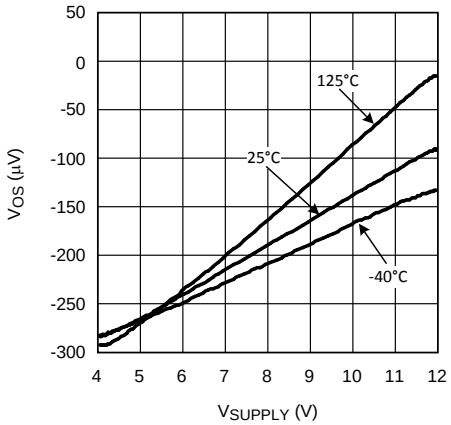


Figure 26.

V_{OS} vs. V_{SUPPLY} (LMH6626)

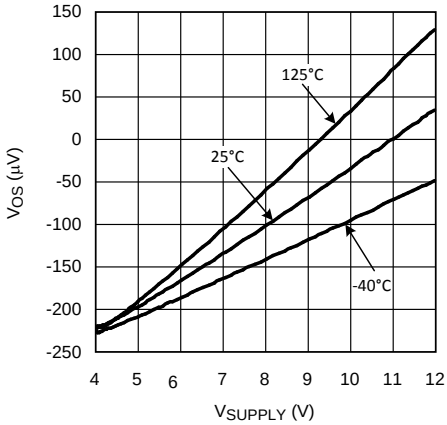


Figure 27.

Typical Performance Characteristics (continued)

Sinking Current vs. V_{OUT} (LMH6624)

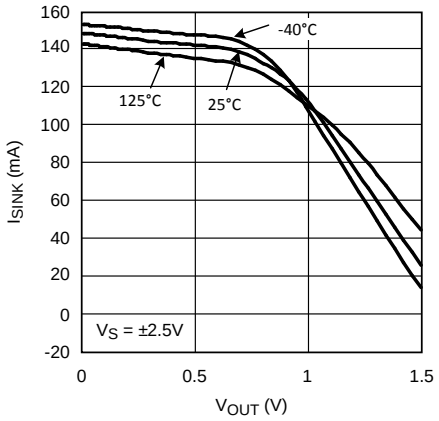


Figure 28.

Sinking Current vs. V_{OUT} (LMH6626)

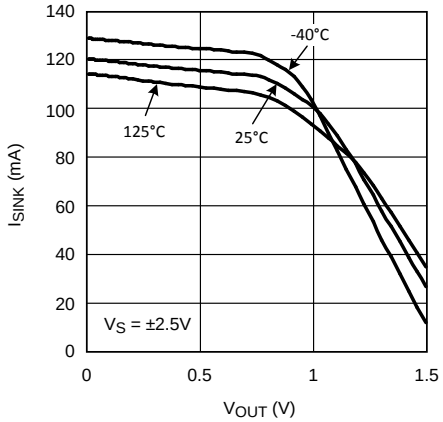


Figure 29.

Sinking Current vs. V_{OUT} (LMH6624)

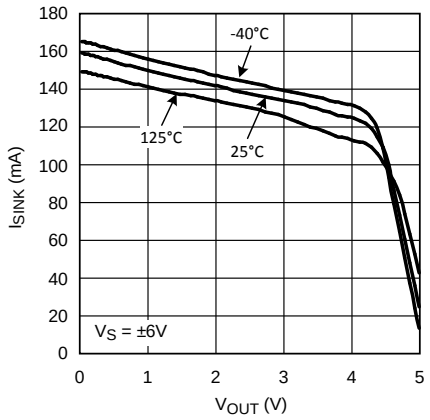


Figure 30.

Sinking Current vs. V_{OUT} (LMH6626)

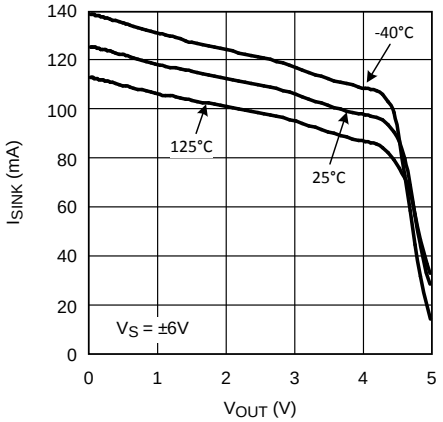


Figure 31.

I_{OS} vs. V_{SUPPLY}

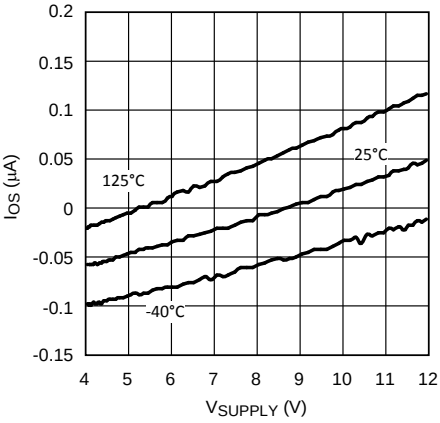


Figure 32.

Crosstalk Rejection vs. Frequency (LMH6626)

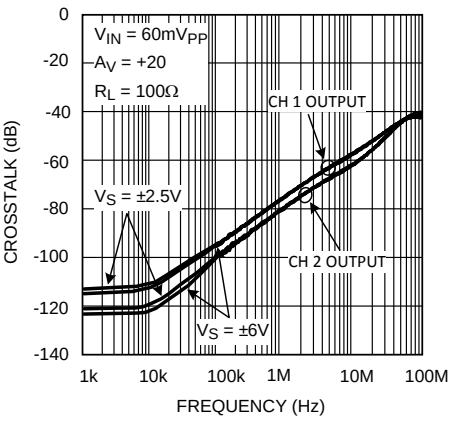


Figure 33.

Typical Performance Characteristics (continued)

Distortion vs. Frequency

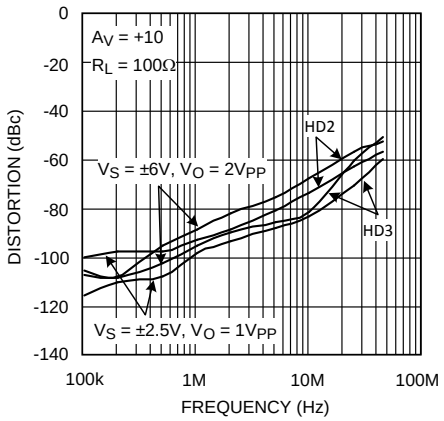


Figure 34.

Distortion vs. Frequency

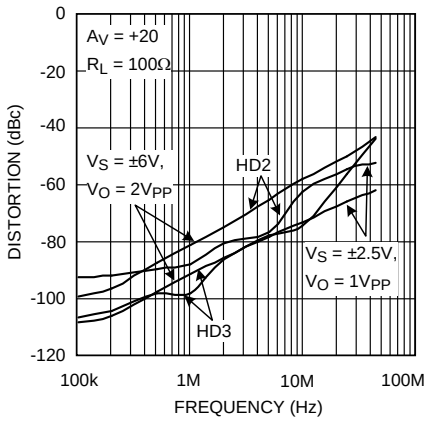


Figure 35.

Distortion vs. Frequency

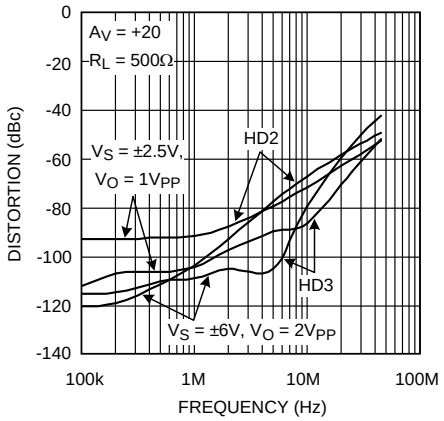


Figure 36.

Distortion vs. Gain

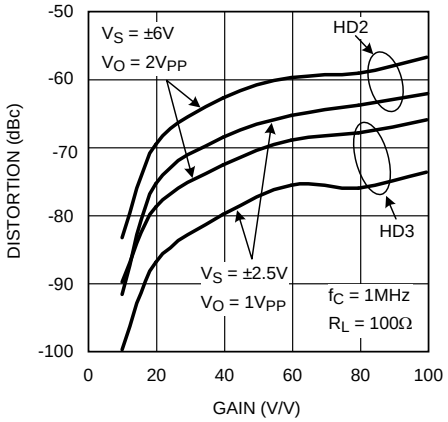


Figure 37.

Distortion vs. V_{OUT} Peak to Peak

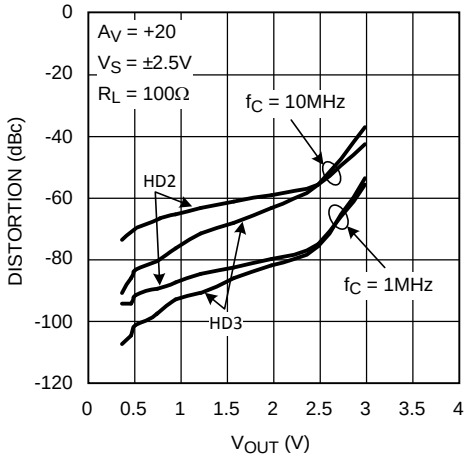


Figure 38.

Distortion vs. V_{OUT} Peak to Peak

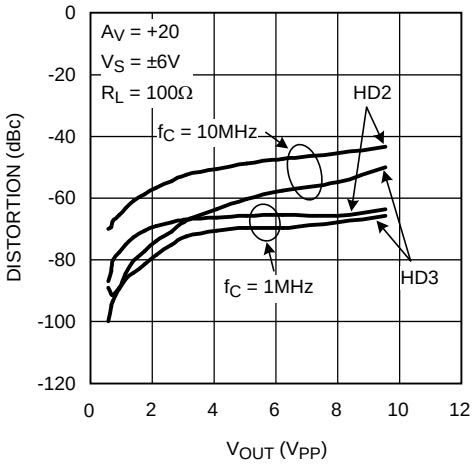


Figure 39.

Typical Performance Characteristics (continued)

Non-Inverting Large Signal Pulse Response

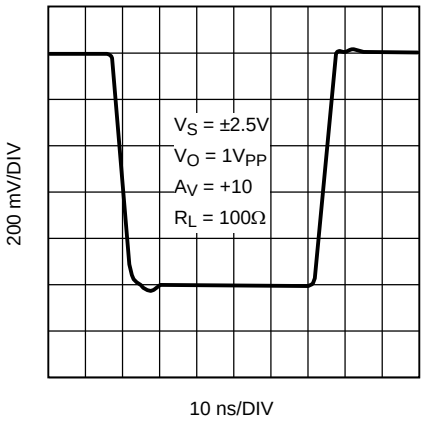


Figure 40.

Non-Inverting Large Signal Pulse Response

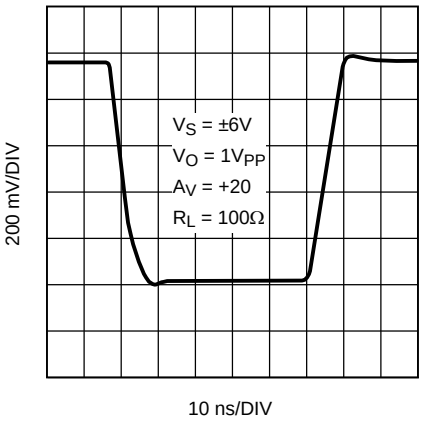


Figure 41.

Non-Inverting Small Signal Pulse Response

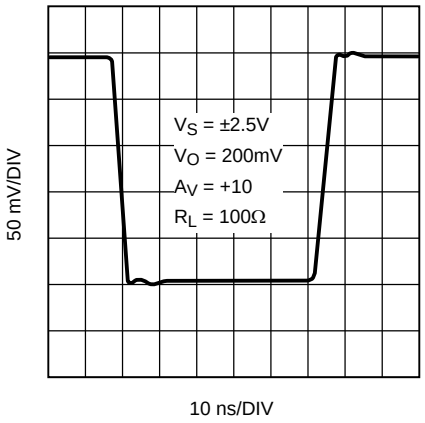


Figure 42.

Non-Inverting Small Signal Pulse Response

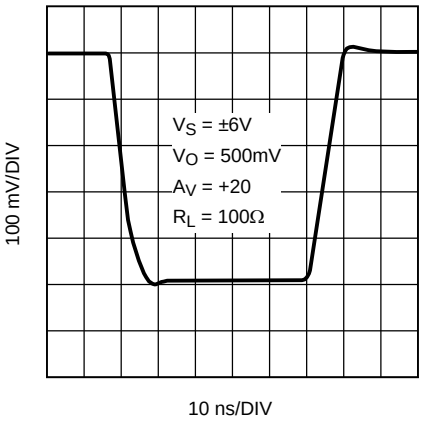


Figure 43.

PSRR vs. Frequency

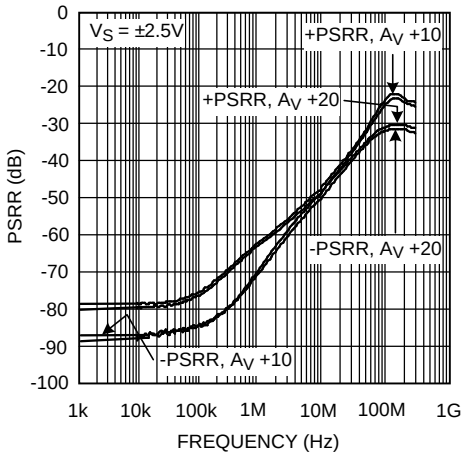


Figure 44.

PSRR vs. Frequency

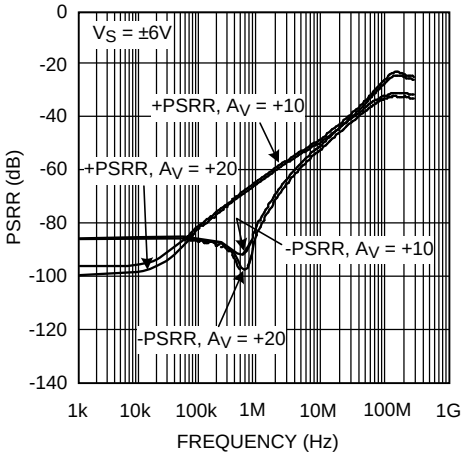


Figure 45.

Typical Performance Characteristics (continued)

Input Referred CMRR vs. Frequency

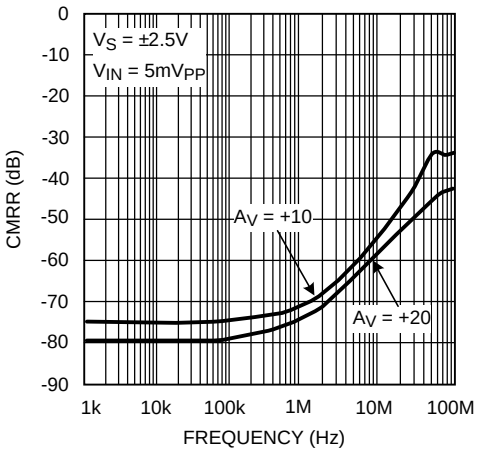


Figure 46.

Input Referred CMRR vs. Frequency

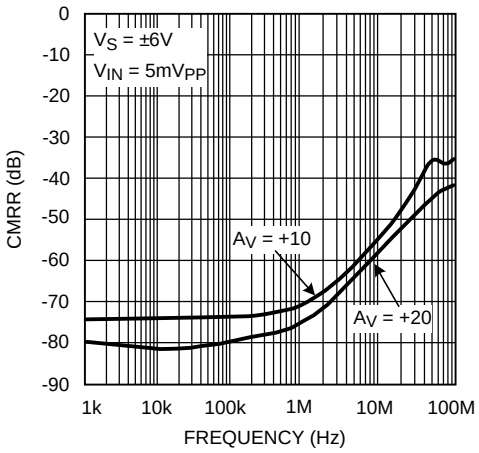


Figure 47.

Amplifier Peaking with Varying R_F

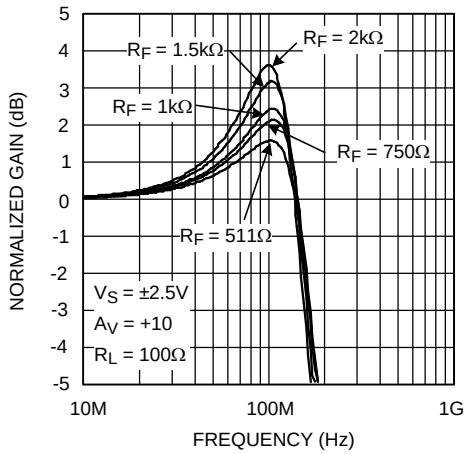


Figure 48.

Amplifier Peaking with Varying R_F

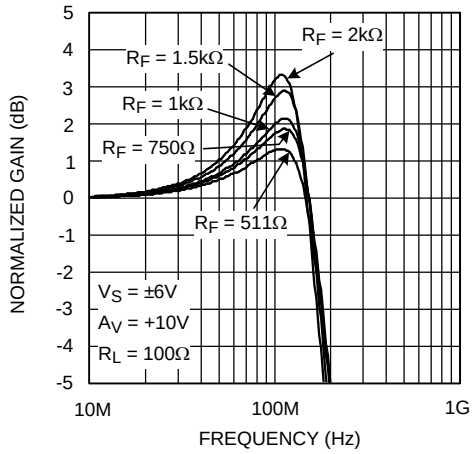


Figure 49.

APPLICATION SECTION

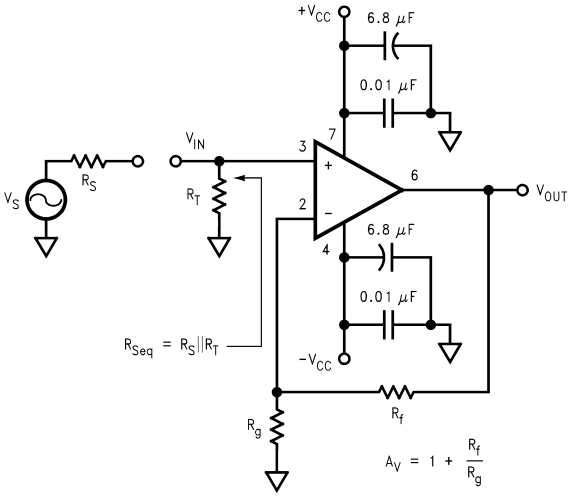


Figure 50. Non-Inverting Amplifier Configuration

INTRODUCTION

The LMH6624/LMH6626 are very wide gain bandwidth, ultra low noise voltage feedback operational amplifiers. Their excellent performances enable applications such as medical diagnostic ultrasound, magnetic tape & disk storage and fiber-optics to achieve maximum high frequency signal-to-noise ratios. The set of characteristic plots in the "Typical Performance" section illustrates many of the performance trade offs. The following discussion will enable the proper selection of external components to achieve optimum system performance.

BIAS CURRENT CANCELLATION

To cancel the bias current errors of the non-inverting configuration, the parallel combination of the gain setting (R_g) and feedback (R_f) resistors should equal the equivalent source resistance (R_{seq}) as defined in Figure 50. Combining this constraint with the non-inverting gain equation also seen in Figure 50, allows both R_f and R_g to be determined explicitly from the following equations:

$$R_f = A_V R_{seq} \text{ and } R_g = R_f/(A_V-1) \quad (1)$$

When driven from a 0Ω source, such as the output of an op amp, the non-inverting input of the LMH6624/LMH6626 should be isolated with at least a 25Ω series resistor.

As seen in Figure 51, bias current cancellation is accomplished for the inverting configuration by placing a resistor (R_b) on the non-inverting input equal in value to the resistance seen by the inverting input ($R_f||(R_g+R_s)$). R_b should to be no less than 25Ω for optimum LMH6624/LMH6626 performance. A shunt capacitor can minimize the additional noise of R_b.

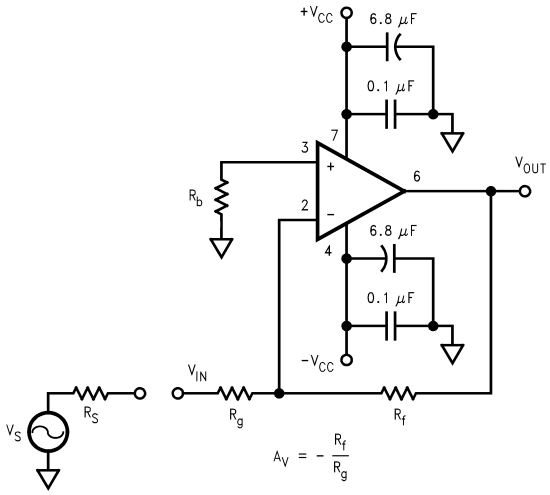


Figure 51. Inverting Amplifier Configuration

TOTAL INPUT NOISE vs. SOURCE RESISTANCE

To determine maximum signal-to-noise ratios from the LMH6624/LMH6626, an understanding of the interaction between the amplifier's intrinsic noise sources and the noise arising from its external resistors is necessary.

Figure 52 describes the noise model for the non-inverting amplifier configuration showing all noise sources. In addition to the intrinsic input voltage noise (e_n) and current noise ($i_n = i_n^+ = i_n^-$) source, there is also thermal voltage noise ($e_t = \sqrt{(4KTR)}$) associated with each of the external resistors. Equation 1 provides the general form for total equivalent input voltage noise density (e_{ni}). Equation 2 is a simplification of Equation 1 that assumes

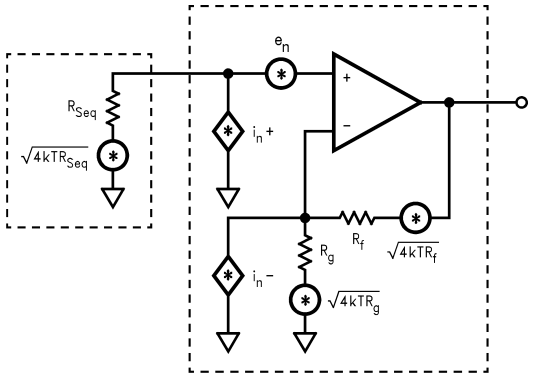


Figure 52. Non-Inverting Amplifier Noise Model

$$e_{ni} = \sqrt{e_n^2 + \left(i_{n+} R_{Seq}\right)^2 + 4kTR_{Seq} + \left(i_{n-}\left(R_f \| R_g\right)\right)^2 + 4kT\left(R_f \| R_g\right)} \quad (2)$$

$R_f||R_g = R_{seq}$ for bias current cancellation. Figure 53 illustrates the equivalent noise model using this assumption. Figure 54 is a plot of e_{ni} against equivalent source resistance (R_{seq}) with all of the contributing voltage noise source of Equation 2. This plot gives the expected e_{ni} for a given (R_{seq}) which assumes $R_f||R_g = R_{seq}$ for bias current cancellation. The total equivalent output voltage noise (e_{no}) is $e_{ni}*A_V$.

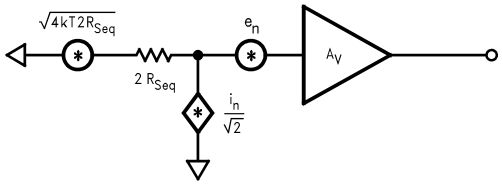


Figure 53. Noise Model with $R_f||R_g = R_{seq}$

$$e_{ni} = \sqrt{e_n^2 + 2(i_n R_{Seq})^2 + 4kT(2R_{Seq})} \quad (3)$$

As seen in Figure 54, e_{ni} is dominated by the intrinsic voltage noise (e_n) of the amplifier for equivalent source resistances below 33.5Ω. Between 33.5Ω and 6.43kΩ, e_{ni} is dominated by the thermal noise ($e_t = \sqrt{(4kT(2R_{seq}))}$ of the external resistor. Above 6.43kΩ, e_{ni} is dominated by the amplifier's current noise ($i_n = \sqrt{(2)}\ i_n R_{seq}$). When R_{seq} = 464Ω (ie., $e_n/\sqrt{(2)}\ i_n$) the contribution from voltage noise and current noise of LMH6624/LMH6626 is equal. For example, configured with a gain of +20V/V giving a −3dB of 90MHz and driven from R_{seq} = 25Ω, the LMH6624 produces a total equivalent input noise voltage ($e_{ni} \times \sqrt{Hz}1.57*90MHz$) of 16.5μ$V_{rms}$.

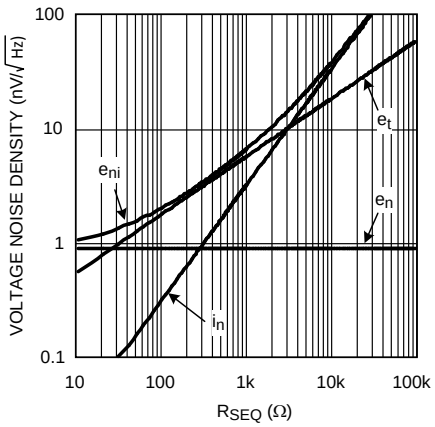


Figure 54. Voltage Noise Density vs. Source Resistance

If bias current cancellation is not a requirement, then $R_f||R_g$ need not equal R_{seq}. In this case, according to Equation 1, $R_f||R_g$ should be as low as possible to minimize noise. Results similar to Equation 1 are obtained for the inverting configuration of Figure 51 if R_{seq} is replaced by R_b and R_g is replaced by $R_g + R_s$. With these substitutions, Equation 1 will yield an e_{ni} referred to the non-inverting input. Referring e_{ni} to the inverting input is easily accomplished by multiplying e_{ni} by the ratio of non-inverting to inverting gains.

NOISE FIGURE

Noise Figure (NF) is a measure of the noise degradation caused by an amplifier.

$$NF = 10LOG\left\{\frac{S_i / N_i}{S_o / N_o}\right\} = 10LOG\left\{\frac{e_{ni}^2}{e_t^2}\right\} \quad (4)$$

The Noise Figure formula is shown in Equation 4. The addition of a terminating resistor R_T, reduces the external thermal noise but increases the resulting NF. The NF is increased because R_T reduces the input signal amplitude thus reducing the input SNR.

$$NF = 10\ LOG\left[\frac{e_n^2 + i_n^2 (R_{Seq}^2 + (R_f||R_g)^2) + 4KT\ (R_{Seq} + (R_f||R_g))}{4KT\ (R_{Seq} + (R_f||R_g))}\right] \quad (5)$$

The noise figure is related to the equivalent source resistance (R_{seq}) and the parallel combination of R_f and R_g. To minimize noise figure.

- Minimize $R_f||R_g$
- Choose the Optimum R_S (R_{OPT})

R_{OPT} is the point at which the NF curve reaches a minimum and is approximated by:

$$R_{OPT} \approx e_n/i_n \quad (6)$$

SINGLE SUPPLY OPERATION

The LMH6624/LMH6626 can be operated with single power supply as shown in Figure 55. Both the input and output are capacitively coupled to set the DC operating point.

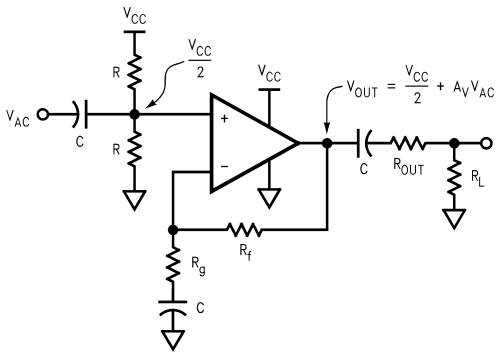


Figure 55. Single Supply Operation

LOW NOISE TRANSIMPEDANCE AMPLIFIER

Figure 56 implements a low-noise transimpedance amplifier commonly used with photo-diodes. The transimpedance gain is set by R_f. Equation 4 provides the total input current noise density (i_{ni}) equation for the basic transimpedance configuration and is plotted against feedback resistance (R_f) showing all contributing noise sources in Figure 57. This plot indicates the expected total equivalent input current noise density (i_{ni}) for a given feedback resistance (R_f). The total equivalent output voltage noise density (e_{no}) is i_{ni}*R_f.

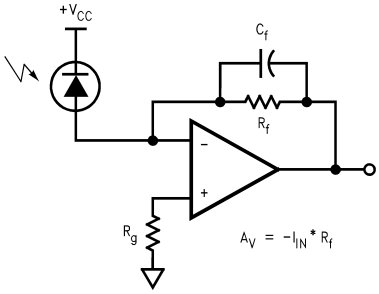


Figure 56. Transimpedance Amplifier Configuration

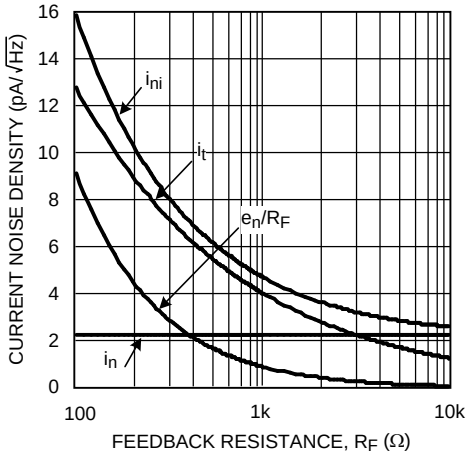


Figure 57. Current Noise Density vs. Feedback Resistance

$$i_{ni} = \sqrt{i_n^2 + \left(\frac{e_n}{R_f}\right)^2 + \frac{4kT}{R_f}} \quad (7)$$

LOW NOISE INTEGRATOR

The LMH6624/LMH6626 implement a deBoo integrator shown in Figure 58. Positive feedback maintains integration linearity. The LMH6624/LMH6626's low input offset voltage and matched inputs allow bias current cancellation and provide for very precise integration. Keeping R_G and R_S low helps maintain dynamic stability.

$$V_O \cong V_{IN} \frac{K_O}{sR_SC} \quad ; \quad K_O = 1 + \frac{R_F}{R_G}$$

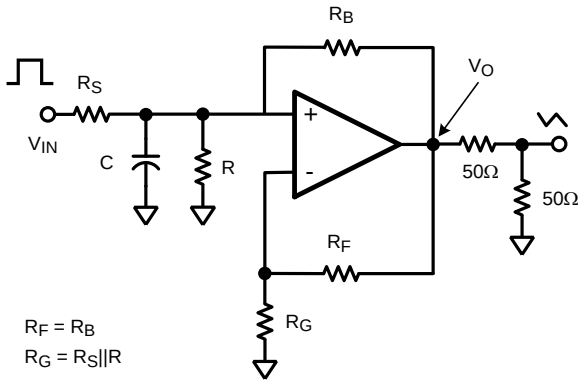


Figure 58. Low Noise Integrator

HIGH-GAIN SALLEN-KEY ACTIVE FILTERS

The LMH6624/LMH6626 are well suited for high gain Sallen-Key type of active filters. Figure 59 shows the 2nd order Sallen-Key low pass filter topology. Using component predistortion methods discussed in OA-21 (SNOA369) enables the proper selection of components for these high-frequency filters.

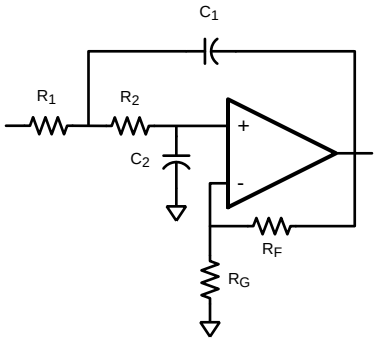
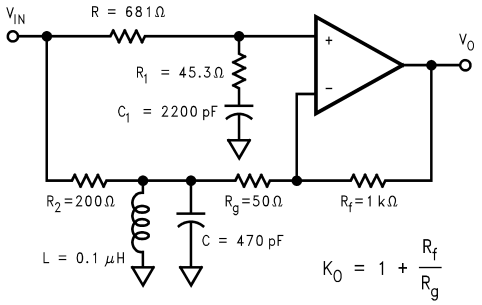


Figure 59. Sallen-Key Active Filter Topology

LOW NOISE MAGNETIC MEDIA EQUALIZER

The LMH6624/LMH6626 implement a high-performance low noise equalizer for such application as magnetic tape channels as shown in Figure 60. The circuit combines an integrator with a bandpass filter to produce the low noise equalization. The circuit's simulated frequency response is illustrated in Figure 61.



$$\frac{V_O}{V_{IN}} = K_O \left(\frac{sC_1 R_1 + 1}{sC_1 (R_1 + R) + 1} - \left(\frac{R_f}{R_f + R_g} \right) \frac{sLR_g}{s^2 LCR_2 R_g + sL(R_2 + R_g) + R_2 R_g} \right)$$

Figure 60. Low Noise Magnetic Media Equalizer

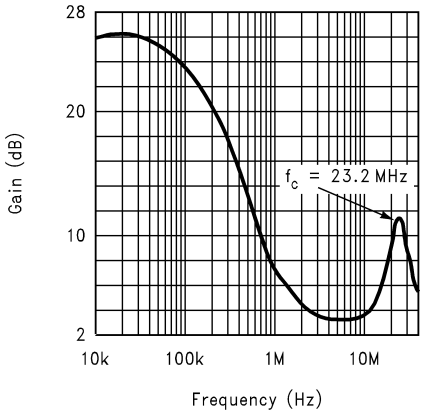


Figure 61. Equalizer Frequency Response

LAYOUT CONSIDERATION

TI suggests the copper patterns on the evaluation boards listed below as a guide for high frequency layout. These boards are also useful as an aid in device testing and characterization. As is the case with all high-speed amplifiers, accepted-practice RF design technique on the PCB layout is mandatory. Generally, a good high frequency layout exhibits a separation of power supply and ground traces from the inverting input and output pins. Parasitic capacitances between these nodes and ground may cause frequency response peaking and possible circuit oscillations (see Application Note OA-15 (SNOA367) for more information). Use high quality chip capacitors with values in the range of 1000pF to 0.1F for power supply bypassing. One terminal of each chip capacitor is connected to the ground plane and the other terminal is connected to a point that is as close as possible to each supply pin as allowed by the manufacturer's design rules. In addition, connect a tantalum capacitor with a value between 4.7μF and 10μF in parallel with the chip capacitor. Signal lines connecting the feedback and gain resistors should be as short as possible to minimize inductance and microstrip line effect. Place input and output termination resistors as close as possible to the input/output pins. Traces greater than 1 inch in length should be impedance matched to the corresponding load termination.

Symmetry between the positive and negative paths in the layout of differential circuitry should be maintained to minimize the imbalance of amplitude and phase of the differential signal.

Component value selection is another important parameter in working with high speed/high performance amplifiers. Choosing external resistors that are large in value compared to the value of other critical components will affect the closed loop behavior of the stage because of the interaction of these resistors with parasitic capacitances. These parasitic capacitors could either be inherent to the device or be a by-product of the board layout and component placement. Moreover, a large resistor will also add more thermal noise to the signal path. Either way, keeping the resistor values low will diminish this interaction. On the other hand, choosing very low value resistors could load down nodes and will contribute to higher overall power dissipation and high distortion.

Device	Package	Evaluation Board Part Number
LMH6624MF	SOT-23–5	LMH730216
LMH6624MA	SOIC-8	LMH730227
LMH6626MA	SOIC-8	LMH730036
LMH6626MM	VSSOP-8	LMH730123

REVISION HISTORY

Changes from Revision E (March 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	20

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMH6624MA	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 125	LMH66 24MA	Samples
LMH6624MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMH66 24MA	Samples
LMH6624MAX	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125	LMH66 24MA	Samples
LMH6624MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMH66 24MA	Samples
LMH6624MF	ACTIVE	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	A94A	Samples
LMH6624MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	A94A	Samples
LMH6624MFX	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125	A94A	Samples
LMH6624MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	A94A	Samples
LMH6626MA	ACTIVE	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 125	LMH66 26MA	Samples
LMH6626MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMH66 26MA	Samples
LMH6626MAX	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125	LMH66 26MA	Samples
LMH6626MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMH66 26MA	Samples
LMH6626MM	ACTIVE	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 125	A98A	Samples
LMH6626MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	A98A	Samples
LMH6626MMX	ACTIVE	VSSOP	DGK	8	3500	TBD	Call TI	Call TI	-40 to 125	A98A	Samples
LMH6626MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	A98A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

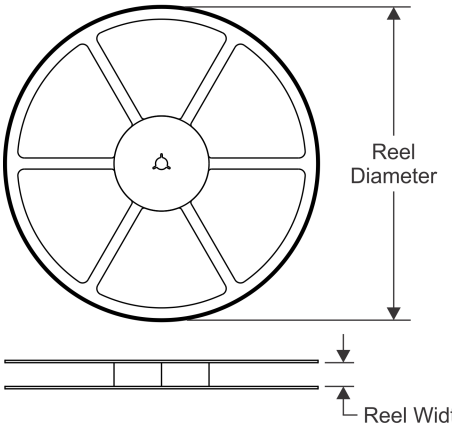
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

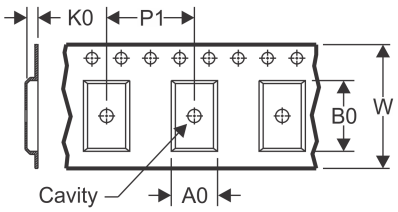
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

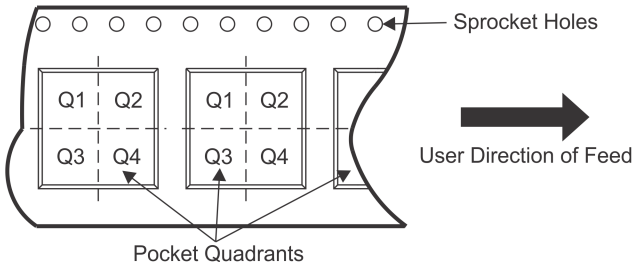


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

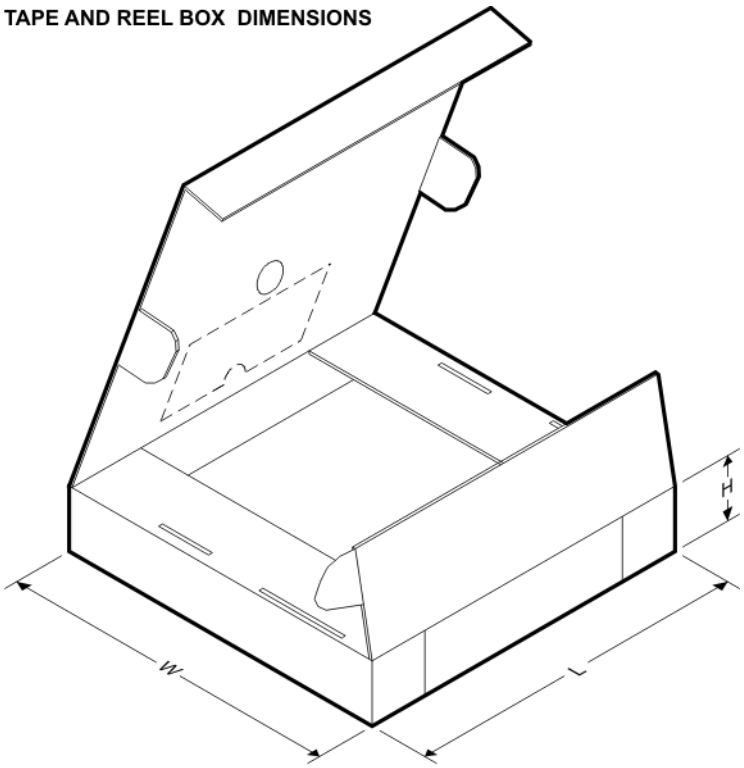
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6624MAX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6624MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6624MF	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6624MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6624MFX	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6624MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMH6626MAX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6626MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMH6626MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMH6626MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMH6626MMX	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMH6626MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

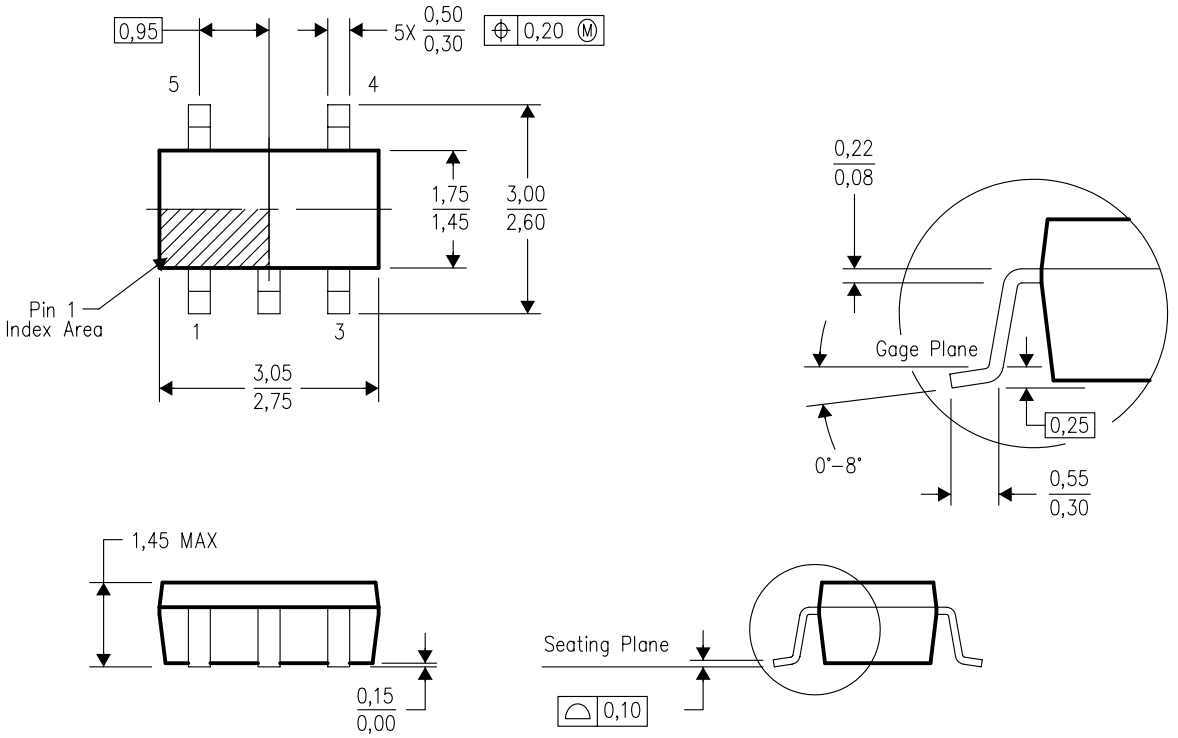
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6624MAX	SOIC	D	8	2500	367.0	367.0	35.0
LMH6624MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6624MF	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMH6624MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMH6624MFX	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMH6624MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMH6626MAX	SOIC	D	8	2500	367.0	367.0	35.0
LMH6626MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMH6626MM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMH6626MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMH6626MMX	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMH6626MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

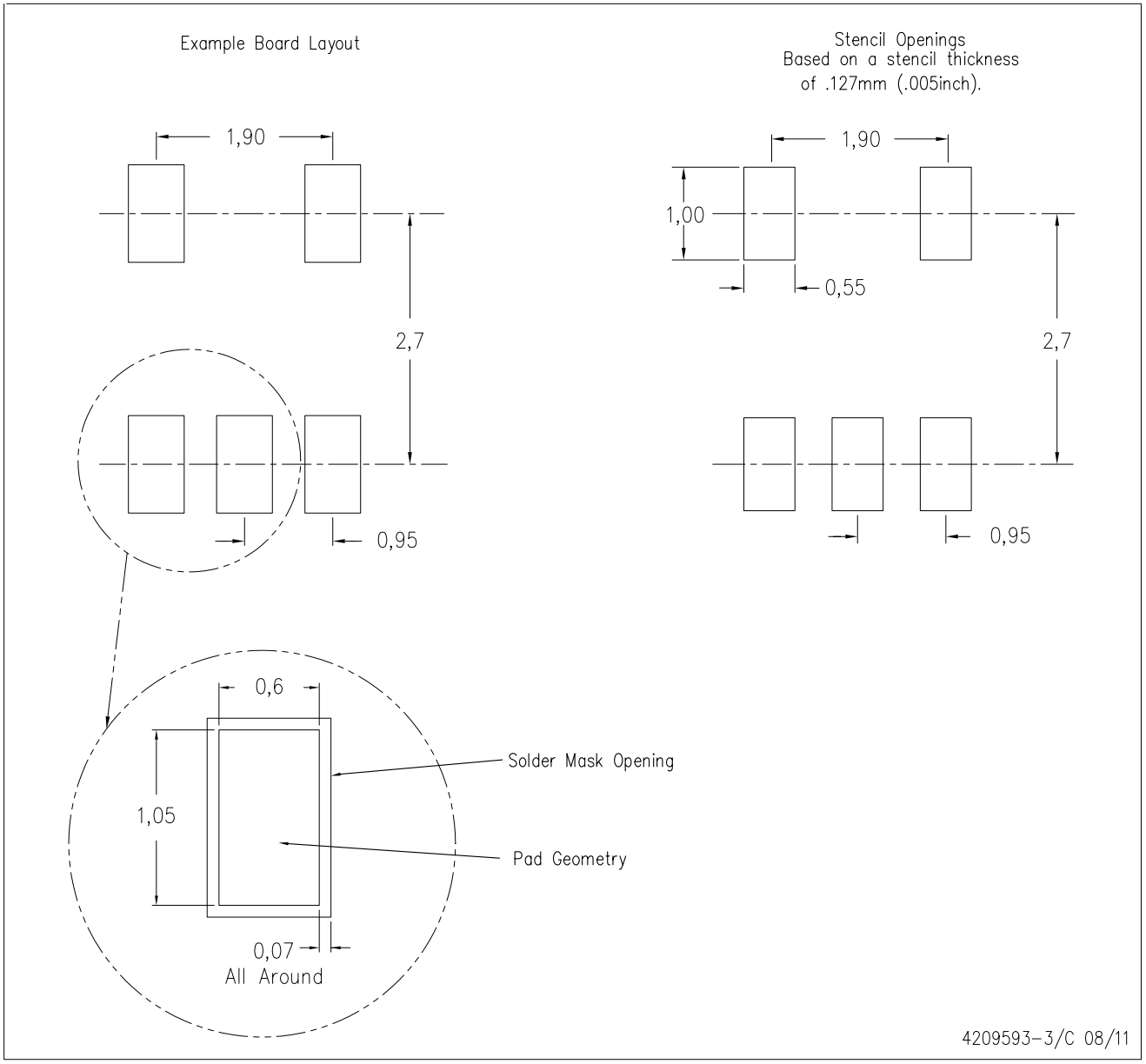
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/K 03/2006

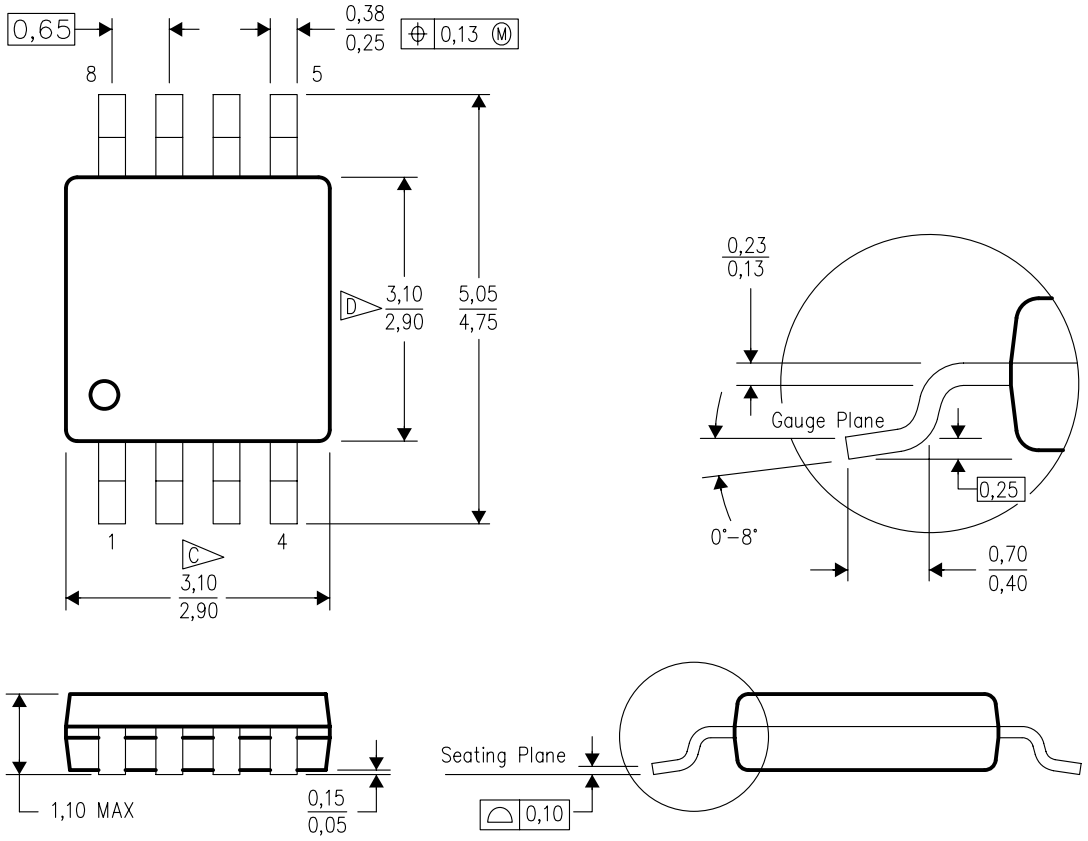
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

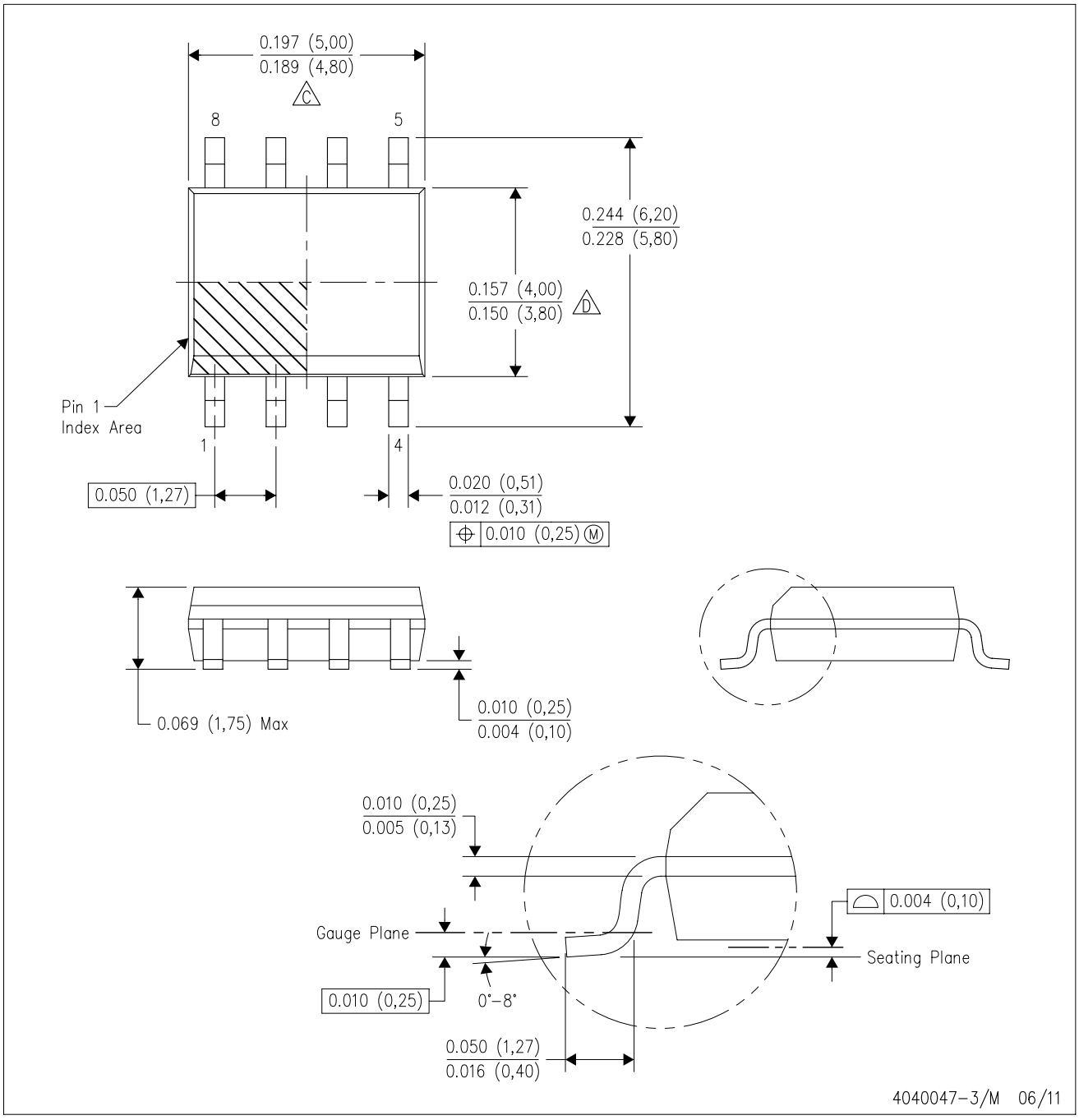
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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