LM124A/LM124JAN Low Power Quad Operational Amplifiers

Check for Samples: LM124JAN

FEATURES

- **Internally Frequency Compensated for Unity Gain**
- **Large DC Voltage Gain 100 dB**
- **Wide Bandwidth (Unity Gain)1 MHz (Temperature Compensated)**
- **Wide Power Supply Range:**
  - **Single Supply 3V to 32V**
  - **or Dual Supplies ±1.5V to ±16V**
- **Very Low Supply Current Drain (700 μA)—Essentially Independent of Supply Voltage**
- **Low Input Biasing Current 45 nA (Temperature Compensated)**
- **Low Input Offset Voltage 2 mV and Offset Current: 5 nA**
- **Input Common-Mode Voltage Range Includes Ground**
- **Differential Input Voltage Range Equal to the Power Supply Voltage**
- **Large Output Voltage Swing 0V to $V^+ - 1.5V$**

UNIQUE CHARACTERISTICS

- **In the Linear Mode the Input Common-Mode Voltage Range Includes Ground and the Output Voltage can also Swing to Ground, even though Operated from Only a Single Power Supply Voltage**
- **The Unity Gain Cross Frequency is Temperature Compensated**
- **The Input Bias Current is also Temperature Compensated**

ADVANTAGES

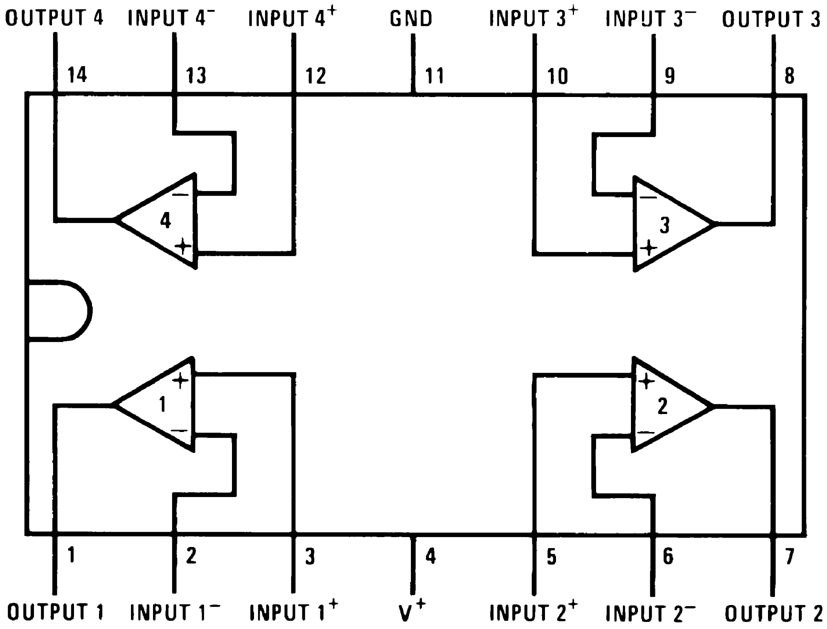
- **Eliminates Need for Dual Supplies**
- **Four Internally Compensated Op Amps in a Single Package**
- **Allows Directly Sensing Near GND and V_{OUT} also goes to GND**
- **Compatible with all Forms of Logic**
- **Power Drain Suitable for Battery Operation**

DESCRIPTION

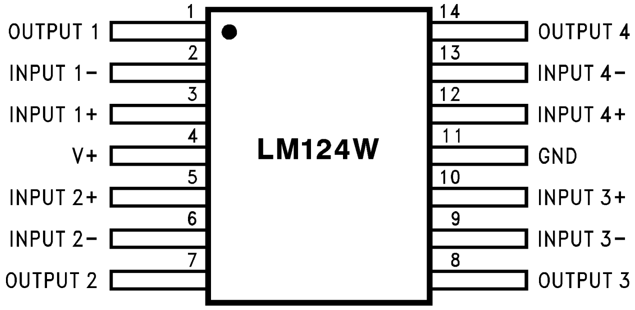
The LM124/124A consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124/124A can be directly operated off of the standard +5Vdc power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional +15Vdc power supplies.

Connection Diagrams



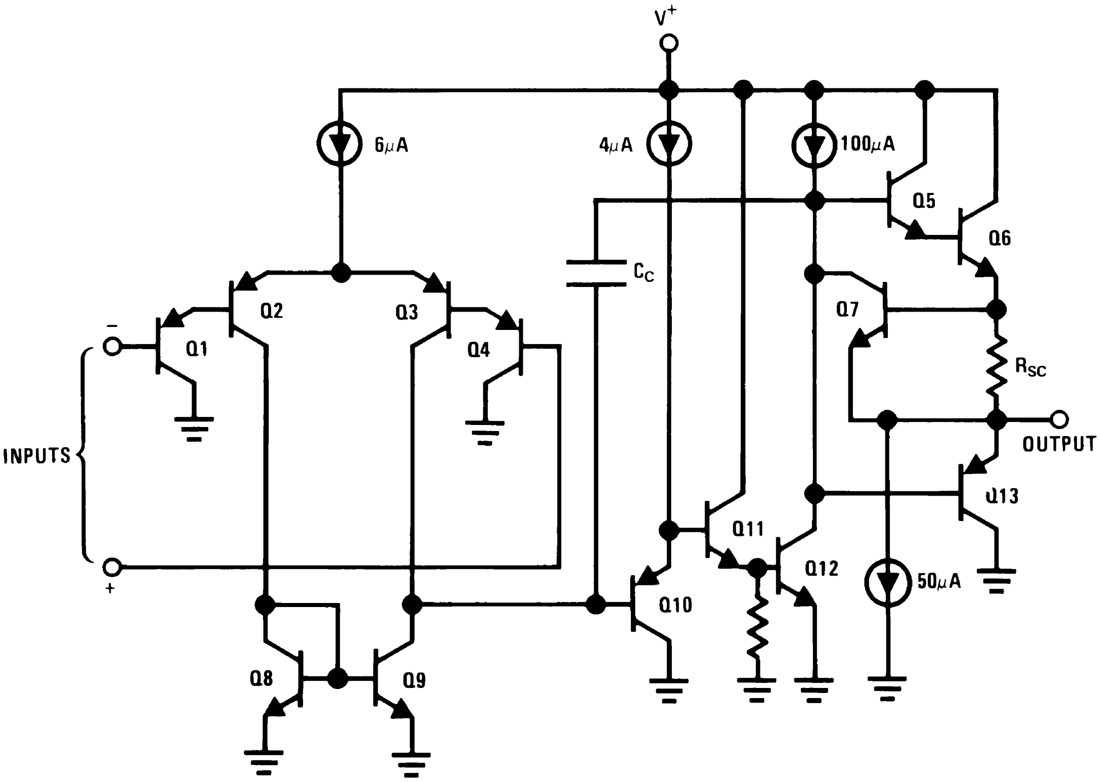
Dual-In-Line CDIP Package
Top View
See Package Number J



CLGA Package
See Package Number NAC or NAD

Schematic Diagram

(Each Amplifier)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)

Power Dissipation(2)		CDIP		400mW
		CLGA		350mW
		Ceramic SOIC		350mW
Supply Voltage, V^+				$36V_{DC}$ or $\pm 18V_{DC}$
Input Voltage Differential				$30V_{DC}$
Input Voltage				$-0.3V_{DC}$ to $+32V_{DC}$
Input Current ($V_{IN} < -0.3V_{DC}$)(3)				10 to 0.1mA
Output Short-Circuit to GND(4)		$V^+ \le 15V_{DC}$ and $T_A = 25°C$ (One Amplifier)		Continuous
Operating Temperature Range				$-55°C \le T_A \le +125°C$
Maximum Junction Temperature(2)				175°C
Storage Temperature Range				$-65°C \le T_A \le +150°C$
Lead Temperature (Soldering, 10 seconds)				260°C
Thermal Resistance	**θ_{JA}**	**CDIP**	(Still Air)	120°C/W
			(500LF/Min Air flow)	51°C/W
		CLGA	(Still Air)	140°C/W
			(500LF/Min Air flow)	116°C/W
		Ceramic SOIC	(Still Air)	140°C/W
			(500LF/Min Air flow)	116°C/W
	θ_{JC}	CDIP		35°C/W
		CLGA		60°C/W
		Ceramic SOIC		60°C/W
Package Weight (Typical)	CDIP			2200mg
	CLGA			460mg
	Ceramic SOIC			410mg
ESD Tolerance(5)				250V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

(3) This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3V_{DC}$ (at 25°C).

(4) Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40mA independent of the magnitude of V^+. At values of supply voltage in excess of $+15V_{DC}$, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

(5) Human body model, 1.5 kΩ in series with 100 pF.

Table 1. QUALITY CONFORMANCE INSPECTION (1)

Subgroup	Description	Temp (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55

(1) MIL-STD-883, Method 5005 — Group A

LM124 JAN DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	NOTES	MIN	MAX	UNIT	SUB GROUPS
V_{IO}	Input Offset Voltage	V_{CC}^{+} = 30V, V_{CC}^{-}= Gnd, V_{CM} = +15V		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
		V_{CC}^{+} = 2V, V_{CC}^{-}= -28V, V_{CM} = -13V		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
		V_{CC}^{+} = 5V, V_{CC}^{-}= Gnd, V_{CM} = +1.4V		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
		V_{CC}^{+} = 2.5V, V_{CC}^{-}= -2.5V, V_{CM} = -1.1V		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
I_{IO}	Input Offset Current	V_{CC}^{+} = 30V, V_{CC}^{-}= Gnd, V_{CM} = +15V		-30	30	nA	1, 2
				-75	75	nA	3
		V_{CC}^{+} = 2V, V_{CC}^{-}= -28V, V_{CM} = -13V		-30	30	nA	1, 2
				-75	75	nA	3
		V_{CC}^{+} = 5V, V_{CC}^{-}= Gnd, V_{CM} = +1.4V		-30	30	nA	1, 2
				-75	75	nA	3
		V_{CC}^{+} = 2.5V, V_{CC}^{-}= -2.5V, V_{CM} = -1.1V		-30	30	nA	1, 2
				-75	75	nA	3
±I_{IB}	Input Bias Current	V_{CC}^{+} = 30V, V_{CC}^{-}= Gnd, V_{CM} = +15V		-150	+0.1	nA	1, 2
				-300	+0.1	nA	3
		V_{CC}^{+} = 2V, V_{CC}^{-}= -28V, V_{CM} = -13V		-150	+0.1	nA	1, 2
				-300	+0.1	nA	3
		V_{CC}^{+} = 5V, V_{CC}^{-}= Gnd, V_{CM} = +1.4V		-150	+0.1	nA	1, 2
				-300	+0.1	nA	3
		V_{CC}^{+} = 2.5V, V_{CC}^{-}= -2.5V, V_{CM} = -1.1V		-150	+0.1	nA	1, 2
				-300	+0.1	nA	3
+PSRR	Power Supply Rejection Ratio	V_{CC}^{-}= Gnd, V_{CM} = -1.4V, 5V ≤ V_{CC} ≤ 30V		-100	100	µV/V	1, 2, 3
CMRR	Common Mode Rejection Ratio		See (1)	76		dB	1, 2, 3
I_{OS}^{+}	Output Short Circuit Current	V_{CC}^{+} = 30V, V_{CC}^{-}= Gnd, Vo = +25V		-70		mA	1, 2, 3

(1) The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is $V^{+} - 1.5V$ (at 25°C), but either or both inputs can go to +32V without damage independent of the magnitude of V^{+}.

LM124 JAN DC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	CONDITIONS	NOTES	MIN	MAX	UNIT	SUB GROUPS
I_{CC}	Power Supply Current	$V_{CC}^+ = 30V$, $V_{CC}^- =$ Gnd			3	mA	1, 2
					4	mA	3
Delta V_{IO} / Delta T	Input Offset Voltage Temperature Sensitivity	+25°C ≤ T_A ≤ +125°C, $V_{CC}^+ = 5V$, $V_{CC}^- = 0V$, $V_{CM} = +1.4V$		-30	30	µV/°C	2
		-55°C ≤ T_A ≤ +25°C, $V_{CC}^+ = 5V$, $V_{CC}^- = 0V$, $V_{CM} = +1.4V$		-30	30	µV/°C	3
Delta I_{IO} / Delta T	Input Offset Current Temperature Sensitivity	+25°C ≤ T_A ≤ +125°C, $V_{CC}^+ = 5V$, $V_{CC}^- = 0V$, $V_{CM} = +1.4V$		-400	400	pA/°C	2
		-55°C ≤ T_A ≤ +25°C, $V_{CC}^+ = 5V$, $V_{CC}^- = 0V$, $V_{CM} = +1.4V$		-700	700	pA/°C	3
V_{OL}	Logical "0" Output Voltage	$V_{CC}^+ = 30V$, $V_{CC}^- =$ Gnd, $R_L = 10K\Omega$			35	mV	4, 5, 6
		$V_{CC}^+ = 30V$, $V_{CC}^- =$ Gnd, $I_{OL} = 5mA$			1.5	V	4, 5 ,6
		$V_{CC}^+ = 4.5V$, $V_{CC}^- =$ Gnd, $I_{OL} = 2\mu A$			0.4	V	4, 5, 6
V_{OH}	Logical "1" Output Voltage	$V_{CC}^+ = 30V$, $V_{CC}^- =$ Gnd, $I_{OH} = -10mA$		27		V	4, 5, 6
		$V_{CC}^+ = 4.5V$, $V_{CC}^- =$ Gnd, $I_{OH} = -10mA$		2.4		V	4, 5
				2.3		V	6
A_{VS}^+	Voltage Gain	$V_{CC}^+ = 30V$, $V_{CC}^- =$ Gnd, 1V ≤ V_O ≤26V, $R_L = 10K\Omega$		50		V/mV	4
				25		V/mV	5, 6
		$V_{CC}^+ = 30V$, $V_{CC}^- =$ Gnd, 5V ≤ V_O ≤ 20V, $R_L = 2K\Omega$		50		V/mV	4
				25		V/mV	5, 6
A_{VS}	Gain Voltage	$V_{CC}^+ = 5V$, $V_{CC}^- =$ Gnd, 1V ≤ V_O ≤ 2.5V, $R_L = 10K\Omega$		10		V/mV	4, 5, 6
		$V_{CC}^+ = 5V$, $V_{CC}^- =$ Gnd, 1V ≤ V_O ≤ 2.5V, $R_L = 2K\Omega$		10		V/mV	4, 5, 6
$+V_{OP}$	Maximum Output Voltage Swing	$V_{CC}^+ = 30V$, $V_{CC}^- =$ Gnd, $V_O = +30V$, $R_L = 10K\Omega$		27		V	4, 5, 6
		$V_{CC}^+ = 30V$, $V_{CC}^- =$ Gnd, Vo = +30V, $R_L = 2K\Omega$		26		V	4, 5, 6

LM124 JAN AC ELECTRICAL CHARACTERISTICS

The following conditions apply to all the following parameters, unless otherwise specified.
AC: $+V_{CC} = 30V$, $-V_{CC} = 0V$.

SYMBOL	PARAMETER	CONDITIONS	NOTES	MIN	MAX	UNIT	SUB GROUPS
TR_{TR}	Transient Response: Rise Time	V_{CC}^+ = 30V, V_{CC}^-= Gnd			1.0	µS	7, 8A, 8B
TR_{OS}	Transient Response: Overshoot	V_{CC}^+ = 30V, V_{CC}^-= Gnd			50	%	7, 8A, 8B
$\pm S_R$	Slew Rate: Rise/Fall	V_{CC}^+ = 30V, V_{CC}^-= Gnd		0.1		V/µS	7, 8A, 8B
NI_{BB}	Noise Broadband	V_{CC}^+ = 15V, V_{CC}^-= -15V, BW = 10Hz to 5KHz			15	µV/rms	7
NI_{PC}	Noise Popcorn	V_{CC}^+ = 15V, V_{CC}^-= -15V, Rs = 20KΩ			50	µV/pK	7
C_S	Channel Separation	V_{CC}^+ = 30V, V_{CC}^-= Gnd, V_{IN} = 1V and 16V, R_L = 2KΩ		80		dB	7

LM124 JAN DC — DRIFT VALUES

“Delta calculations performed on JAN S and QMLV devices at group B, subgroup 5 only”

SYMBOL	PARAMETER	CONDITIONS	NOTES	MIN	MAX	UNIT	SUB GROUPS
V_{IO}	Input Offset Voltage	V_{CC}^+ = 30V, V_{CC}^-= Gnd, V_{CM} = +15V		-1.0	1.0	mV	1
$\pm I_{IB}$	Input Bias Current	V_{CC}^+ = 30V, V_{CC}^-= Gnd, V_{CM} = +15V		-15	15	nA	1

LM124A JAN DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	NOTES	MIN	MAX	UNIT	SUB GROUPS
V_{IO}	Input Offset Voltage	V_{CC}^+ = 30V, V_{CC}^- = Gnd, V_{CM} = +15V		-2.0	2.0	mV	1
				-4.0	4.0	mV	2, 3
		V_{CC}^+ = 2V, V_{CC}^-= -28V, V_{CM} = −13V		-2.0	2.0	mV	1
				-4.0	4.0	mV	2, 3
		V_{CC}^+ = 5V, V_{CC}^-= Gnd, V_{CM} = +1.4V		-2.0	2.0	mV	1
				-4.0	4.0	mV	2, 3
		V_{CC}^+ = 2.5V, V_{CC}^-= -2.5V, V_{CM} =−1.1V		-2.0	2.0	mV	1
				-4.0	4.0	mV	2, 3
I_{IO}	Input Offset Current	V_{CC}^+ = 30V, V_{CC}^-= Gnd, V_{CM} = +15V		-10	10	nA	1, 2
				-30	30	nA	3
		V_{CC}^+ = 2V, V_{CC}^-= -28V, V_{CM} = −13V		-10	10	nA	1, 2
				-30	30	nA	3
		V_{CC}^+ = 5V, V_{CC}^-= Gnd, V_{CM} = +1.4V		-10	10	nA	1, 2
				-30	30	nA	3
		V_{CC}^+ = 2.5V, V_{CC}^-= -2.5V, V_{CM} = −1.1V		-10	10	nA	1, 2
				-30	30	nA	3
$\pm I_{IB}$	Input Bias Current	V_{CC}^+ = 30V, V_{CC}^-= Gnd, V_{CM} = +15V		-50	+0.1	nA	1, 2
				-100	+0.1	nA	3
		V_{CC}^+ = 2V, V_{CC}^- = -28V, V_{CM} = −13V		-50	+0.1	nA	1, 2
				-100	+0.1	nA	3
		V_{CC}^+ = 5V, V_{CC}^-= Gnd, V_{CM} = +1.4V		-50	+0.1	nA	1, 2
				-100	+0.1	nA	3
		V_{CC}^+ = 2.5V, V_{CC}^-= -2.5V, V_{CM} = −1.1V		-50	+0.1	nA	1, 2
				-100	+0.1	nA	3

LM124A JAN DC ELECTRICAL CHARACTERISTICS (continued)

SYMBOL	PARAMETER	CONDITIONS	NOTES	MIN	MAX	UNIT	SUB GROUPS
+PSRR	Power Supply Rejection Ratio	V_{CC}^-= Gnd, V_{CM} = -1.4V, 5V ≤ V_{CC} ≤ 30V		-100	100	µV/V	1, 2, 3
CMRR	Common Mode Rejection Ratio		See[1]	76		dB	1, 2, 3
I_{OS}+	Output Short Circuit Current	V_{CC}^+ = 30V, V_{CC} - = Gnd, V_O = +25V		-70		mA	1, 2, 3
I_{CC}	Power Supply Current	V_{CC}^+ = 30V, V_{CC} - = Gnd			3.0	mA	1, 2
					4.0	mA	3
Delta V_{IO}/ Delta T	Input Offset Voltage Temperature Sensitivity	+25°C ≤ T_A ≤ +125°C, V_{CC}^+ = 5V, V_{CC}^-= 0V, V_{CM} = +1.4V		-30	30	µV/°C	2
		-55°C ≤ T_A ≤ +25°C, V_{CC}^+ = 5V, V_{CC}^-= 0V, V_{CM} = +1.4V		-30	30	µV/°C	3
Delta I_{IO} / Delta T	Input Offset Current Temperature Sensitivity	+25°C ≤ T_A ≤ +125°C, V_{CC}^+ = 5V, V_{CC}^-= 0V, V_{CM} = +1.4V		-400	400	pA/°C	2
		-55°C ≤ T_A ≤ +25°C, V_{CC}^+ = 5V, V_{CC}^-= 0V, V_{CM} = +1.4V		-700	700	pA/°C	3
V_{OL}	Logical "0" Output Voltage	V_{CC}^+ = 30V, V_{CC}^-= Gnd, R_L = 10KΩ			35	mV	4, 5, 6
		V_{CC}^+ = 30V, V_{CC}^-= Gnd, I_{OL} = 5mA			1.5	V	4, 5, 6
		V_{CC}^+ = 4.5V, V_{CC}^-= Gnd, I_{OL} = 2µA			0.4	V	4, 5, 6
V_{OH}	Logical "1" Output Voltage	V_{CC}^+ = 30V, V_{CC}^- = Gnd, I_{OH} = -10mA		27		V	4, 5, 6
		V_{CC}+ = 4.5V, V_{CC}- = Gnd, I_{OH} = -10mA		2.4		V	4, 5
				2.3		V	6
A_{VS}^+	Voltage Gain	V_{CC}^+ = 30V, V_{CC}^- = Gnd, 1V ≤ V_O ≤ 26V, R_L = 10KΩ		50		V/mV	4
				25		V/mV	5, 6
		V_{CC}^+ = 30V, V_{CC}^-= Gnd, 5V ≤ V_O ≤ 20V, R_L = 2KΩ		50		V/mV	4
				25		V/mV	5, 6
A_{VS}	Gain Voltage	V_{CC}^+ = 5V, V_{CC}^-= Gnd, 1V ≤ V_O ≤ 2.5V, R_L = 10KΩ		10		V/mV	4, 5, 6
		V_{CC}^+ = 5V, V_{CC}^- = Gnd, 1V ≤ V_O ≤ 2.5V, R_L = 2KΩ		10		V/mV	4, 5, 6
+V_{OP}	Maximum Output Voltage Swing	V_{CC}^+ = 30V, V_{CC}^-= Gnd, V_O = +30V, R_L = 10KΩ		27		V	4, 5, 6
		V_{CC}^+ = 30V, V_{CC}^- = Gnd, V_O = +30V, R_L = 2KΩ		26		V	4, 5, 6

(1) The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is V^+ − 1.5V (at 25°C), but either or both inputs can go to +32V without damage independent of the magnitude of V^+.

LM124A JAN AC ELECTRICAL CHARACTERISTICS

The following conditions apply to all the following parameters, unless otherwise specified.

AC: $+V_{CC} = 30V$, $-V_{CC} = 0V$

SYMBOL	PARAMETER	CONDITIONS	NOTES	MIN	MAX	UNIT	SUB GROUPS
TR_{TR}	Transient Response: Rise Time	$V_{CC}^{+} = 30V$, V_{CC}^{-}= Gnd			1.0	µS	7, 8A, 8B
TR_{OS}	Transient Response: Overshoot	$V_{CC}^{+} = 30V$, V_{CC}^{-}= Gnd			50	%	7, 8A, 8B
$\pm S_R$	Slew Rate: Rise/Fall	$V_{CC}^{+} = 30V$, V_{CC}^{-}= Gnd		0.1		V/µS	7, 8A, 8B
NI_{BB}	Noise Broadband	$V_{CC}^{+} = 15V$, $V_{CC}^{-} = -15V$, BW = 10Hz to 5KHz			15	µV/rms	7
NI_{PC}	Noise Popcorn	$V_{CC}^{+} = 15V$, $V_{CC}^{-} = -15V$, Rs = 20KΩ BW = 10Hz to 5KHz			50	µV/pK	7
C_S	Channel Separation	$V_{CC}^{+} = 30V$, V_{CC}^{-}= Gnd R_L = 2KΩ		80		dB	7
		$V_{CC}^{+} = 30V$, V_{CC}^{-}= Gnd, V_{IN} = 1V and 16V, R_L = 2KΩ		80		dB	7

LM124A JAN DC — DRIFT VALUES

"Delta calculations performed on JAN S and QMLV devices at group B, subgroup 5 only"

Symbol	PARAMETER	CONDITIONS	NOTES	MIN	MAX	UNIT	SUB GROUPS
V_{io}	Input Offset Voltage	$V_{cc}^{+} = 30V$, V_{cc}^{-}= Gnd, $V_{cm} = +15V$		-0.5	0.5	mV	1
$\pm i_{ib}$	Input Bias Current	$V_{cc}^{+} = 30V$, V_{cc}^{-}= Gnd, $V_{cm} = +15V$		-10	10	nA	1

TYPICAL PERFORMANCE CHARACTERISTICS

Input Voltage Range

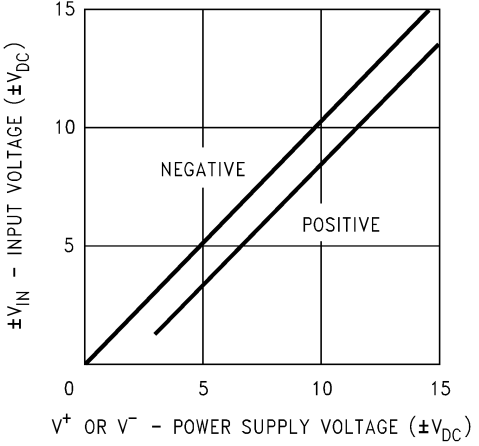


Figure 1.

Input Current

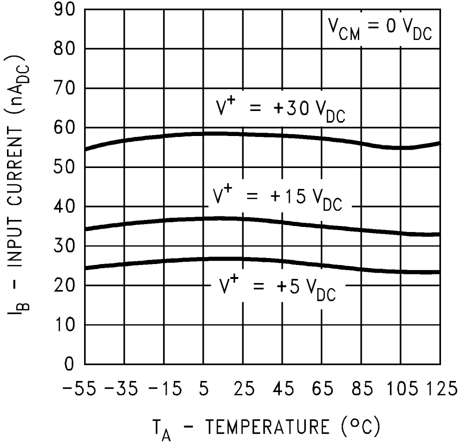


Figure 2.

Supply Current

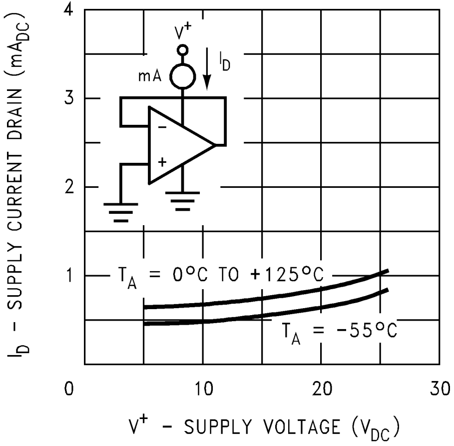


Figure 3.

Voltage Gain

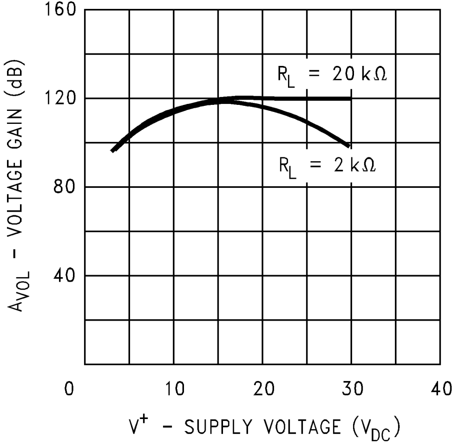


Figure 4.

Open Loop Frequency Response

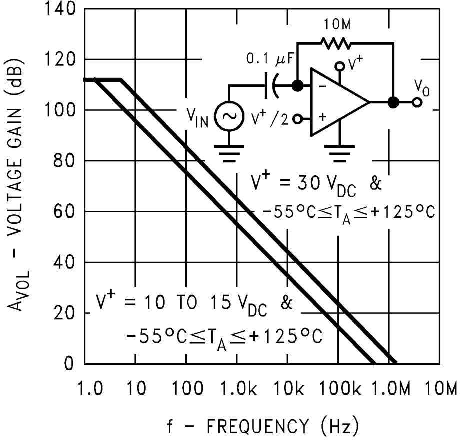


Figure 5.

Common Mode Rejection Ratio

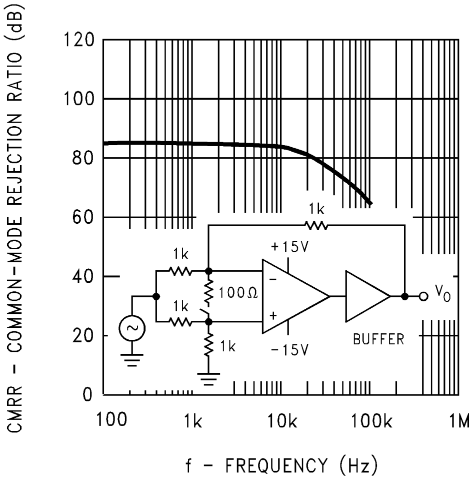
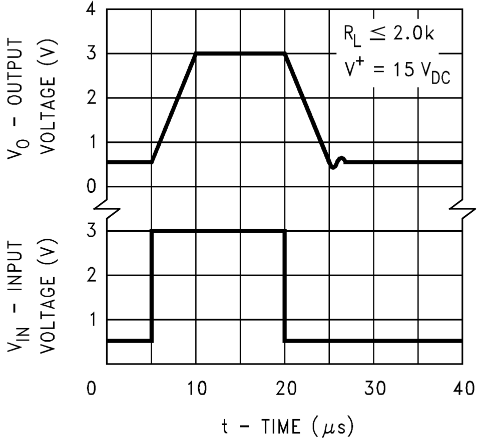


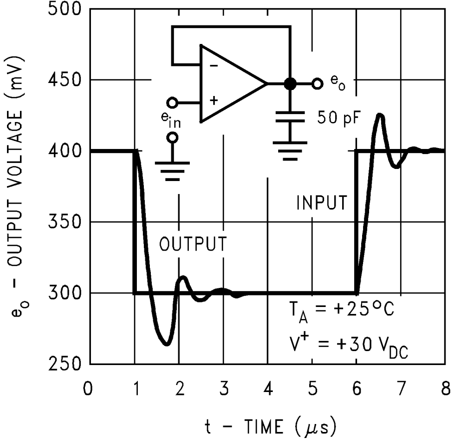
Figure 6.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)



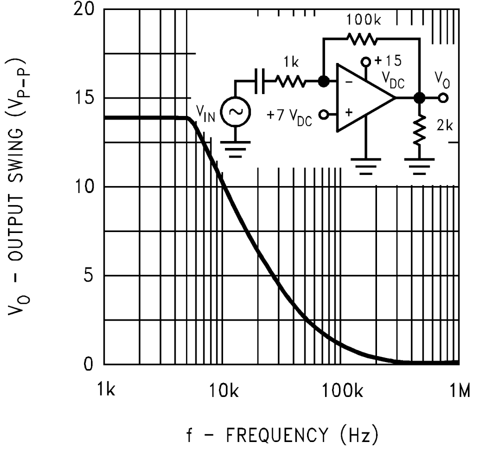
Voltage Follower Pulse Response

Figure 7.



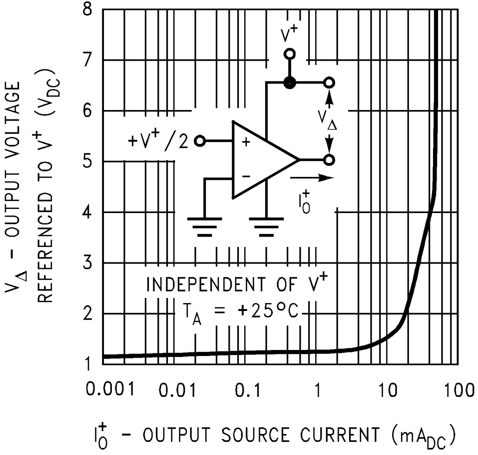
Voltage Follower Pulse Response (Small Signal)

Figure 8.



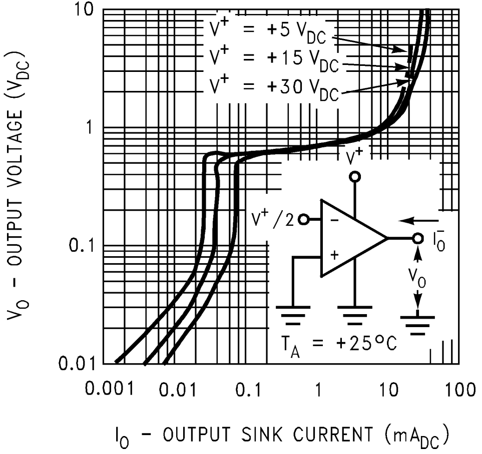
Large Signal Frequency Response

Figure 9.



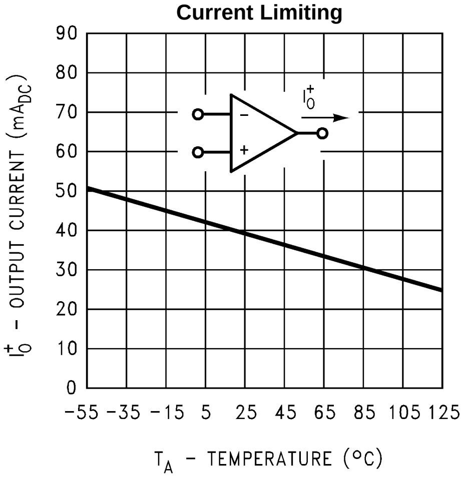
Output Characteristics Current Sourcing

Figure 10.



Output Characteristics Current Sinking

Figure 11.



Current Limiting

Figure 12.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Input Current (LM2902 only)

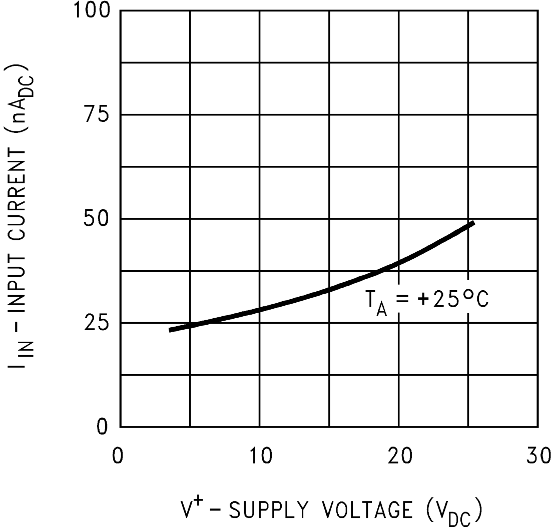


Figure 13.

Voltage Gain (LM2902 only)

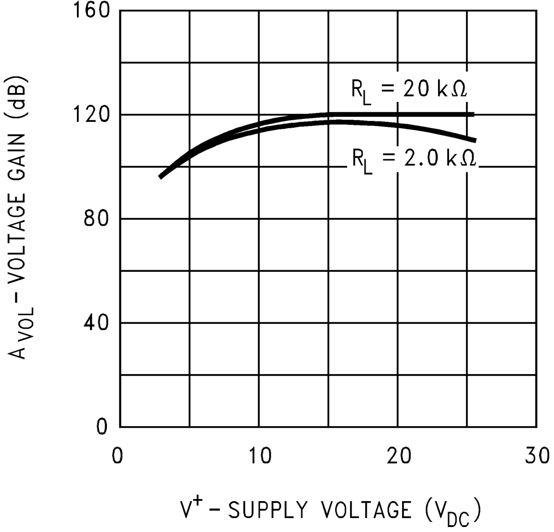


Figure 14.

APPLICATION HINTS

The LM124MIL series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

The pinouts of the package have been designed to simplify PC board layouts. Inverting inputs are adjacent to outputs for all of the amplifiers and the outputs have also been placed at the corners of the package (pins 1, 7, 8, and 14).

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion.

Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

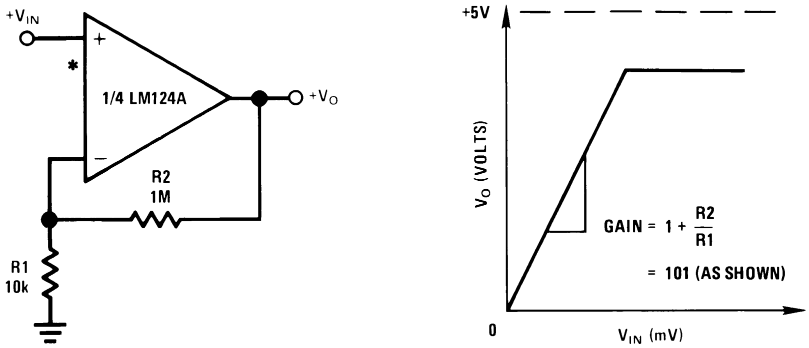
The bias network of the LM124MIL establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 3 V_{DC} to 30 V_{DC}.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see TYPICAL PERFORMANCE CHARACTERISTICS) than a standard IC op amp.

The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

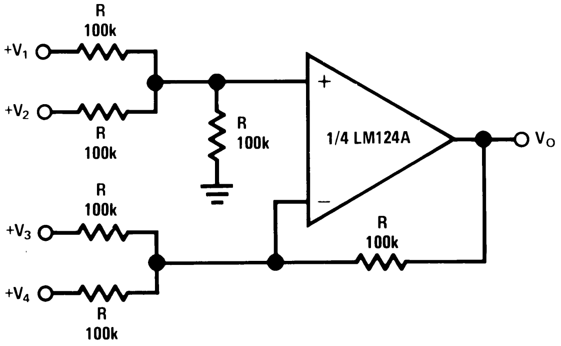
Typical Single-Supply Applications

($V^+ = 5.0\ V_{DC}$)



*R not needed due to temperature independent I_{IN}

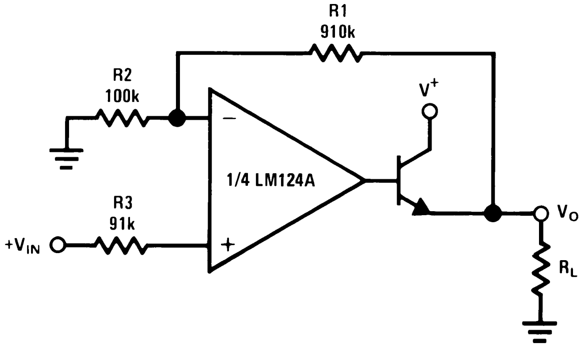
Figure 15. Non-Inverting DC Gain (0V Input = 0V Output)



Where: $V_0 = V_1 + V_2 - V_3 - V_4$

$(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0\ V_{DC}$

Figure 16. DC Summing Amplifier
($V_{IN'S} \geq 0\ V_{DC}$ and $V_O \geq V_{DC}$)



$V_0 = 0\ V_{DC}$ for $V_{IN} = 0\ V_{DC}$

$A_V = 10$

Figure 17. Power Amplifier

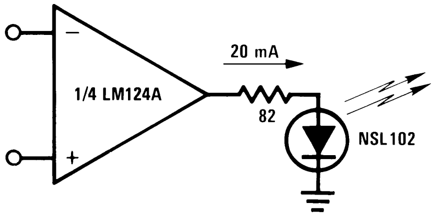
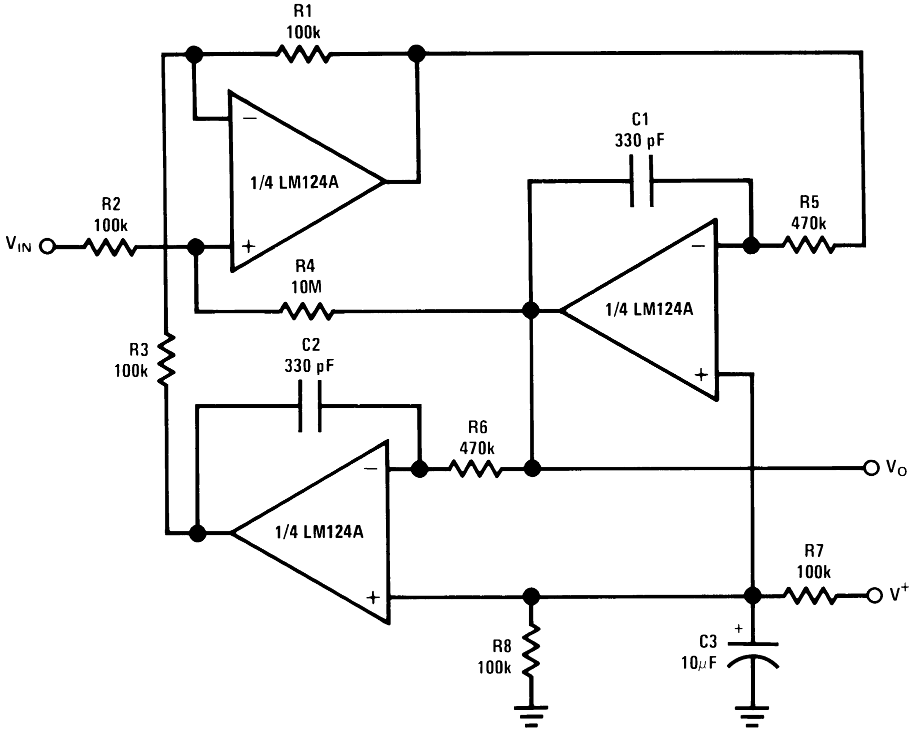
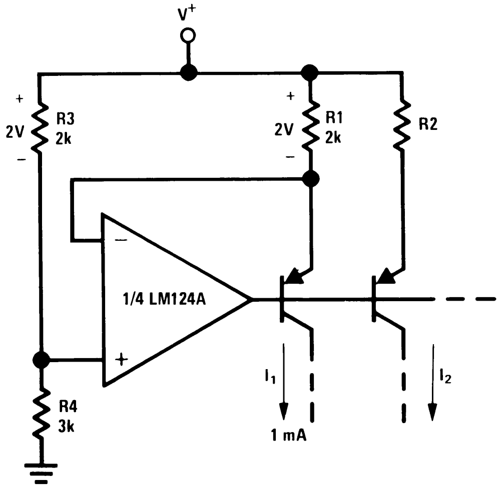


Figure 18. LED Driver



f_o = 1 kHz
Q = 50
A_V = 100 (40 dB)

Figure 19. “BI-QUAD” RC Active Bandpass Filter



$$I_2 = \left(\frac{R1}{R2}\right) I_1$$

Figure 20. Fixed Current Sources

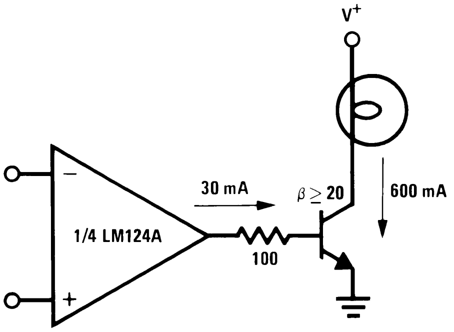
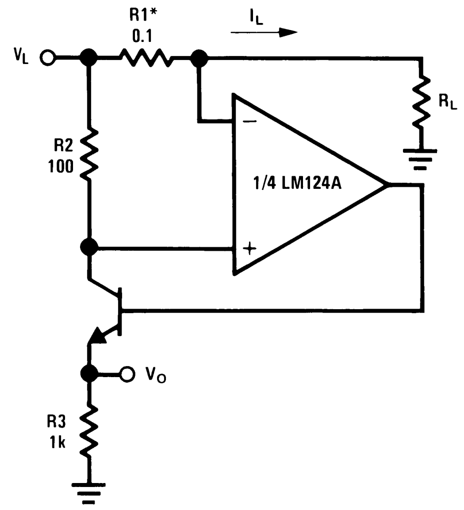


Figure 21. Lamp Driver



$$V_O = \frac{1V(I_L)}{1A}$$

$$V_L \leq V^+ - 2V$$

*(Increase R1 for I_L small)

Figure 22. Current Monitor

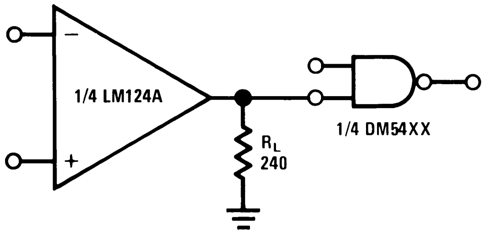


Figure 23. Driving TTL

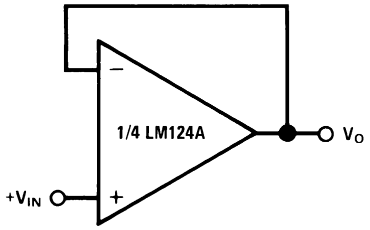


Figure 24. Voltage Follower

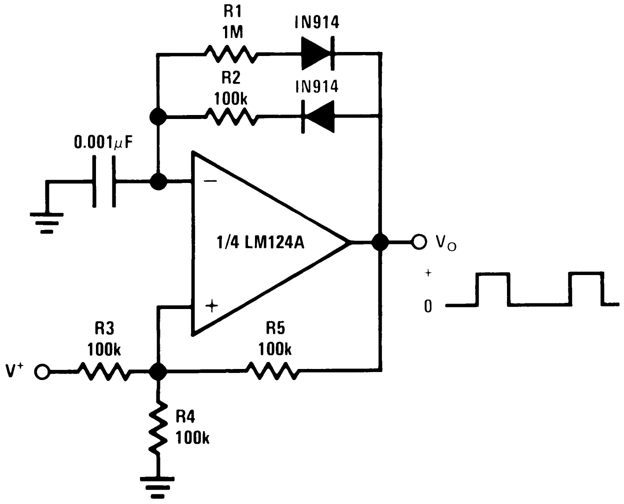


Figure 25. Pulse Generator

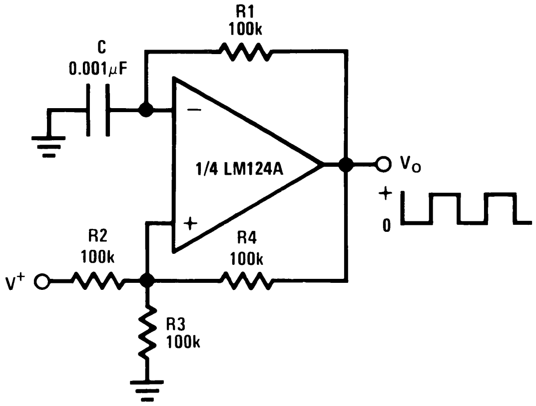


Figure 26. Squarewave Oscillator

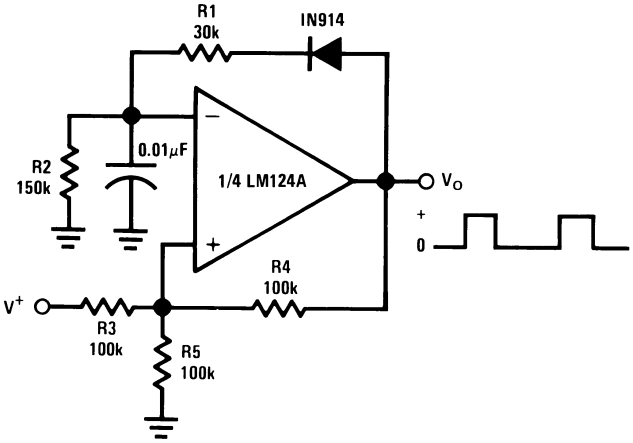
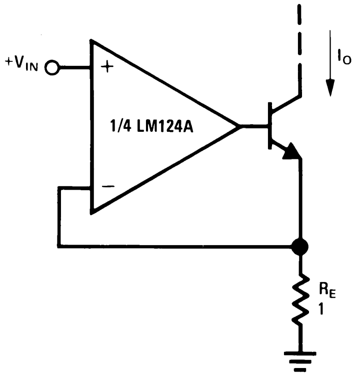


Figure 27. Pulse Generator



I_O = 1 amp/volt V_{IN}
(Increase R_E for I_o small)

Figure 28. High Compliance Current Sink

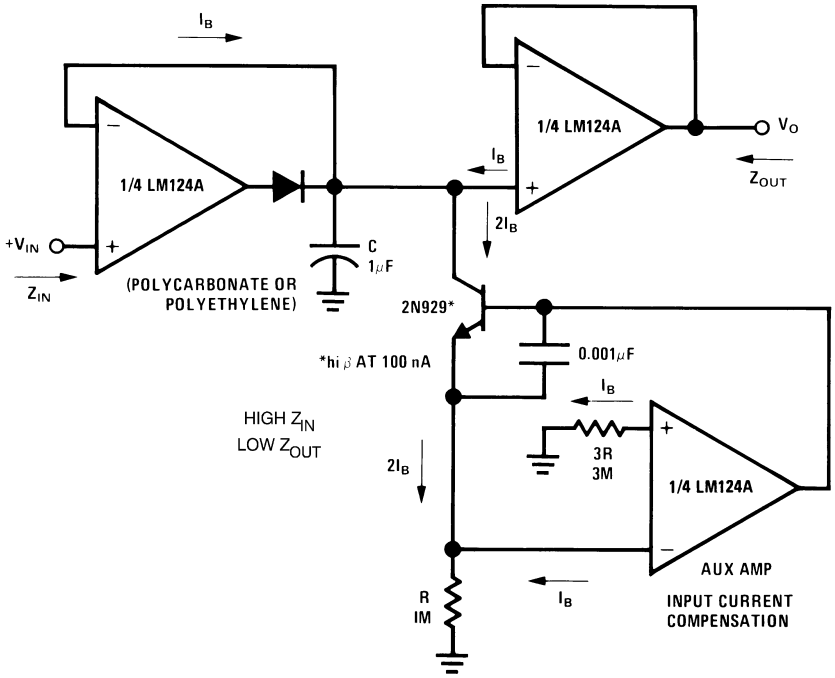


Figure 29. Low Drift Peak Detector

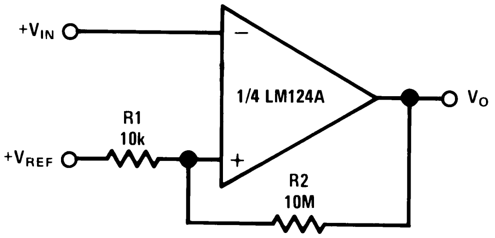
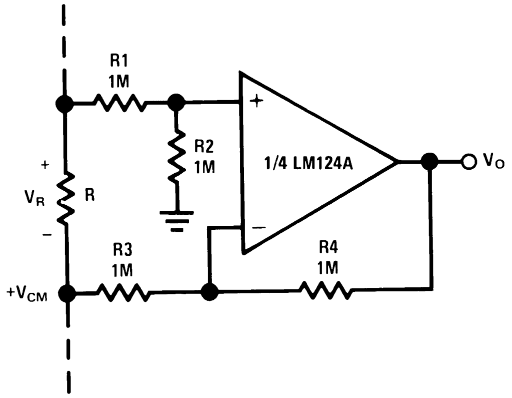
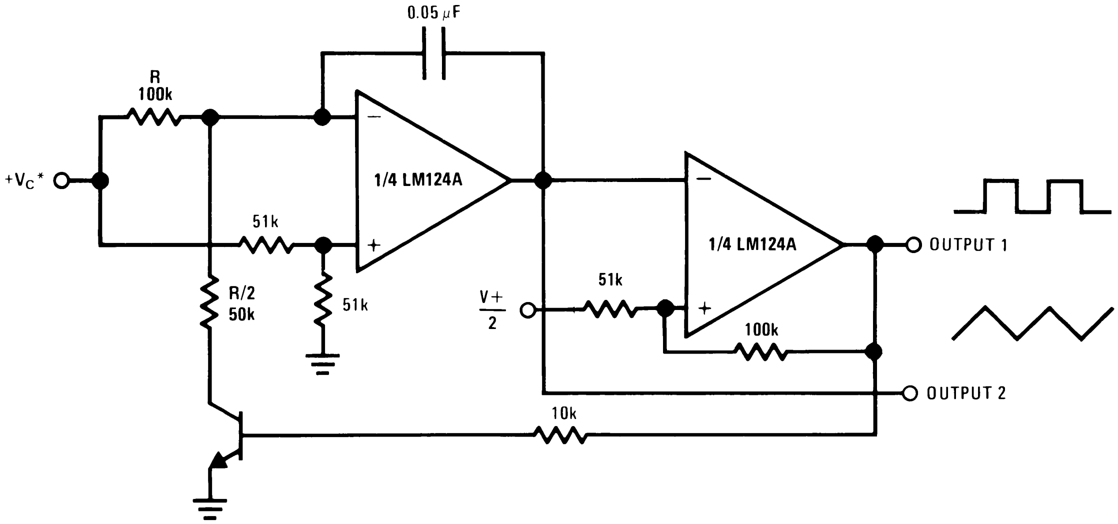


Figure 30. Comparator with Hysteresis



$V_O = V_R$

Figure 31. Ground Referencing a Differential Input Signal



*Wide control voltage range: 0 $V_{DC} \leq V_C \leq 2$ (V^+ −1.5 V_{DC})

Figure 32. Voltage Controlled Oscillator Circuit

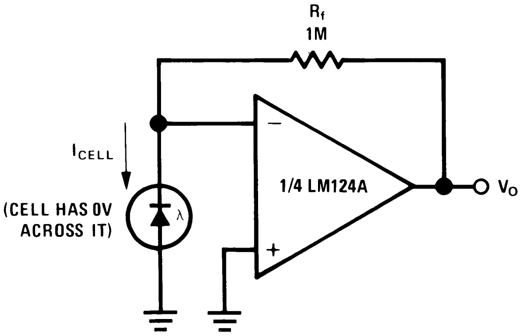
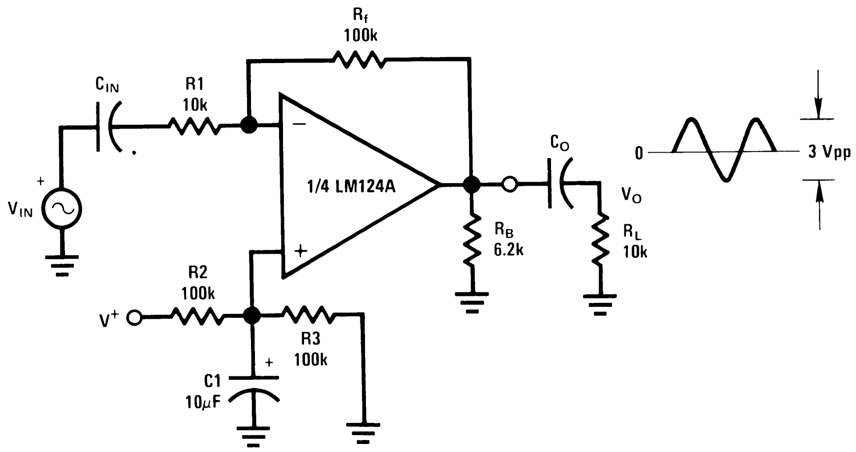
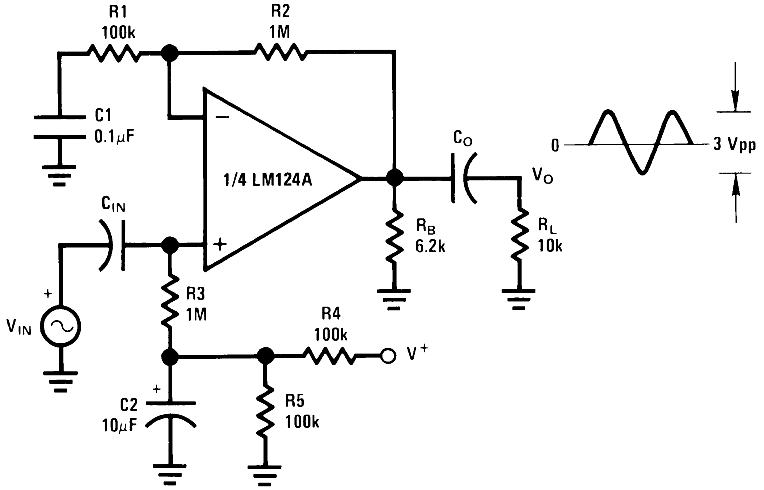


Figure 33. Photo Voltaic-Cell Amplifier



$$A_V = \frac{R_f}{R1} \text{ (As shown, } A_V = 10\text{)}$$

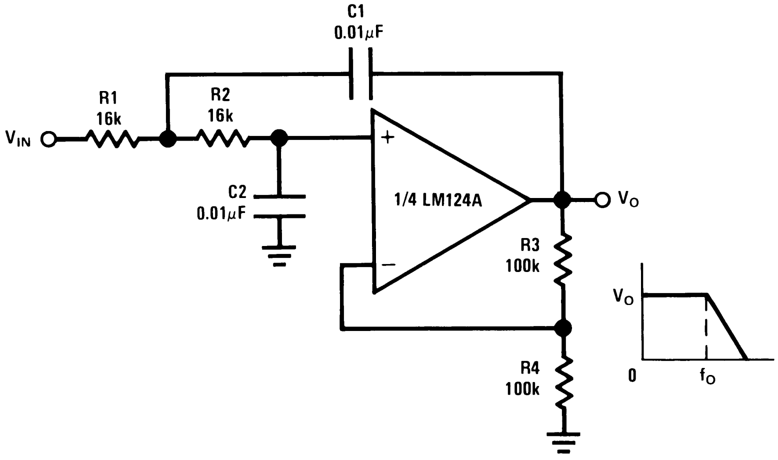
Figure 34. AC Coupled Inverting Amplifier



$$A_V = 1 + \frac{R2}{R1}$$

$$A_V = 11 \text{ (As shown)}$$

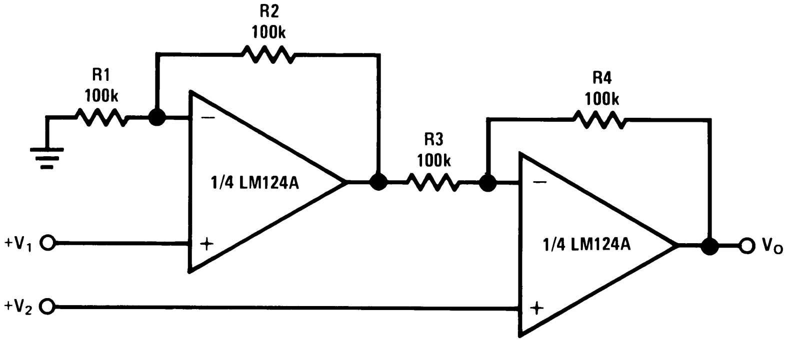
Figure 35. AC Coupled Non-Inverting Amplifier



f_O = 1 kHz
Q = 1
A_V = 2

Figure 36. DC Coupled Low-Pass RC Active Filter

Figure 37.

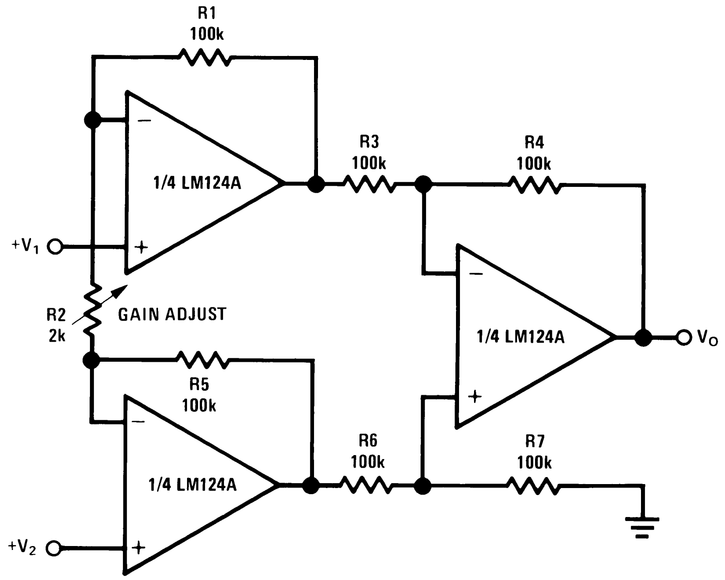


For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

$$V_O = 1 + \frac{R4}{R3}(V_2 - V_1)$$

As shown: $V_O = 2(V_2 - V_1)$

Figure 38. High Input Z, DC Differential Amplifier



If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

$$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$$

As shown $V_O = 101\,(V_2 - V_1)$

Figure 39. High Input Z Adjustable-Gain DC Instrumentation Amplifier

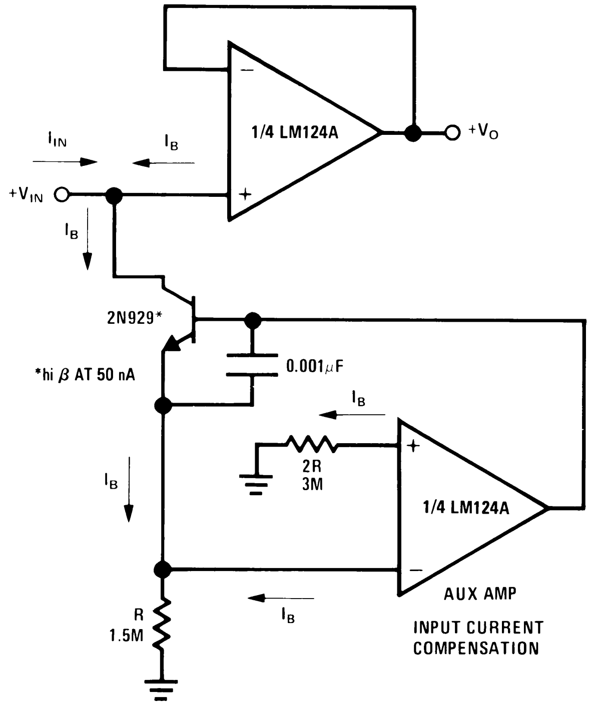
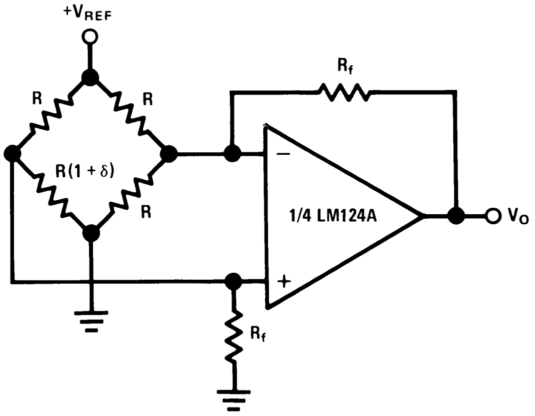


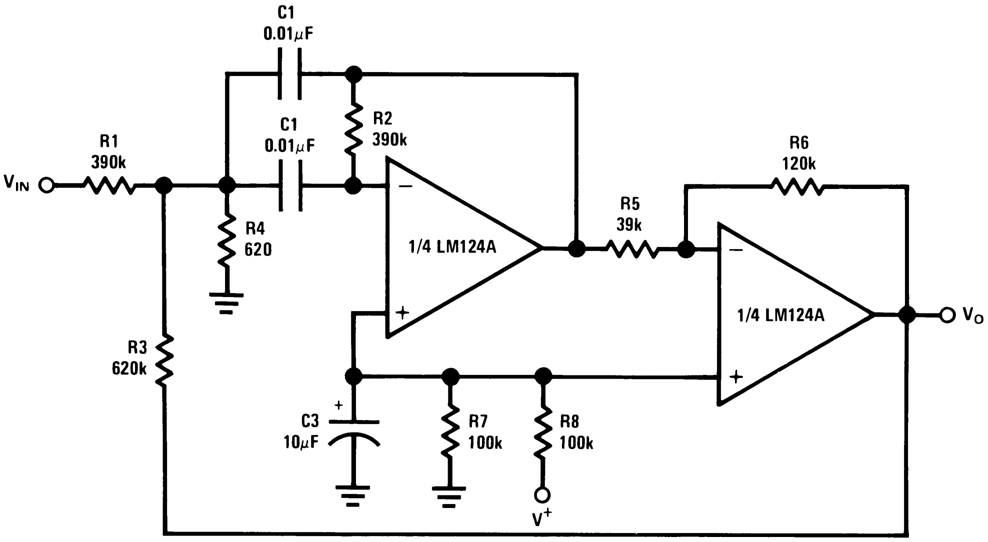
Figure 40. Using Symmetrical Amplifiers to Reduce Input Current (General Concept)



For δ < < 1 and R_f > > R

$$V_O \cong V_{REF}\left(\frac{\delta}{2}\right)\frac{R_f}{R}$$

Figure 41. Bridge Current Amplifier



f_O = 1 kHz
Q = 25

Figure 42. Bandpass Active Filter

REVISION HISTORY

Date Released	Revision	Section	Changes
01/27/05	A	New Released, Corporate format	2 MDS data sheets converted into one Corp. data sheet format. MJLM124–X, Rev. 1B1 and MJLM124A-X, Rev. 2A1. MDS data sheets will be archived.
04/18/05	B	Update Absolute Maximum Ratings Section	Corrected typo for Supply Voltage limit From: 32Vdc or +18Vdc TO: 32Vdc or ±18Vdc. Added Cerdip package weight.
09/27/2010	C	Obsolete Data Sheet	End Of Life on Product/NSID Dec. 2008/2009

Changes from Revision E (April 2013) to Revision F **Page**

- Changed layout of National Data Sheet to TI format 24

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