FPD87208AXA +2.5V Low EMI, Low Dynamic Power XGA/WXGA TFT-LCD Timing Controller with Reduced Swing Differential Signaling RSDS™ Outputs

Check for Samples: FPD87208

FEATURES

- **Reduced Swing Differential Signaling (RSDS) Digital Bus Reduces Dynamic Power, EMI and Bus-Width from the Timing Controller**
- **LVDS Single Pixel Input Interface System**
- **Input Clock Range from 25 MHz to 85 MHz**
- **Drives RSDS Column Drivers at 170 Mb/s with an 85 MHz Clock (Max)**
- **BIST Function**
- **CMOS Circuitry Operates from a 2.25V–2.75V; 0°C–70°C**
- **64 TQFP Package with Body Size 10 mm x 10 mm x 1.0 mm**

DESCRIPTION

The FPD87208AXA is a timing controller that combines an LVDS single pixel input interface with TI Reduced Swing Differential Signaling (RSDS™) output driver interface for XGA and Wide XGA resolutions. It resides on the TFT-LCD panel and provides the data buffering and control signal generation for XGA, and Wide XGA graphic modes. The RSDS path to the column driver contributes toward lowering radiated EMI and reducing system dynamic power consumption.

This single RSDS bus conveys the 6-bit color data for XGA, and three different WXGA resolutions.

System Diagram

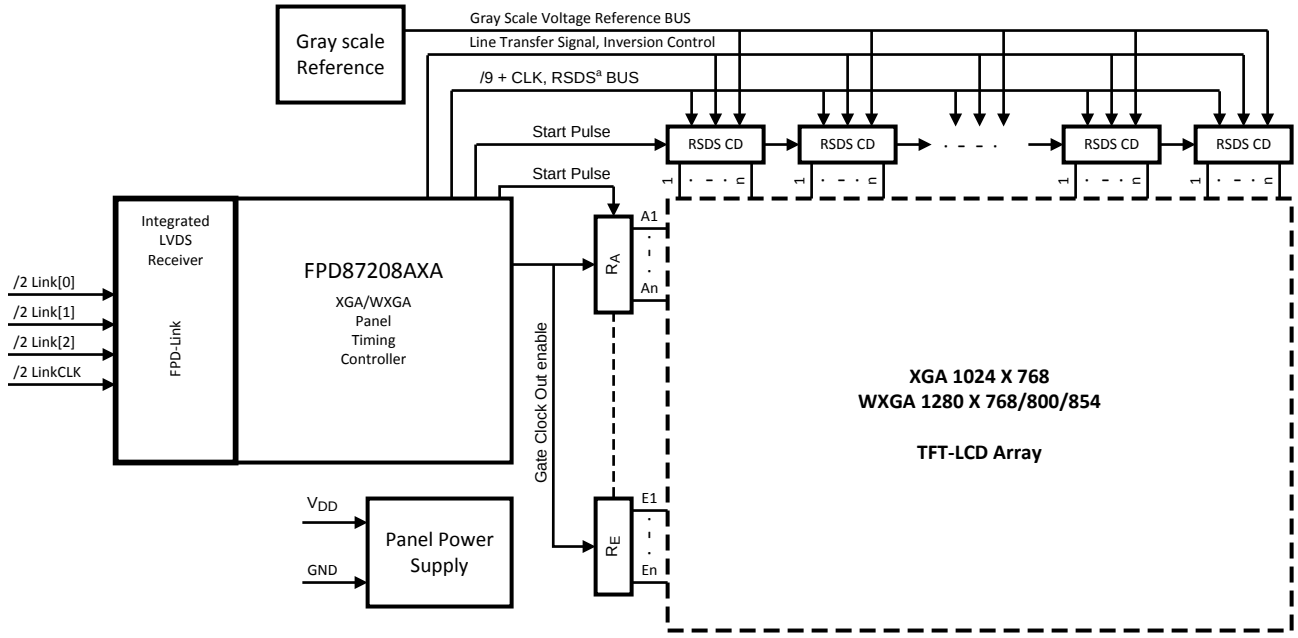

Figure 1. Block Diagram of the LCD Module

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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Absolute Maximum Ratings (1)(2)

Supply Voltage (V_{DD})		−0.3V to +3.0V
DC TTL Input Voltage (V_{IN})		−0.3V to (V_{DD} + 0.3V)
DC LVDS Input Voltage (V_{IN})		−0.3V to (V_{DD} + 0.3V)
DC Output Voltage (V_{OUT})		−0.3V to (V_{DD} + 0.3V)
Junction Temperature		+150°C
Storage Temperature Range (T_{STG})		−65°C to +150°C
Lead Temperature (T_L) (Soldering 10 sec.)		260°C
ESD Rating	HBM: R_{ZAP} = 1.5 kΩ, C_{ZAP} = 100 pF	2 kV
	MM: R_{ZAP} = 0Ω, C_{ZAP} = 200 pF	200V

(1) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The table of Electrical Characteristics specifies conditions of device operation.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{DD})	2.25	2.75	V
Operating Temp. Range (T_A)	0	70	°C
Supply Noise Voltage		200	mV_{PP}

DC Electrical Characteristics TTL DC Electrical Characteristics

V_{DD} = 2.5V ±0.25V, T_A = 0°C to 70°C, I_{PI} = 100 µA (Unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Supply Voltage		2.25	2.5	2.75	
V_{IH}	Minimum Input High Voltage		1.8			V
V_{IL}	Maximum Input Low Voltage				0.7	V
V_{OH}	Output High Voltage	I_{OH} = −8 mA	0.8 x V_{DD}			
V_{OL}	Output Low Voltage	I_{OL} = 8 mA			0.4	
I_{IN}	Input Current	V_{IN} = V_{DD}			10	µA
		V_{IN} = GND			10	µA
I_{DD}	Average Supply Current	CLK = 85 MHz, RPI = 12.3k $C_{L(TTL)}$ = 50 pF, $R_{L(RSDS)}$ = 100Ω and $C_{L(RSDS)}$ = 5 pF (jig & test fixture capacitance), See Figure 3 for input conditions		80 I_P = 100 µA V_{DD} = 2.5V	120 I_P = 100 µA V_{DD} = 2.75V	mA

DC Electrical Characteristics FPD-Link (LVDS) Receiver Input (RxCLKP/N; RxIN[y]P/N, y = 0,1,2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVDS RECEIVER DC SPECIFICATIONS **Note:** LVDS Receiver DC parameters are measured under Static and Steady state conditions which may not be reflective of its performance in the end application. This device is compatible with TIA644 SPEC. V0 and V2.4.						
V_{THLVDS}	Differential Input **H**igh **T**hreshold **V**oltage	V_{CM} = 1.2V			+100	mV
V_{TLLVDS}	Differential Input **L**ow **T**hreshold **V**oltage		−100			mV
I_{IN}	**IN**put Current	V_{IN} = V_{DD} –0.4V, V_{DD} = 2.75V			±10	µA
		V_{IN} = 0V, V_{DD} = 2.75V			±10	µA
V_{IN}	**IN**put **V**oltage Range		0		V_{DD} –0.4	V
$\|V_{ID}\|$	**D**ifferential **I**nput **V**oltage		0.100		0.600	V
V_{CM}	**C**ommon **M**ode **V**oltage Offset		0 + $\|V_{ID}\|/2$		(V_{DD} –0.4) − $\|V_{ID}\|/2$	V

LVDS V_{ID} and V_{CM} Allowable Operating Range

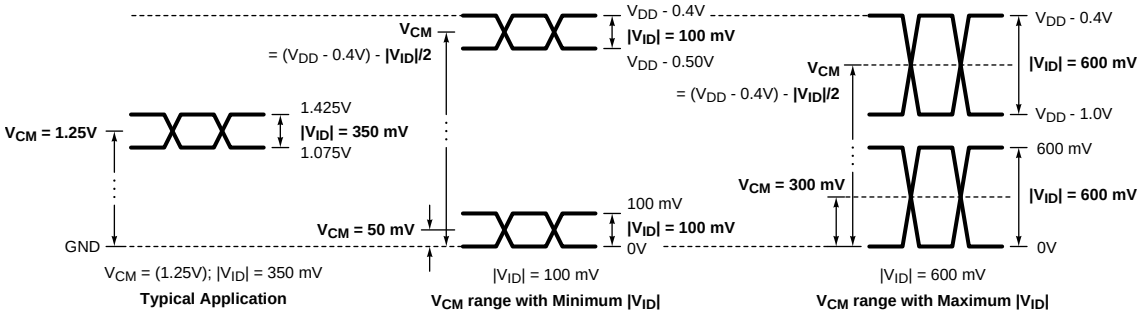


Figure 2. $|V_{ID}|$ and V_{CM} Definitions

FPD-Link Receiver Input Pattern Used to Measure I_{DD}

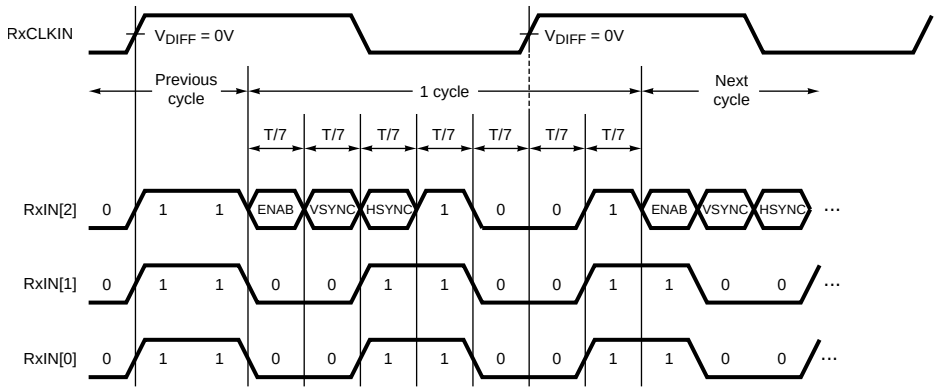


Figure 3. FPD-Link Receiver I_{DD} Pattern

DC Electrical Characteristics RSDS Output

(CLKP/N, xyP/N; x = R, G, B; y = 0, 1, 2), V_{DD} = 2.25V to 2.75V (Unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$\|V_{ODRSDS}\|$	Differential Output Voltage Typ.	R_L = 100Ω I_{PI} = 100 µA		200 (Figure 4)		mV
V_{OSRSDS}	Offset Voltage			1.2		V

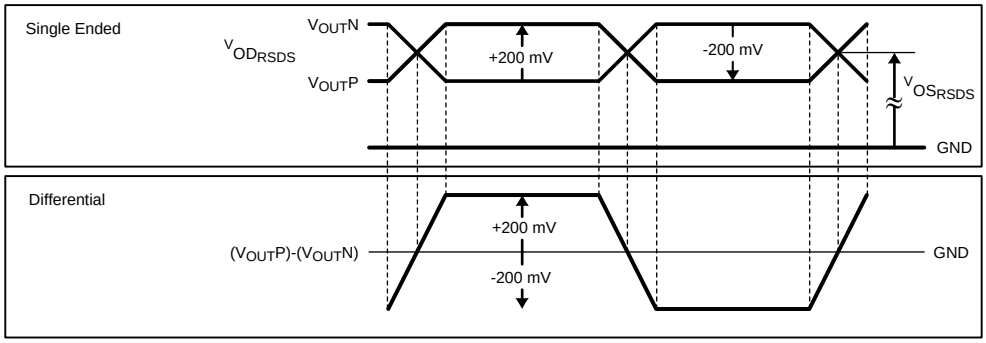


Figure 4. RSDS Output Waveforms: Single Ended vs Differential

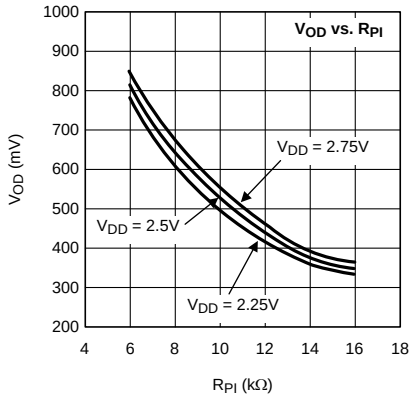


Figure 5. Typical RSDS V_{OD} vs R_{PI} Response Curve

DC Electrical Characteristics Schmitt Trigger

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_H	Hysteresis Voltage	$V_{T+} - V_{T-}$		0.4		V
V_{T-}	Hysteresis Low Threshold Voltage			1.2		V
V_{T+}	Hysteresis High Threshold Voltage			1.6		V
I_{INHYS}	Input Current	$V_{IN} = V_{DD}$			20	µA
		$V_{IN} = V_{SS}$	−20	0		µA

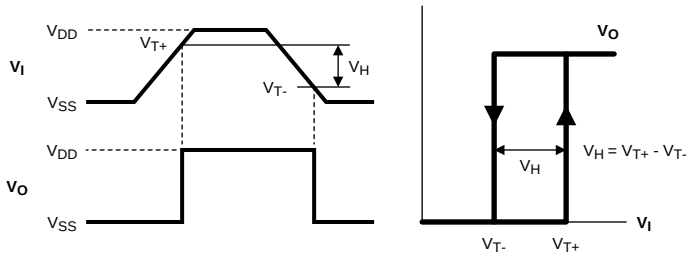


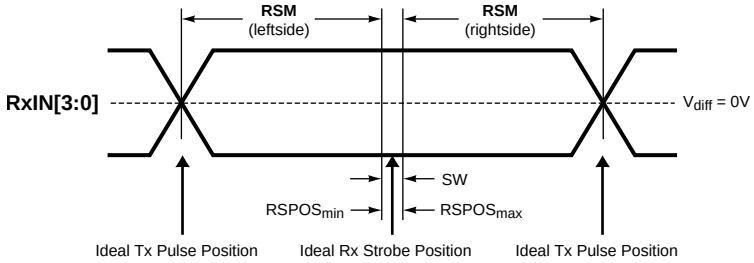
Figure 6. Hysteresis Definition

AC Electrical Characteristics
LVDS Data Input R_T = 100Ω, I_{PI} = 100 µA, f = 85 MHz (Unless otherwise specified)

T_A = 0°C to 70°C, V_{DD} = 2.5V ±0.25V, I_{PI} = 100 µA (Unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Units
F_{RXCLK}	RxCLK Frequency (LVDS)		25	85	MHz
RPLLS	FPD-Link Receiver Phase Lock Loop Wake-Up Time			10	ms
RMS	RxIN Strobe Margin(1) and (Figure 7)	F = 85 MHz	400		ps

(1) Receiver Strobe Margin is defined as the valid data sampling region at the receiver inputs.



Acronyms:
RSM **R**eceiver **S**trobe **M**argin
RSPOS **R**eceiver **S**trobe **Pos**ition
SW **S**trobe **W**idth

Definitions:
SW Setup and Hold Time (Internal data sampling window)

Figure 7. FPD-Link Receiver Input Skew Margin

Table 1. Ring Oscillator Characteristics R_T = 100Ω, I_{PI} = 100 µA, f = 85 MHz (Unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RESOSC	Ring Oscillator Clock Frequency	R = 14.5KΩ; V_{DD}= 2.5V		40		MHz

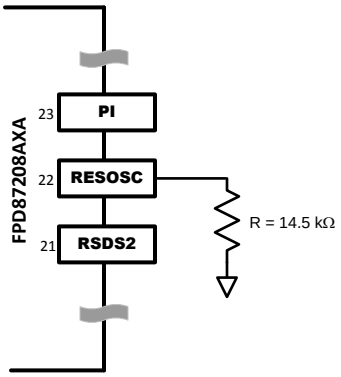


Figure 8. Application diagram of Ring Oscillator

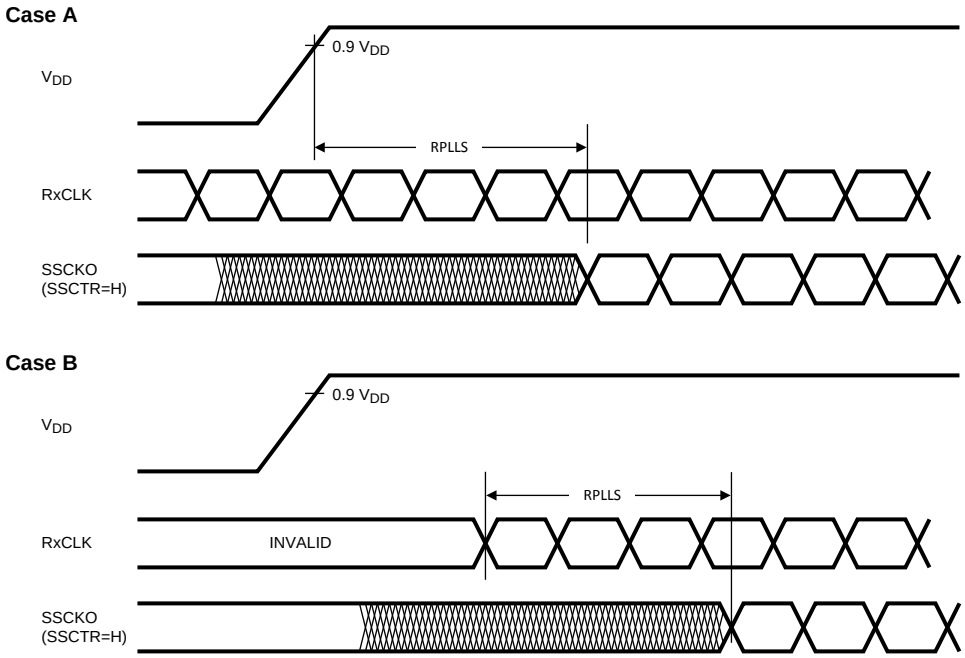
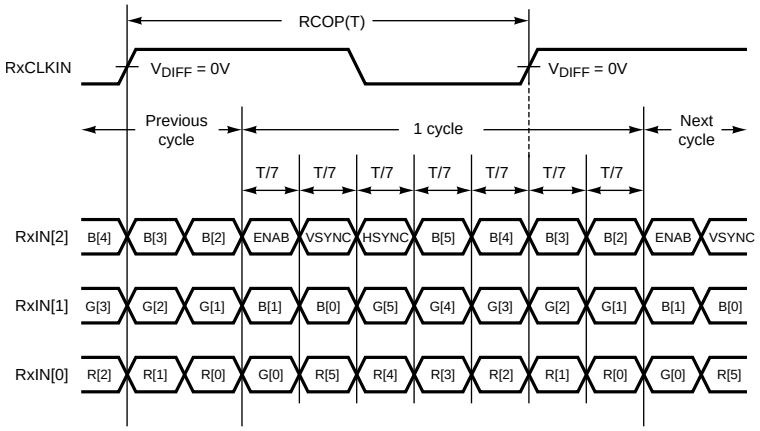


Figure 9. FPD-Link Receiver Phase Lock Loop Wake-Up Time



Note: R/G/B[7]s are MSBs and R/G/B[0]s are LSBs

Figure 10. FPD-Link Receiver Input Data Mapping

Table 2. Output Timing R_T = 100Ω, I_{PI} = 100 µA, f = 85 MHz (Unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RCHP	RSDS Clock (RSCK) High Period	$C_{L(RSDS)}$ = 5 pF		5.8		ns
RCLP	RSDS Clock (RSCK) Low Period	$C_{L(RSDS)}$ = 5 pF		5.8		ns
SPSTU	STH Rising to RSCK Falling	$C_{L(TTL)}$ = 15 pF	4.0			ns
SPHLD	STH Falling to RSCK Falling		4.0			ns
RSTU(1)	RSDS Setup to Falling or Rising Edge of RSCK	$C_{L(RSDS)}$ = 5 pF RSDS[2:0]=[011]		3.3		ns
RHLD(1)	RSDS Hold from Falling or Rising Edge of RSCK			2.1		ns

(1) Refer to the table “RSDS Setup and Hold Time with Data Skew Control Values” for each skew control.

Table 3. RSDS Setup and Hold Time with Data Skew Control Values—Reference Only (RxCLKP/N = 85 MHz, R_T = 100Ω, I_{PI} = 100 µA, V_{DD} = 2.5V; Duty Clock = 50%/50%, ±2%; 25°C)(1)

RSDS[2:0]	Setup Time (RSTU, nS)			Hold Time (RHLD, nS)			Units
	Min	Typ	Max	Min	Typ	Max	
000		1.83			3.61		ns
001		2.33			3.09		
010		2.83			2.61		
011		3.31			2.10		
100		3.85			1.55		
101		4.34			1.03		
110		4.81			0.53		
111		5.33			0.01		

(1) Typical values on this table are measured under Static and Steady state conditions which may not be reflective of its performance in the end application.

Table 4. RSDS and TTL Output Tr/Tf

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RSTr/RSTf	RSDS Output Rising/Falling Time (All RSDS Outputs)	$C_{L(RSDS)}$ = 5 pF		1.5		ns
TTL Tr/Tf	TTL Output Rising and Falling Time	C_L = 15 pF (20%–80%)		2.0		ns

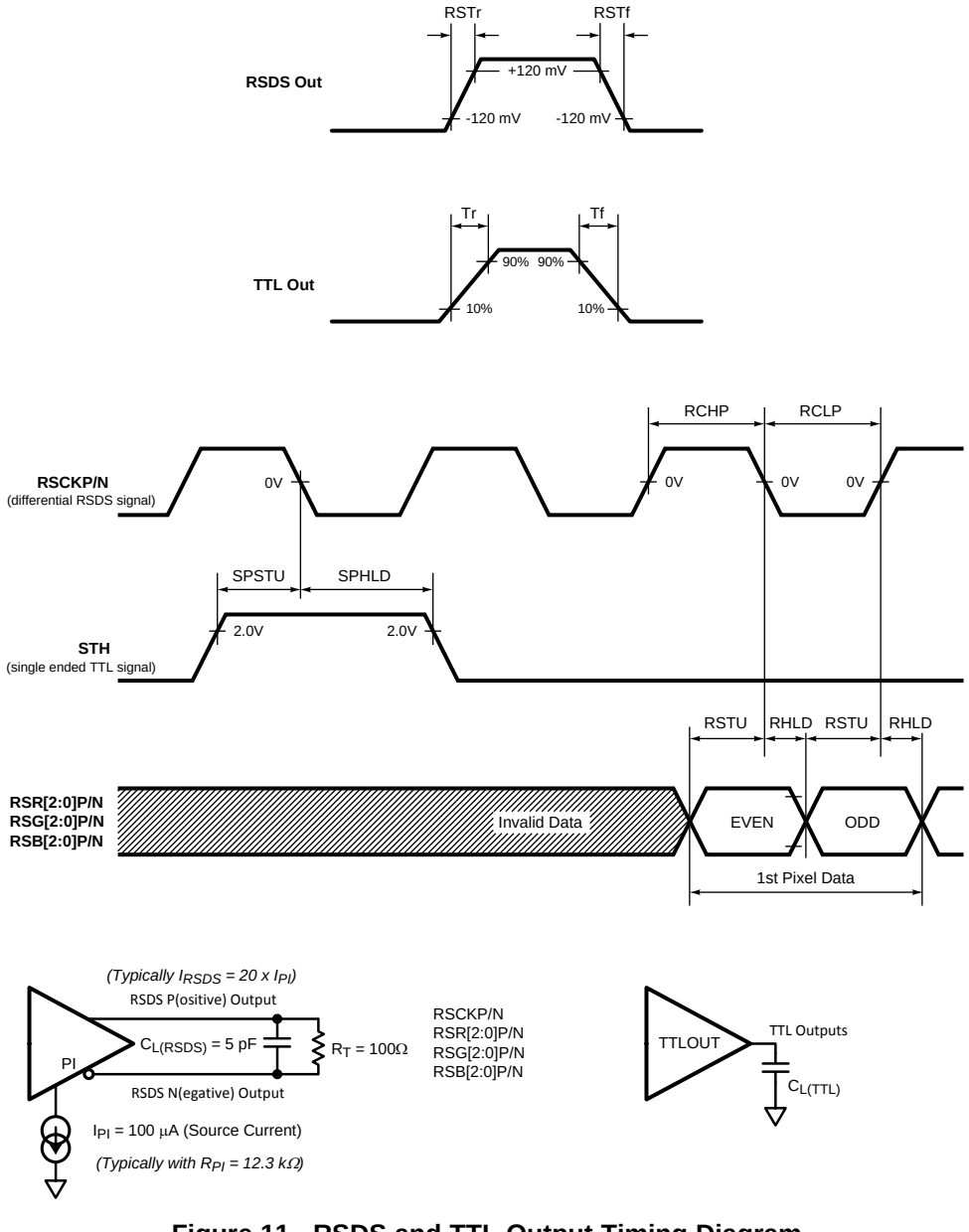
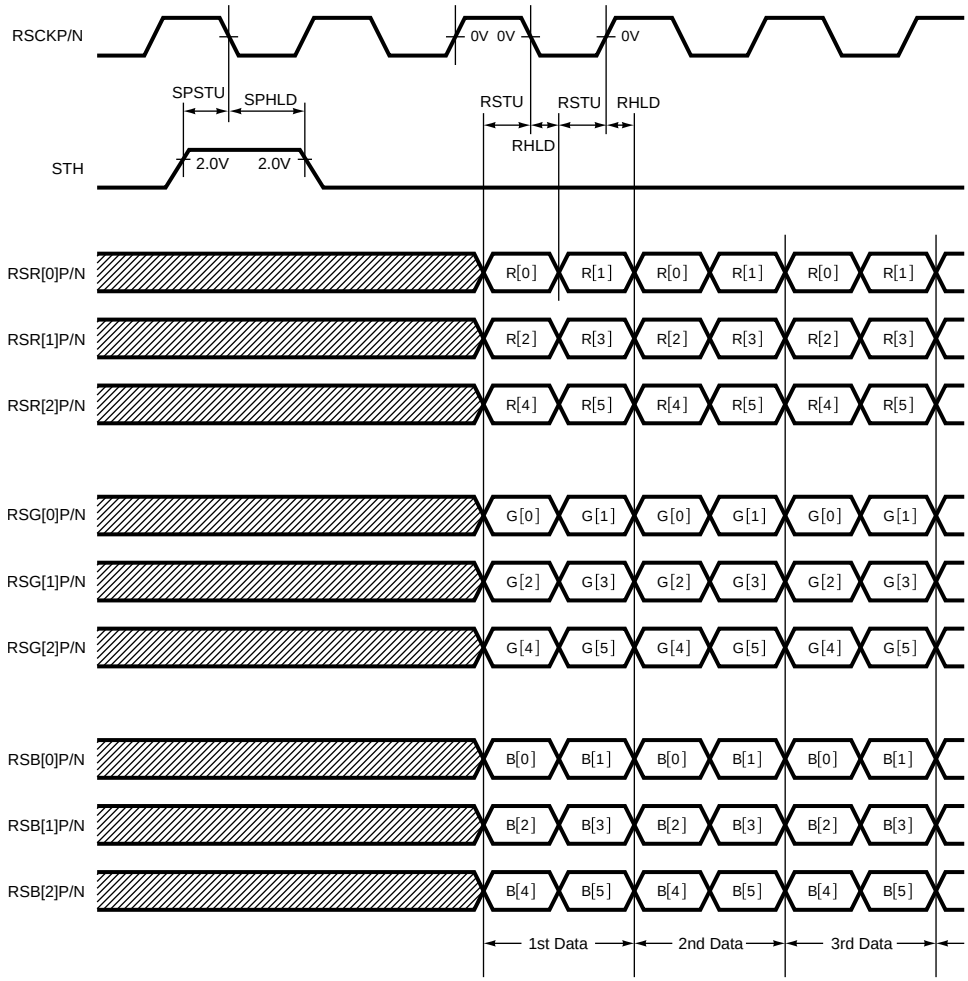


Figure 11. RSDS and TTL Output Timing Diagram



Note: RSCKP/N, RSR[2:0]P/N, RSG[2:0]P/N and RSB[2:0]P/N are differential outputs, STH is a single ended TTL output.

Figure 12. RSDS Output Data Mapping

Table 5. Input Signal Timing—Reference Only

Signal	Item	Symbol		XGA (1024 x 768)	WXGA1 (1280 x 768)	WXGA2 (1280 x 800)	WXGA3 (1280 x 854)	Unit
Clock Frequency	1/Tclk	F	Typ	65	82	68	69	MHz
Vertical Timing	Total	Tv	Min	774	774	806	860	Th
			Typ	806	806	816	880	
			Max	1024	1024	1024	1024	
	Active	Tvact	Min	-	-	-	-	
			Typ	768	768	800	854	
			Max	-	-	-	-	
Horizontal Timing	Total	Th	Min	1078	1334	1334	1334	Tclk
			Typ	1344	1688	1408	1408	
			Max	2047	2047	2047	2047	
	Active	Thact	Min	100	100	100	100	
			Typ	1024	1280	1280	1280	
			Max	-	-	-	-	

Output Timing—TTL

Table 6. Display Resolution Selection Control

DTM1	DTM0	Display Mode	Resolution
0	0	WXGA1	1280 x 768
0	1	WXGA2	1280 x 800
1	0	XGA	1024 x 768
1	1	WXGA3	1280 x 854

Table 7. TTL Timing Selection Control: RO[2:0]

XGA									
RO[2:0]	**000**	**001**	**010**	**011**	**100**	**101**	**110**	**111**	**Unit**
T1	2	2	2	2	2	2	2	TEST MODE	T_{CLK}
T2	1	1	1	1	1	1	1		T_{CLK}
T3	1030	1030	1030	1030	1030	1030	1030		T_{CLK}
T4	16	24	16	24	32	48	42		T_{CLK}
T5	912	960	960	912	842	912	802		T_{CLK}
T5'	782	830	830	782	712	782	672		T_{CLK}
T6	200	160	160	130	220	220	260		T_{CLK}
T6'	130	130	130	130	130	130	130		T_{CLK}
T7	1038	1056	1056	976	874	976	834		T_{CLK}
T8	650	650	650	650	680	680	725		T_{CLK}
T9	348	348	348	348	348	348	348		T_{CLK}
T10	1	1	1	1	1	1	1		HLINE
T11	348	348	348	348	348	348	348		T_{CLK}
T12	1	1	1	1	1	1	1		HLINE
T13(1)	567	567	567	567	567	567	567		T_{CLK}
T14(1)	2	2	2	2	2	2	2		HLINE

(1) Timing based on first occurrence of STH.

WXGA									
RO[2:0]	**000**	**001**	**010**	**011**	**100**	**101**	**110**	**111**	**Unit**
T1	2	2	2	2	2	2	2	TEST MODE	T_{CLK}
T2	1	1	1	1	1	1	1		T_{CLK}
T3	1286	1286	1286	1286	1286	1286	1286		T_{CLK}
T4	16	24	16	24	32	48	42		T_{CLK}
T5	1168	1216	1216	1168	1098	1168	1058		T_{CLK}
T5'	1038	1086	1086	1038	968	1038	928		T_{CLK}
T6	200	160	160	130	220	220	260		T_{CLK}
T6'	130	130	130	130	130	130	130		T_{CLK}
T7	1294	1312	1312	1232	1130	1232	1090		T_{CLK}
T8	650	650	650	650	680	680	725		T_{CLK}
T9	348	348	348	348	348	348	348		T_{CLK}
T10	1	1	1	1	1	1	1		HLINE
T11	348	348	348	348	348	348	348		T_{CLK}
T12	1	1	1	1	1	1	1		HLINE
T13(1)	567	567	567	567	567	567	567		T_{CLK}
T14(1)	2	2	2	2	2	2	2		HLINE

(1) Timing based on first occurrence of STH.

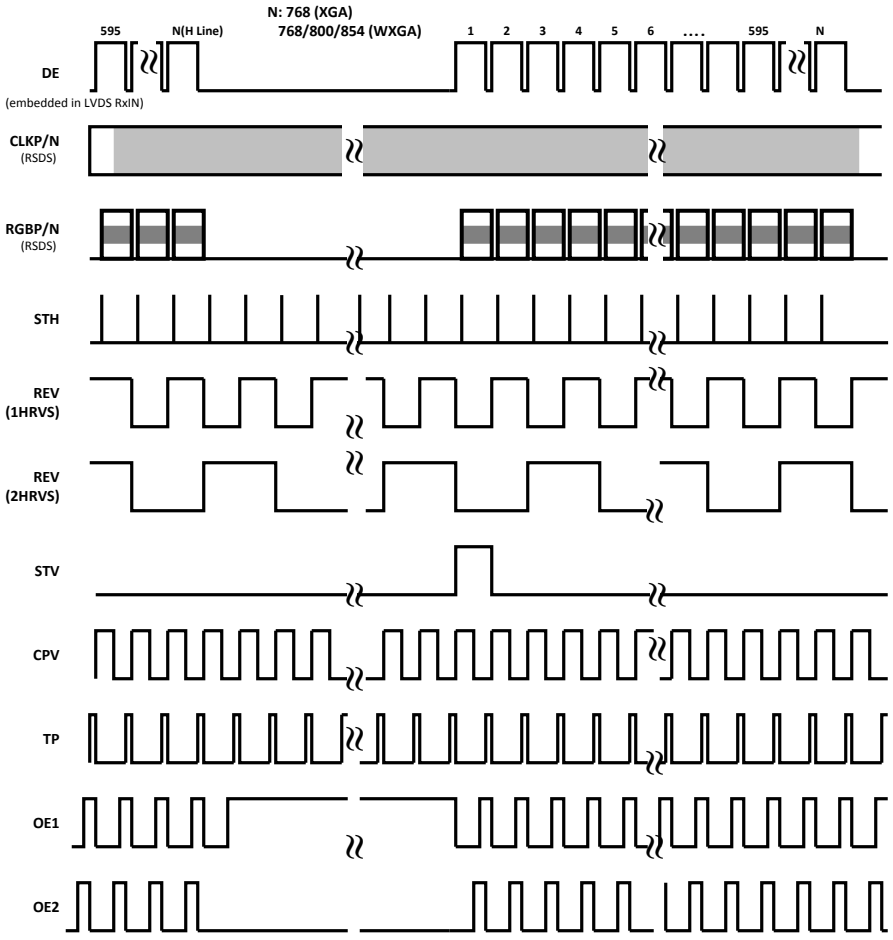
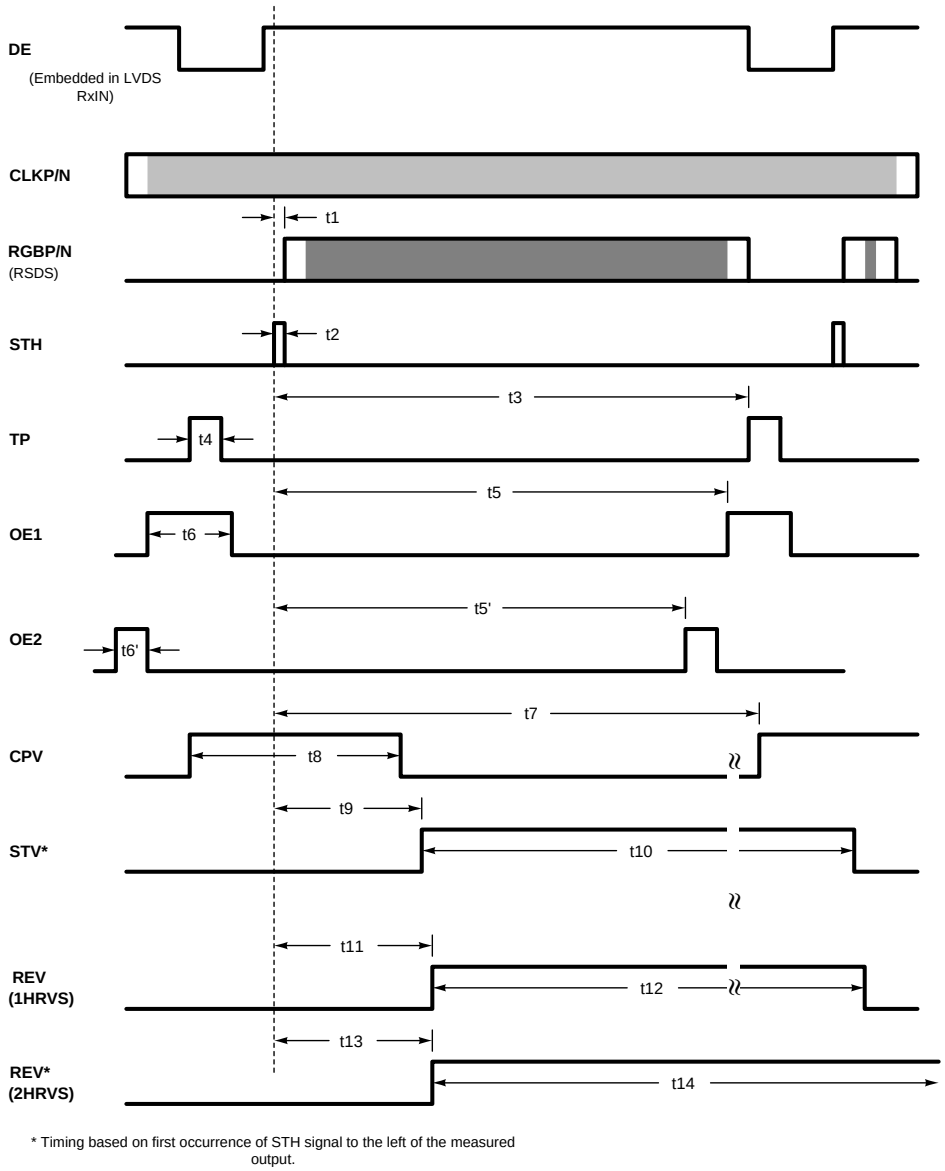


Figure 13. TTL Output Timing Diagram



* Timing based on first occurrence of STH signal to the left of the measured output.

Figure 14. TTL Output Timing Diagram (Continued)

Output Timing—Power-Up Sequence (reference only)

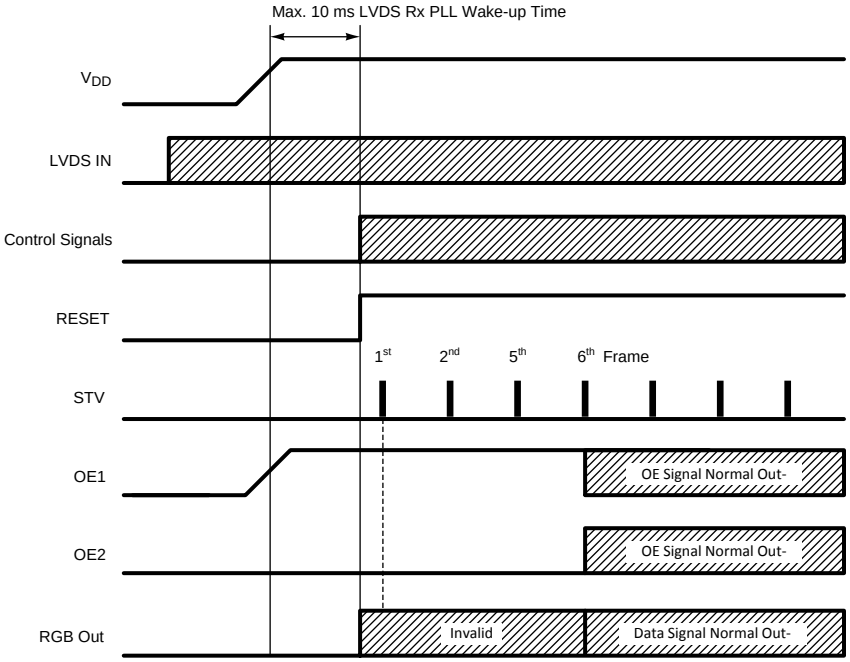


Figure 15. Power-Up Sequence

Connection Diagram

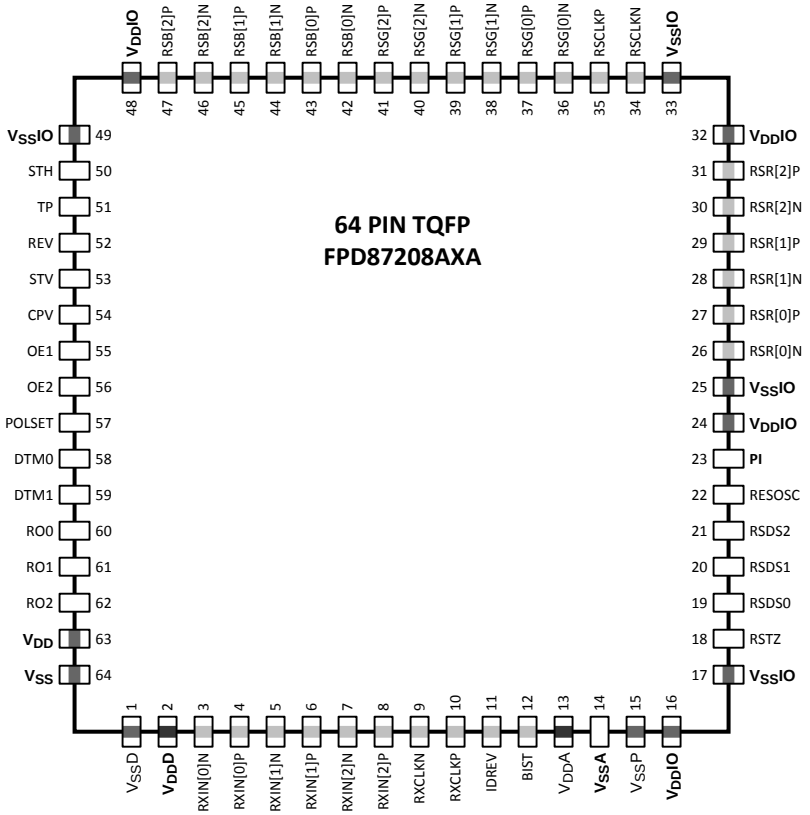


Figure 16. Pinout Assignment

Pin Descriptions

Table 8. LVDS Rx Inputs

Symbol	Pin Count	Type	Function
RxIN[0]N/P	2	LVDSI	LVDS Rx Data Differential Input Pairs
RxIN[1]N/P	2	LVDSI	LVDS Rx Data Differential Input Pairs
RxIN[2]N/P	2	LVDSI	LVDS Rx Data Differential Input Pairs
RxCLKN/P	2	LVDSI	LVDS Rx Clock Differential Input Pairs
Sub-Total Pin Count	8		

Table 9. RSDS Tx Outputs

Symbol	Pin Count	Type	Function
R [2:0]P/N	6	RSO	Red Reduced Swing Differential Outputs to Column Drivers
G [2:0]P/N	6	RSO	Green Reduced Swing Differential Outputs to Column Drivers
B [2:0]P/N	6	RSO	Blue Reduced Swing Differential Outputs to Column Drivers
CLKP/N	2	RSO	Clock Reduced Swing Differential Outputs to Column Drivers
Sub-Total Pin Count	20		

Table 10. RSDS Tx Bias Reference Input

Symbol	Pin Count	Type	Function
PI	1		Current Reference for RSDS Tx Output (1.23V)
Sub-Total Pin Count	1		

Table 11. CMOS Input (2.75V Maximum)

Symbol	Pin Count	Type	Function
RSDS[2:0]	3	I	RSDS Skew/Timing Control
RO[2:0]	3	I	Display Timing Selection
POLSET	1	I	0: Two Line Inversion; 1: One Line Inversion
DTM[1:0]	2	I	Display Mode Selection (XGA, WXGA1, WXGA2, WXGA3)
RESOSC	1	AI	RC oscillator reference for BIST function. 14.5 kΩ = ~40 MHz
IDREV	1	PU	IDREV = HIGH (default, pull high): Output data is 3F during vertical blanking. IDREV = LOW: Output data is 00 during vertical blanking.
BIST	1	I	BIST Control Function (Active High), tied to ground for norm mode
RESETZ	1	Schmitt I	TCON Reset (Active Low)
Sub-Total Pin Count	13		

Table 12. CMOS Outputs (2.75V Maximum)

Symbol	Pin Count	Type	Function
STV	1	TO	Row Driver Start Pulse
CPV	1	TO	Row Driver Shift Clock
TP	1	TO	Line Latch Signal Output to Column Drivers
STH	1	TO	Horizontal Start Signal Output to Column Drivers
REV	1	TO	Alternative Signal Output for each 1 or 2 Horizontal Line to Column Drivers
OE1	1	TO	Control TFT Gate Pulse Width to Row Drivers
OE2	1	TO	Control TFT Gate Pulse Width to Row Drivers
Sub-Total Pin Count	7		

Table 13. Power Supply

Symbol	Pin Count	Type	Function
V_{DD}	1	P	Digital Power for Logic Core
V_{SS}	1	G	Digital Ground for Logic Core
V_{DDIO}	4	P	Digital I/O and RSDS Power
V_{SSIO}	4	G	Digital I/O and RSDS Ground
V_{DDA}	1	P	FPD Receiver—Power for Analog
V_{DDD}	1	P	FPD Receiver—Power for Digital
V_{SSD}	1	G	FPD Receiver—Ground for Digital
V_{SSP}	1	G	FPD Receiver—Ground for PLL
V_{SSA}	1	G	FPD Receiver—Ground for Analog
Sub-Total Pin Count	15		
Total Pin Count	64		System Interface = 8 RSDS Tx Out = 20 RSDS Tx Bias Reference Input = 1 CMOS Input (control) = 13 CMOS Output = 7 Power Supply = 15

Pin Types

AI -Analog Input

I -Input (LVTTL)

TO -TTL Output (LVTTL)

LVDSI -Low Voltage Differential Signal Input

RSO -Reduced Swing Differential Output

P -Power

G -Ground

PD -Pull Down

PU -Pull Up

Schmitt I -Schmitt Triggered Input

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	15

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