LMC6064EP Precision CMOS Quad Micropower Operational Amplifier

Check for Samples: LMC6064EP

FEATURES

(Typical Unless Otherwise Noted)

- **Low Offset Voltage: 100 µV**
- **Ultra Low Supply Current: 16 µA/Amplifier**
- **Operates from 4.5V to 15V Single Supply**
- **Ultra Low Input Bias Current: 10 fA**
- **Output Swing Within 10 mV of Supply Rail, 100k Load**
- **Input Common-Mode Range Includes V^-**
- **High Voltage Gain: 140 dB**
- **Improved Latchup Immunity**

APPLICATIONS

- **Instrumentation Amplifier**
- **Photodiode and Infrared Detector Preamplifier**
- **Transducer Amplifiers**
- **D/A Converter**
- **Selected Military Applications**
- **Selected Avionics Applications**

ENHANCED PLASTIC

- **Extended Temperature Performance of −40°C to +85°C**
- **Baseline Control - Single Fab & Assembly Site**
- **Process Change Notification (PCN)**
- **Qualification & Reliability Data**
- **Solder (PbSn) Lead Finish is standard**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**

PATENT PENDING

DESCRIPTION

The LMC6064EP is a precision quad low offset voltage, micropower operational amplifier, capable of precision single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low power consumption make the LMC6064EP ideally suited for battery powered applications.

Other applications using the LMC6064EP include precision full-wave rectifiers, integrators, references, sample-and-hold circuits, and true instrumentation amplifiers.

This device is built with Texas Instruments' advanced double-Poly Silicon-Gate CMOS process.

For designs that require higher speed, see the LMC6084 precision quad operational amplifier.

For single or dual operational amplifier with similar features, see the LMC6061 or LMC6062 respectively.

Connection Diagram

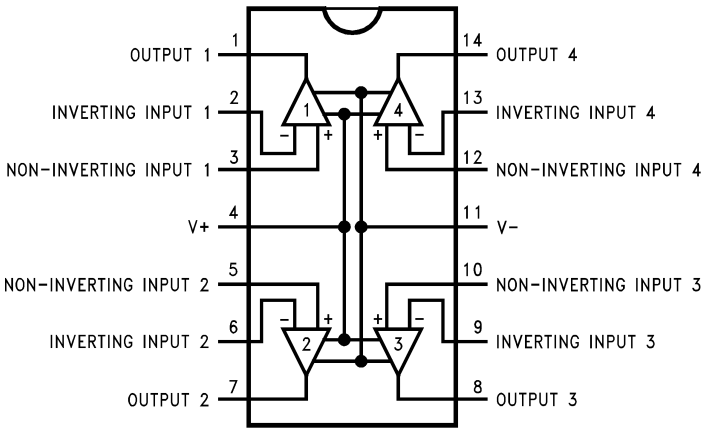


Figure 1. 14-Pin PDIP/SOIC - Top View

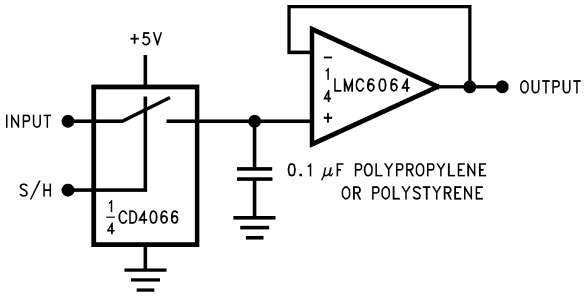


Figure 2. Low-Leakage Sample and Hold

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)

Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	(V^+) +0.3V,
	(V^-) −0.3V
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	See (2)
Output Short Circuit to V^-	See (3)
Lead Temperature	
(Soldering, 10 sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature	150°C
ESD Tolerance (4)	2 kV
Current at Input Pin	±10 mA
Current at Output Pin	±30 mA
Current at Power Supply Pin	40 mA
Power Dissipation	See (5)

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed.
(2) Do not connect output to V^+, when V^+ is greater than 13V or reliability witll be adversely affected.
(3) Applies to both single-supply and split-supply operation. Continous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.
(4) Human body model, 1.5 kΩ in series with 100 pF.
(5) The maximum power dissipation is a function of $T_{J(Max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} - T_A)/\theta_{JA}$.

OPERATING RATINGS (1)

Temperature Range	
LMC6064AIEP, LMC6064IEP	$-40°C \le T_J \le +85°C$
Supply Voltage	$4.5V \le V^+ \le 15.5V$
Thermal Resistance (θ_{JA}) (2)	
14-Pin PDIP	81°C/W
14-Pin SOIC	126°C/W
Power Dissipation	See (3)

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed.
(2) All numbers apply for packages soldered directly into a PC board.
(3) For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all limits specified for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified. (1)

Symbol	Parameter	Conditions		Typ (2)	LMC6064AIEP Limit (3)	LMC6064IEP Limit (3)	Units
V_{OS}	Input Offset Voltage			100	350	800	µV
					900	**1300**	Max
TCV_{OS}	Input Offset Voltage			1.0			µV/°C
	Average Drift						
I_B	Input Bias Current			0.010			pA
					4	**4**	Max
I_{OS}	Input Offset Current			0.005			pA
					2	**2**	Max
R_{IN}	Input Resistance			>10			Tera Ω
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 12.0V V^+ = 15V		85	75	66	dB
					72	**63**	Min
+PSRR	Positive Power Supply Rejection Ratio	5V ≤ V^+ ≤ 15V V_O = 2.5V		85	75	66	dB
					72	**63**	Min
−PSRR	Negative Power Supply Rejection Ratio	0V ≤ V^- ≤ −10V		100	84	74	dB
					81	**71**	Min
V_{CM}	Input Common-Mode Voltage Range	V^+ = 5V and 15V for CMRR ≥ 60 dB		−0.4	−0.1	−0.1	V
					0	**0**	Max
				V^+ − 1.9	V^+ − 2.3	V^+ − 2.3	V
					V^+ − 2.5	**V^+ − 2.5**	Min
A_V	Large Signal Voltage Gain	R_L = 100 kΩ (4)	Sourcing	4000	400	300	V/mV
					300	**200**	Min
			Sinking	3000	180	90	V/mV
					100	**60**	Min
		R_L = 25 kΩ (4)	Sourcing	3000	400	200	V/mV
					150	**80**	Min
			Sinking	2000	100	70	V/mV
					50	**35**	Min

(1) "Testing and other quality control techniques are used to the extent deemed necessary to ensure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific PARAMETRIC testing, product performance is assured by characterization and/or design."
(2) Typical values represent the most likely parametric norm.
(3) All limits are ensured by testing or statistical analysis.
(4) V^+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 2.5V ≤ V_O ≤ 7.5V.

DC ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified, all limits specified for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified. (1)

Symbol	Parameter	Conditions	Typ (2)	LMC6064AIEP Limit (3)	LMC6064IEP Limit (3)	Units
V_O	Output Swing	V^+ = 5V R_L = 100 kΩ to 2.5V	4.995	4.990	4.950	V
				4.980	**4.925**	Min
			0.005	0.010	0.050	V
				0.020	**0.075**	Max
		V^+ = 5V R_L = 25 kΩ to 2.5V	4.990	4.975	4.950	V
				4.965	**4.850**	Min
			0.010	0.020	0.050	V
				0.035	**0.150**	Max
		V^+ = 15V R_L = 100 kΩ to 7.5V	14.990	14.975	14.950	V
				14.965	**14.925**	Min
			0.010	0.025	0.050	V
				0.035	**0.075**	Max
		V^+ = 15V R_L = 25 kΩ to 7.5V	14.965	14.900	14.850	V
				14.850	**14.800**	Min
			0.025	0.050	0.100	V
				0.150	**0.200**	Max
I_O	Output Current V^+ = 5V	Sourcing, V_O = 0V	22	16	13	mA
				10	**8**	Min
		Sinking, V_O = 5V	21	16	16	mA
				8	**8**	Min
	Output Current V^+ = 15V	Sourcing, V_O = 0V	25	15	15	mA
				10	**10**	Min
		Sinking, V_O = 13V (5)	26	20	20	mA
				8	**8**	Min
I_S	Supply Current	All Four Amplifiers V^+ = +5V, V_O = 1.5V	64	76	92	µA
				92	**112**	Max
		All Four Amplifiers V^+ = +15V, V_O = 7.5V		94	114	µA
			80	**110**	**132**	Max

(5) Do not connect output to V^+, when V^+ is greater than 13V or reliability witll be adversely affected.

AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all limits specified for T_J = 25°C, **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified. (1)

Symbol	Parameter	Conditions	Typ(2)	LMC6064AIEP Limit(3)	LMC6064IEP Limit(3)	Units
SR	Slew Rate	See (4)	35	20	15	V/ms
				10	**7**	Min
GBW	Gain-Bandwidth Product		100			kHz
θ_m	Phase Margin		50			Deg
	Amp-to-Amp Isolation	See (5)	155			dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	83			nV/$\sqrt{Hz}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002			pA/$\sqrt{Hz}$
T.H.D.	Total Harmonic Distortion	F = 1 kHz, A_V = −5				
		R_L = 100 kΩ, V_O = 2 V_{PP}	0.01			%
		±5V Supply				

(1) "Testing and other quality control techniques are used to the extent deemed necessary to ensure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific PARAMETRIC testing, product performance is assured by characterization and/or design."
(2) Typical values represent the most likely parametric norm.
(3) All limits are ensured by testing or statistical analysis.
(4) V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.
(5) Input referred V^+ = 15V and R_L = 100 kΩ connected to 7.5V. Each amp excited in turn with 100 Hz to produce V_O = 12 V_{PP}.

TYPICAL PERFORMANCE CHARACTERISTICS

Distribution of LMC6064AIMEP Input Offset Voltage (T_A = +25°C)

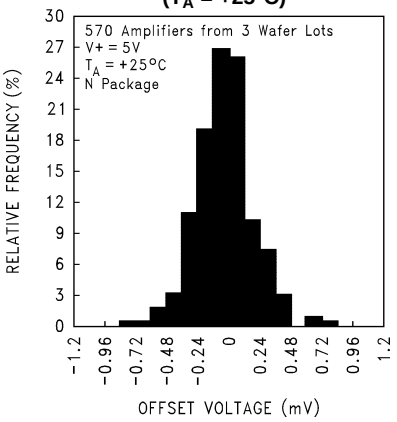


Figure 3.

Distribution of LMC6064AIMEP Input Offset Voltage (T_A = −55°C)

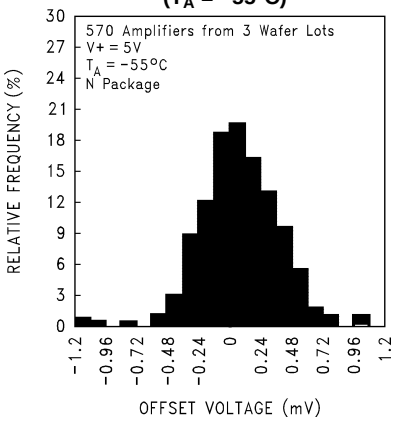


Figure 4.

Distribution of LMC6064AIMEP Input Offset Voltage (T_A = +125°C)

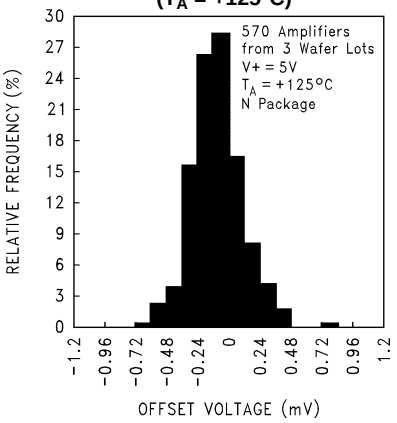


Figure 5.

Input Bias Current vs Temperature

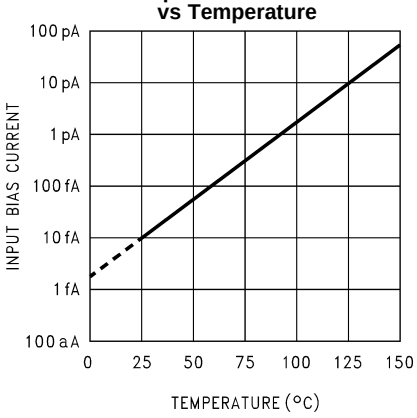


Figure 6.

Supply Current vs Supply Voltage

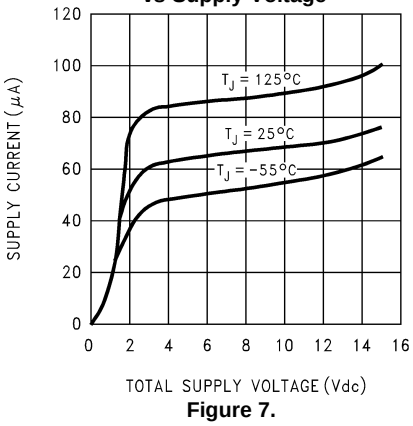


Figure 7.

Input Voltage vs Output Voltage

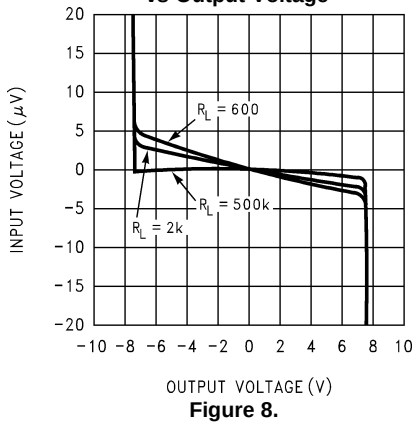


Figure 8.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Common Mode Rejection Ratio vs Frequency

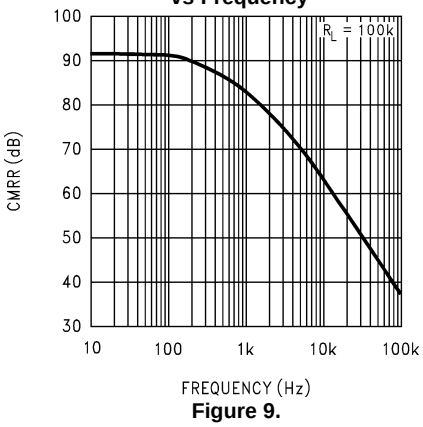


Figure 9.

Power Supply Rejection Ratio vs Frequency

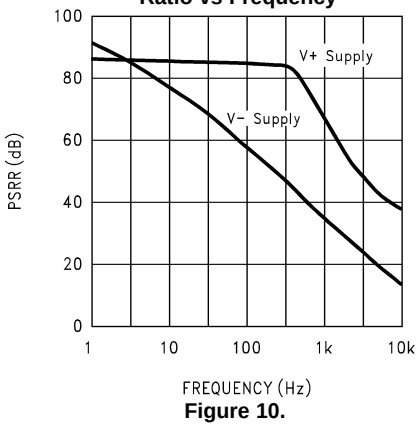


Figure 10.

Input Voltage Noise vs Frequency

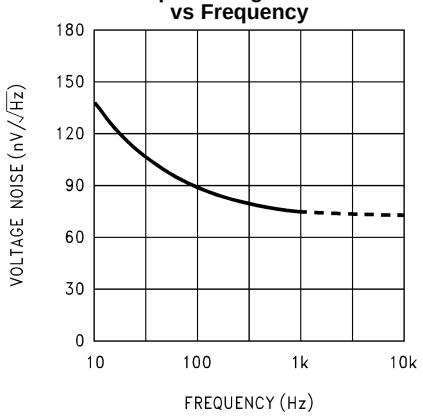


Figure 11.

Output Characteristics Sourcing Current

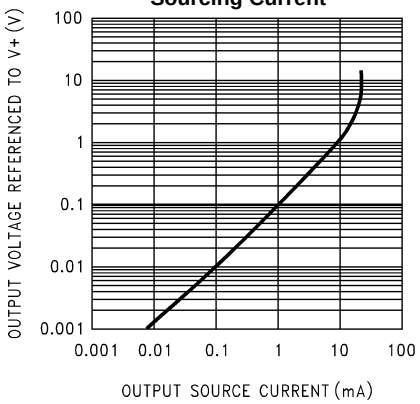


Figure 12.

Output Characteristics Sinking Current

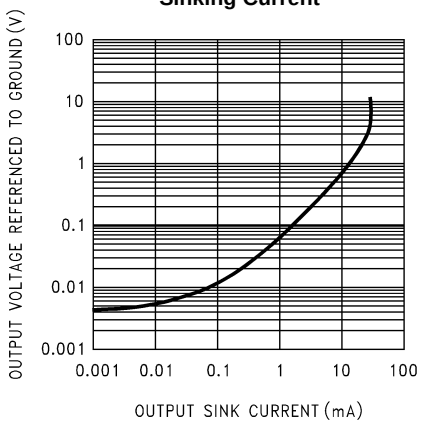


Figure 13.

Gain and Phase Response vs Temperature (−55°C to +125°C)

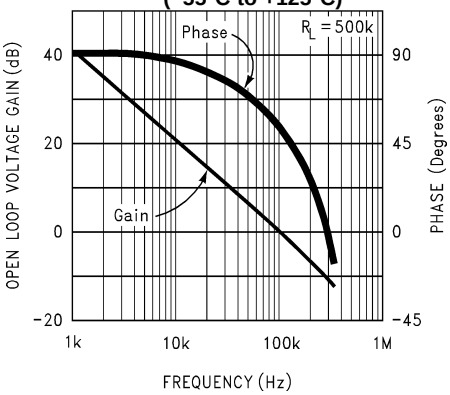


Figure 14.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Gain and Phase Response vs Capacitive Load with R_L = 20 kΩ

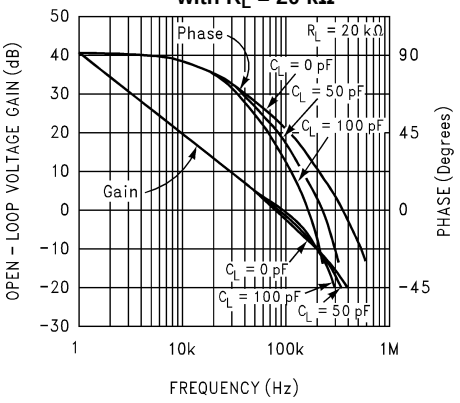


Figure 15.

Gain and Phase Response vs Capacitive Load with R_L = 500 kΩ

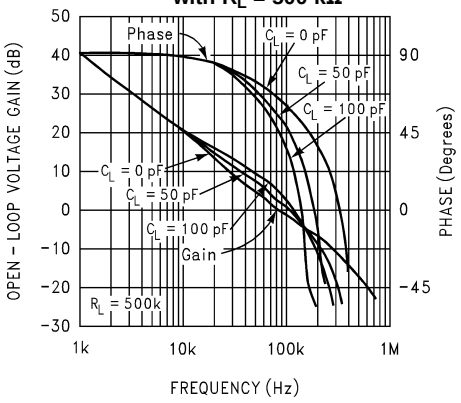


Figure 16.

Open Loop Frequency Response

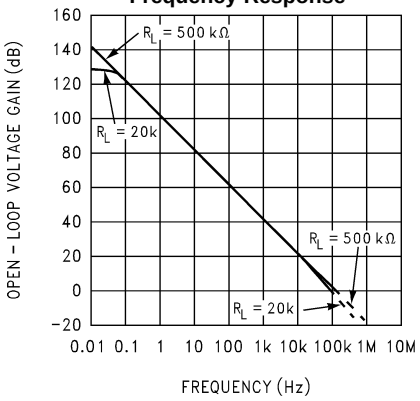


Figure 17.

Inverting Small Signal Pulse Response

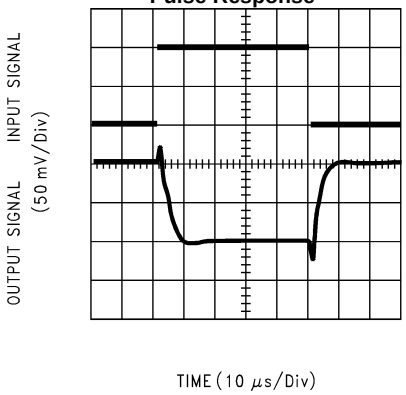


Figure 18.

Inverting Large Signal Pulse Response

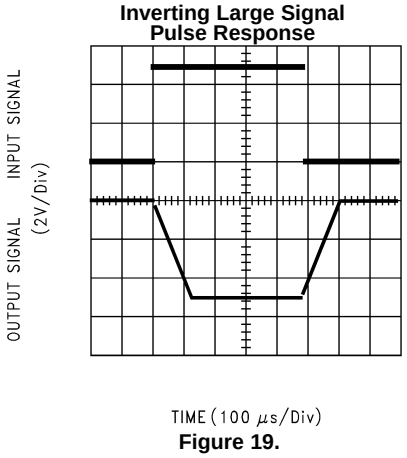


Figure 19.

Non-Inverting Small Signal Pulse Response

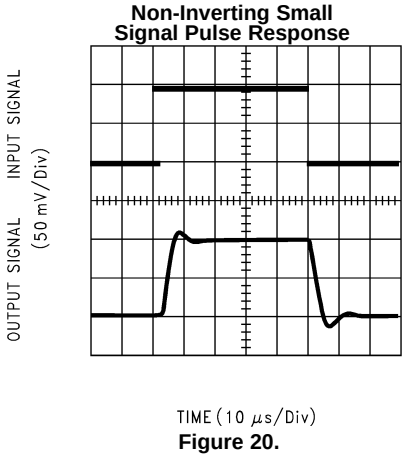


Figure 20.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Non-Inverting Large Signal Pulse Response

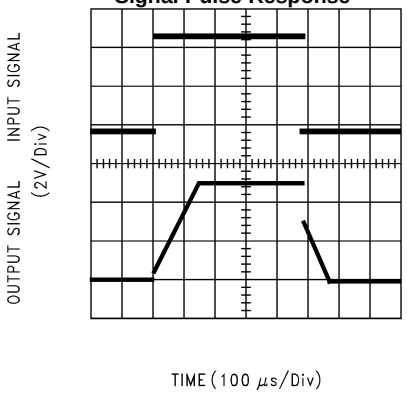


Figure 21.

Crosstalk Rejection vs Frequency

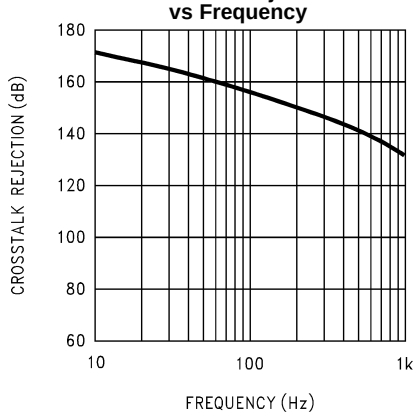


Figure 22.

Stability vs Capacitive Load, R_L = 20 kΩ

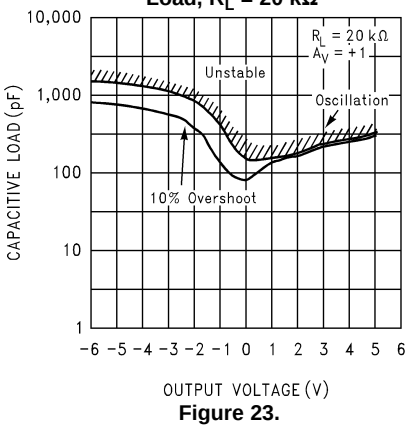


Figure 23.

Stability vs Capacitive Load R_L = 1 MΩ

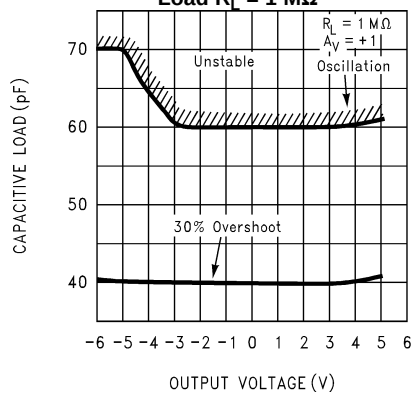


Figure 24.

APPLICATIONS HINTS

AMPLIFIER TOPOLOGY

The LMC6064EP incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6064EP both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6064EP.

Although the LMC6064EP is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6064EP is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See *Printed-Circuit-Board Layout for High-Impedance Work*).

The effect of input capacitance can be compensated for by adding a capacitor. Place a capacitor, C_f, around the feedback resistor (as in Figure 25) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \tag{1}$$

or $R_1 C_{IN} \leq R_2 C_f$

Since it is often difficult to know the exact value of C_{IN}, C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and the LMC662 for a more detailed discussion on compensating for input capacitance.

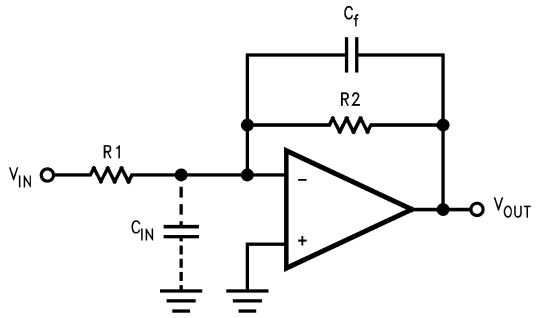


Figure 25. Canceling the Effect of Input Capacitance

CAPACITIVE LOAD TOLERANCE

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominate pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see Typical Performance Characteristics).

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in Figure 26.

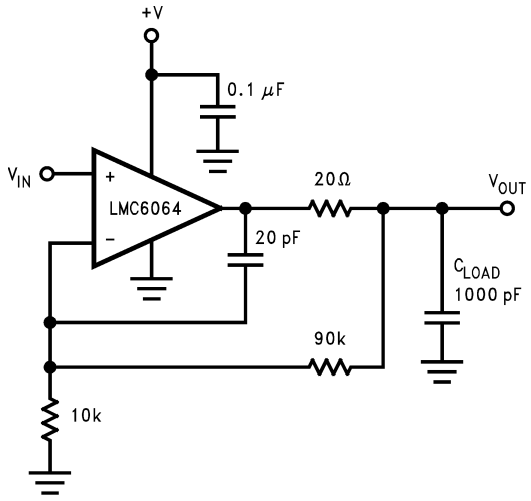


Figure 26. LMC6064EP Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of Figure 26, R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (Figure 27). Typically a pull up resistor conducting 10 µA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

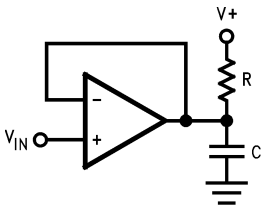


Figure 27. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6064EP, typically less than 10 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6064EP's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals etc. connected to the op-amp's inputs, as in Figure 28. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6064EP's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See Figure 31 for typical connections of guard rings for standard op-amp configurations.

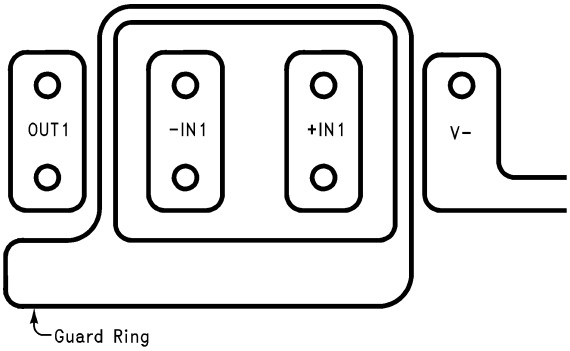


Figure 28. Example of Guard Ring in P.C. Board Layout

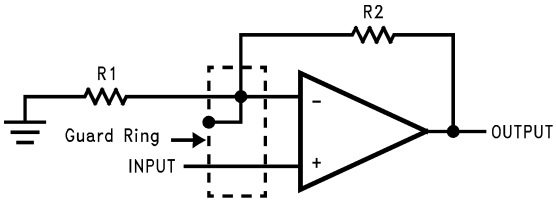


Figure 30. Non-Inverting Amplifier Typical Connection of Guard Rings

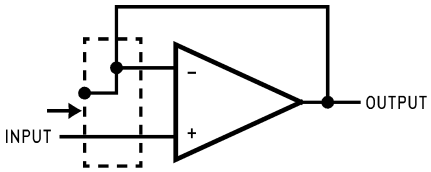


Figure 31. Follower Typical Connection of Guard Rings

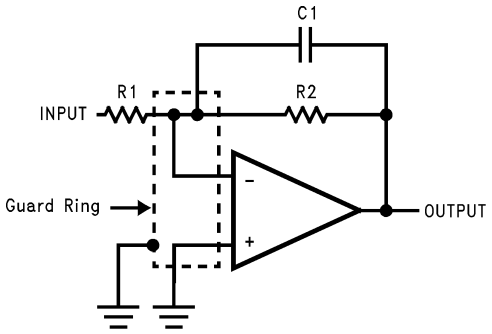
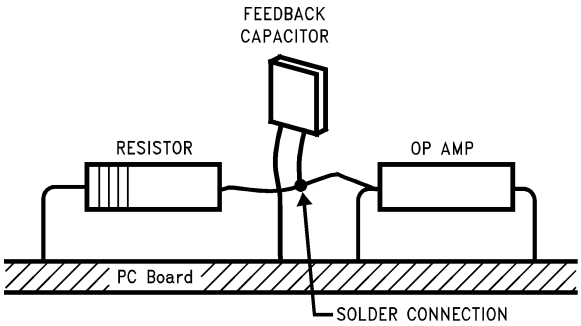


Figure 29. Inverting Amplifier Typical Connection of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 32.

LATCHUP

CMOS devices tend to be susceptible to latchup due to their internal parasitic SCR effects. The (I/O) input and output pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMC6064EP and LMC6082 are designed to withstand 100 mA surge current on the I/O pins. Some resistive method should be used to isolate any capacitance from supplying excess current to the I/O pins. In addition, like an SCR, there is a minimum holding current for any latchup mode. Limiting current to the supply pins will also inhibit latchup susceptibility.



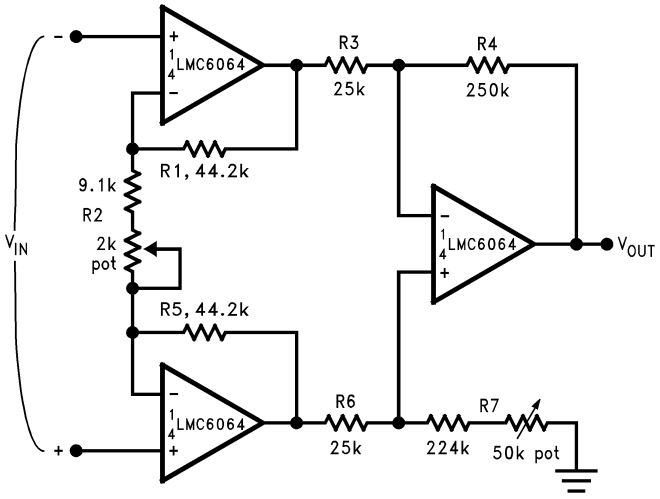
(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board).

Figure 32. Air Wiring

TYPICAL SINGLE-SUPPLY APPLICATIONS ($V^+ = 5.0\ V_{DC}$)

The extremely high input impedance, and low power consumption, of the LMC6064EP make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

Figure 33 shows an instrumentation amplifier that features high differential and common mode input resistance ($>10^{14}\Omega$), 0.01% gain accuracy at A_V = 100, excellent CMRR with 1 kΩ imbalance in bridge source resistance. Input current is less than 100 fA and offset drift is less than 2.5 µV/°C. R_2 provides a simple means of adjusting gain over a wide range without degrading CMRR. R_7 is an initial trim used to maximize CMRR without using super precision matched resistors. For good CMRR over temperature, low drift resistors should be used.



If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3}$$

$\therefore A_V \approx 100$ for circuit shown (R_2 = 9.822k).

Figure 33. Instrumentation Amplifier

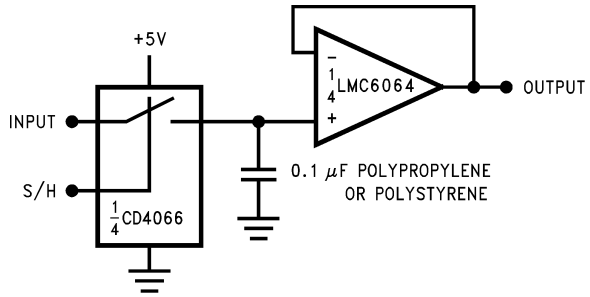


Figure 34. Low-Leakage Sample and Hold

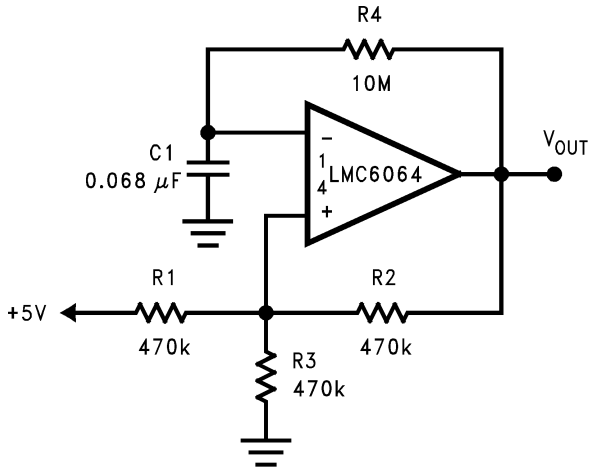


Figure 35. 1 Hz Square Wave Oscillator

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	15

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