

FPD87370AXA Low EMI, Low Dynamic Power VGA/XGA/WXGA TFT-LCD Timing Controller with Reduced Swing Differential Signaling (RSDS™) Outputs

Check for Samples: [FPD87370](#)

FEATURES

- **Reduced Swing Differential Signalling (RSDS™) Digital Bus Reduces Dynamic Power, EMI and Bus Width from the Timing Controller**
- **LVDS Single Pixel Input Interface System**
- **Input Clock Range from 25 MHz to 85 MHz**
- **Drives RSDS™ Column Drivers at 170 Mb/s with an 85 MHz Clock (Max.)**
- **Virtual 8 Bit Color Depth in FRC/Dithering Mode**
- **Single Narrow 9-Bit Differential Source Driver Bus Minimizes Width of Source PCB**
- **Ability to Drive VGA, XGA and Wide XGA TFT-LCD Systems**
- **Failure Detect Function in DE Mode (Bonding Option)**
- **CMOS Circuitry Operates from a 3.0V–3.6V Supply**

DESCRIPTION

The FPD87370AXA is a timing controller that combines an LVDS single pixel input interface with TI's Reduced Swing Differential Signaling (RSDS™) output driver interface for VGA, XGA and Wide XGA resolutions. It resides on the TFT-LCD panel and provides the data buffering and control signal generation for VGA, XGA, and Wide XGA graphic modes. The RSDS™ path to the column driver contributes toward lowering radiated EMI and reducing system dynamic power consumption.

This single RSDS™ bus conveys the 8-bit color data for VGA, XGA, and Wide XGA panels at 170 Mb/s when using VESA 60 Hz standard timing.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

System Diagram

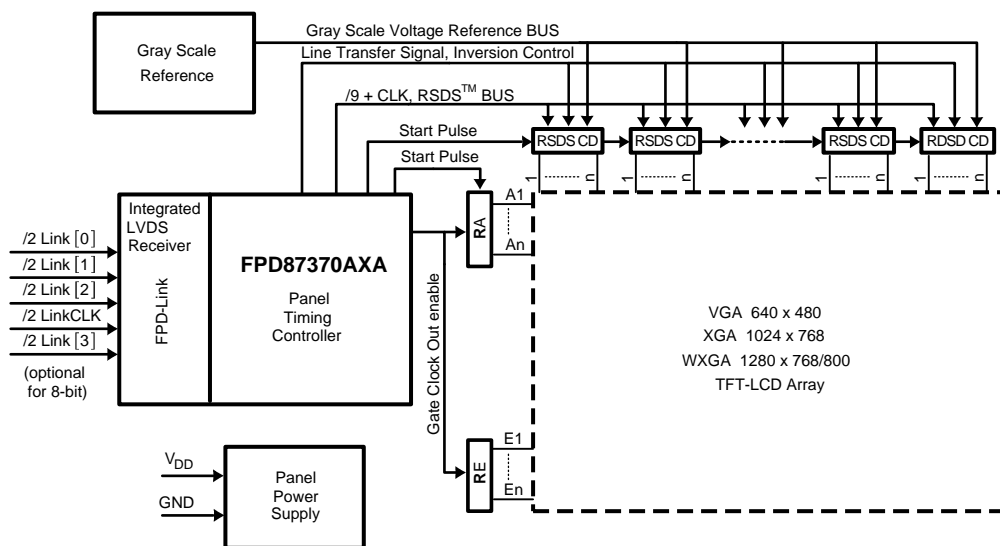


Figure 1. Block Diagram of the LCD Module



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REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	1

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