LMV791/LMV792 17 MHz, Low Noise, CMOS Input, 1.8V Operational Amplifiers with Shutdown

Check for Samples: LMV791, LMV792

FEATURES

(Typical 5V Supply, Unless Otherwise Noted)

- **Input Referred Voltage Noise 5.8 nV/√Hz**
- **Input Bias Current 100 fA**
- **Unity Gain Bandwidth 17 MHz**
- **Supply Current per Channel Enable Mode**
  - **LMV791 1.15 mA**
  - **LMV792 1.30 mA**
- **Supply Current per Channel in Shutdown Mode 0.02 µA**
- **Rail-to-Rail Output Swing**
  - **@ 10 kΩ Load 25 mV from Rail**
  - **@ 2 kΩ Load 45 mV from Rail**
- **Ensured 2.5V and 5.0V Performance**
- **Total Harmonic Distortion 0.01% @1 kHz, 600Ω**
- **Temperature Range −40°C to 125°C**

APPLICATIONS

- **Photodiode Amplifiers**
- **Active Filters and Buffers**
- **Low Noise Signal Processing**
- **Medical Instrumentation**
- **Sensor Interface Applications**

DESCRIPTION

The LMV791 (Single) and the LMV792 (Dual) low noise, CMOS input operational amplifiers offer a low input voltage noise density of 5.8 nV/√Hz while consuming only 1.15 mA (LMV791) of quiescent current. The LMV791 and LMV792 are unity gain stable op amps and have gain bandwidth of 17 MHz. The LMV791/ LMV792 have a supply voltage range of 1.8V to 5.5V and can operate from a single supply. The LMV791/LMV792 each feature a rail-to-rail output stage capable of driving a 600Ω load and sourcing as much as 60 mA of current.

The LMV791 family provides optimal performance in low voltage and low noise systems. A CMOS input stage, with typical input bias currents in the range of a few femtoAmperes, and an input common mode voltage range which includes ground make the LMV791 and the LMV792 ideal for low power sensor applications. The LMV791 family has a built-in enable feature which can be used to optimize power dissipation in low power applications.

The LMV791/LMV792 are manufactured using TI's advanced VIP50 process and are offered in a 6-pin SOT and a 10-pin VSSOP package respectively.

Typical Application

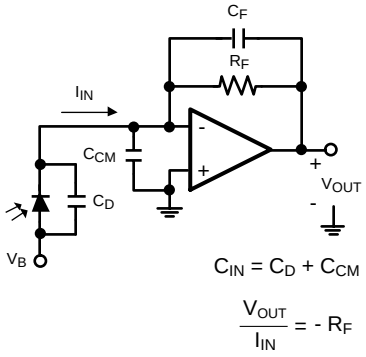


Figure 1. Photodiode Transimpedance Amplifier

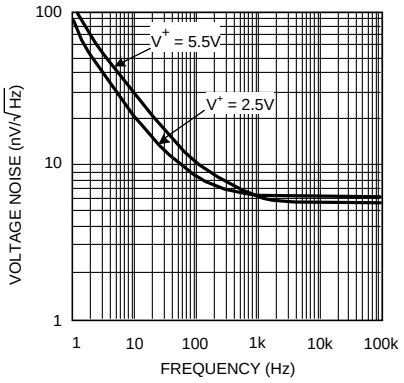


Figure 2. Input Referred Voltage Noise vs. Frequency

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

ESD Tolerance(3)	Human Body Model	2000V
	Machine Model	200V
	Charge-Device Model	1000V
V_{IN} Differential		±0.3V
Supply Voltage ($V^+ - V^-$)		6.0V
Input/Output Pin Voltage		V^+ +0.3V, V^- −0.3V
Storage Temperature Range		−65°C to 150°C
Junction Temperature(4)		+150°C
Soldering Information	Infrared or Convection (20 sec)	235°C
	Wave Soldering Lead Temp (10 sec)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Human Body Model is 1.5 kΩ in series with 100 pF. Machine Model is 0Ω in series with 200 pF
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Operating Ratings(1)

Temperature Range(2)		−40°C to 125°C
Supply Voltage ($V^+ - V^-$) −40°C ≤ T_A ≤ 125°C		2.0V to 5.5V
0°C ≤ T_A ≤ 125°C		1.8V to 5.5V
Package Thermal Resistance (θ_{JA})(2)	6-Pin SOT	170°C/W
	10-Pin VSSOP	236°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

2.5V Electrical Characteristics

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 2.5V, V^- = 0V, $V_{CM} = V^+/2 = V_O$, $V_{EN} = V^+$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min (1)	Typ (2)	Max (1)	Units
V_{OS}	Input Offset Voltage				0.1	±1.35 **±1.65**	mV
TC V_{OS}	Input Offset Voltage Temperature Drift	LMV791(3)			−1.0		µV/°C
		LMV792(3)			−1.8		
I_B	Input Bias Current	V_{CM} = 1.0V(4) (5)	−40°C ≤ T_A ≤ 85 °C		0.05	1 **25**	pA
			−40°C ≤ T_A ≤ 85 °C		0.05	1 **100**	
I_{OS}	Input Offset Current	V_{CM} = 1.0V(5)			10		fA

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using the statistical quality control (SQC) method.
(2) Typical values represent the parametric norm at the time of characterization.
(3) Offset voltage average drift is determined by dividing the change in V_{OS} by temperature change.
(4) Positive current corresponds to current flowing into the device.
(5) This parameter is specified by design and/or characterization and is not tested in production.

2.5V Electrical Characteristics (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 2.5V, V^- = 0V, V_{CM} = $V^+/2$ = V_O, V_{EN} = V^+. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min (1)	Typ (2)	Max (1)	Units
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 1.4V		80 **75**	94		dB
PSRR	Power Supply Rejection Ratio	2.0V ≤ V^+ ≤ 5.5V, V_{CM} = 0V		80 **75**	100		dB
		1.8V ≤ V^+ ≤ 5.5V, V_{CM} = 0V		80	98		
CMVR	Common Mode Voltage Range	CMRR ≥ 60 dB CMRR ≥ 55 dB		−0.3 **−0.3**		1.5 **1.5**	V
A_{VOL}	Open Loop Voltage Gain	V_{OUT} = 0.15V to 2.2V, R_{LOAD} = 2 kΩ to $V^+/2$	LMV791	85 **80**	98		dB
			LMV792	82 **78**	92		
		V_{OUT} = 0.15V to 2.2V, R_{LOAD} = 10 kΩ to $V^+/2$		88 **84**	110		
V_{OUT}	Output Voltage Swing High	R_{LOAD} = 2 kΩ to $V^+/2$			25	75 **82**	mV from either rail
		R_{LOAD} = 10 kΩ to $V^+/2$			20	65 **71**	
	Output Voltage Swing Low	R_{LOAD} = 2 kΩ to $V^+/2$			30	75 **78**	
		R_{LOAD} = 10 kΩ to $V^+/2$			15	65 **67**	
I_{OUT}	Output Current	Sourcing to V^- V_{IN} = 200 mV (6)		35 **28**	47		mA
		Sinking to V^+ V_{IN} = –200 mV (6)		7 **5**	15		
I_S	Supply Current per Amplifier	Enable Mode V_{EN} ≥ 2.1V	LMV791		0.95	1.30 **1.65**	mA
			LMV792 per channel		1.1	1.50 **1.85**	
		Shutdown Mode, V_{EN} < 0.4 per channel			0.02	1 **5**	µA
SR	Slew Rate	A_V = +1, Rising (10% to 90%)			8.5		V/µs
		A_V = +1, Falling (90% to 10%)			10.5		
GBW	Gain Bandwidth				14		MHz
e_n	Input Referred Voltage Noise Density	f = 1 kHz			6.2		nV/√Hz
i_n	Input Referred Current Noise Density	f = 1 kHz			0.01		pA/√Hz
t_{on}	Turn-on Time				140		ns
t_{off}	Turn-off Time				1000		ns
V_{EN}	Enable Pin Voltage Range	Enable Mode		2.1	2 to 2.5		V
		Shutdown Mode			0 to 0.5	0.4	
I_{EN}	Enable Pin Input Current	Enable Mode V_{EN} = 2.5V (7)			1.5	3	µA
		Shutdown Mode V_{EN} = 0V (7)			0.003	0.1	
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 1, R_{LOAD} = 600Ω			0.01		%

(6) The short circuit test is a momentary test, the short circuit duration is 1.5 ms.
(7) Positive current corresponds to current flowing into the device.

5V Electrical Characteristics

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = $V^+/2$ = V_O, V_{EN} = V^+. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min (1)	Typ (2)	Max (1)	Units
V_{OS}	Input Offset Voltage				0.1	±1.35 **±1.65**	mV
TC V_{OS}	Input Offset Voltage Temperature Drift	LMV791 (3)			−1.0		µV/°C
		LMV792 (3)			−1.8		
I_B	Input Bias Current	V_{CM} = 2.0V (4) (5)	−40°C ≤ T_A ≤ 85°C		0.1	1 **25**	pA
			−40°C ≤ T_A ≤ 125°C		0.1	1 **100**	
I_{OS}	Input Offset Current	V_{CM} = 2.0V (5)			10		fA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 3.7V		80 **75**	100		dB
PSRR	Power Supply Rejection Ratio	2.0V ≤ V^+ ≤ 5.5V, V_{CM} = 0V		80 **75**	100		dB
		1.8V ≤ V^+ ≤ 5.5V, V_{CM} = 0V		80	98		
CMVR	Common Mode Voltage Range	CMRR ≥ 60 dB CMRR ≥ 55 dB		−0.3 **−0.3**		4 **4**	V
A_{VOL}	Open Loop Voltage Gain	V_{OUT} = 0.3V to 4.7V, R_{LOAD} = 2 kΩ to $V^+/2$	LMV791	85 **80**	97		dB
			LMV792	82 **78**	89		
		V_{OUT} = 0.3V to 4.7V, R_{LOAD} = 10 kΩ to $V^+/2$		88 **84**	110		
V_{OUT}	Output Voltage Swing High	R_{LOAD} = 2 kΩ to $V^+/2$			35	75 **82**	mV from either rail
		R_{LOAD} = 10 kΩ to $V^+/2$			25	65 **71**	
	Output Voltage Swing Low	R_{LOAD} = 2 kΩ to $V^+/2$	LMV791		42	75 **78**	
			LMV792		45	80 **83**	
		R_{LOAD} = 10 kΩ to $V^+/2$			20	65 **67**	
I_{OUT}	Output Current	Sourcing to V^- V_{IN} = 200 mV (6)		45 **37**	60		mA
		Sinking to V^+ V_{IN} = –200 mV (6)		10 **6**	21		
I_S	Supply Current per Amplifier	Enable Mode V_{EN} ≥ 4.6V	LMV791		1.15	1.40 **1.75**	mA
			LMV792 per channel		1.30	1.70 **2.05**	
		Shutdown Mode (V_{EN} ≤ 0.4V)			0.14	1 **5**	µA
SR	Slew Rate	A_V = +1, Rising (10% to 90%)		6.0	9.5		V/µs
		A_V = +1, Falling (90% to 10%)		7.5	11.5		
GBW	Gain Bandwidth				17		MHz

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using the statistical quality control (SQC) method.
(2) Typical values represent the parametric norm at the time of characterization.
(3) Offset voltage average drift is determined by dividing the change in V_{OS} by temperature change.
(4) Positive current corresponds to current flowing into the device.
(5) This parameter is specified by design and/or characterization and is not tested in production.
(6) The short circuit test is a momentary test, the short circuit duration is 1.5 ms.

5V Electrical Characteristics (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = $V^+/2$ = V_O, V_{EN} = V^+. **Boldface** limits apply at the temperature extremes.

e_n	Input Referred Voltage Noise Density	f = 1 kHz		5.8		nV/√Hz
i_n	Input Referred Current Noise Density	f = 1 kHz		0.01		pA/√Hz
t_{on}	Turn-on Time			110		ns
t_{off}	Turn-off Time			800		ns
V_{EN}	Enable Pin Voltage Range	Enable Mode	4.6	4.5 to 5		V
		Shutdown Mode		0 to 0.5	0.4	
I_{EN}	Enable Pin Input Current	Enable Mode V_{EN} = 5.0V (7)		5.6	10	µA
		Shutdown Mode V_{EN} = 0V (7)		0.005	0.2	
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 1, R_{LOAD} = 600Ω		0.01		%

(7) Positive current corresponds to current flowing into the device.

Connection Diagram

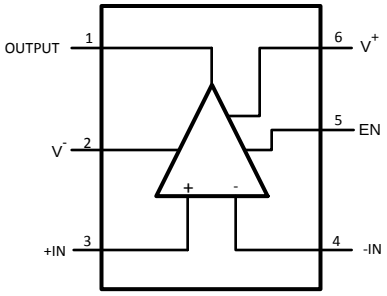


Figure 3. 6-Pin SOT
Top View

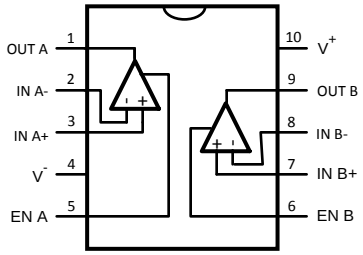


Figure 4. 10-Pin VSSOP
Top View

Typical Performance Characteristics

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = Supply Voltage = 5V, V_{CM} = V^+/2, V_{EN} = V^+.

Supply Current vs. Supply Voltage (LMV791)

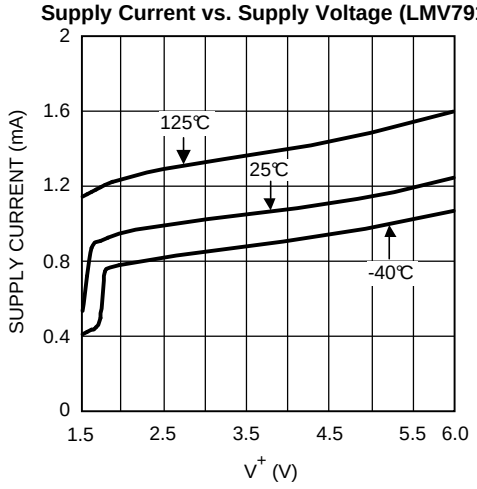


Figure 5.

Supply Current vs. Supply Voltage (LMV792)

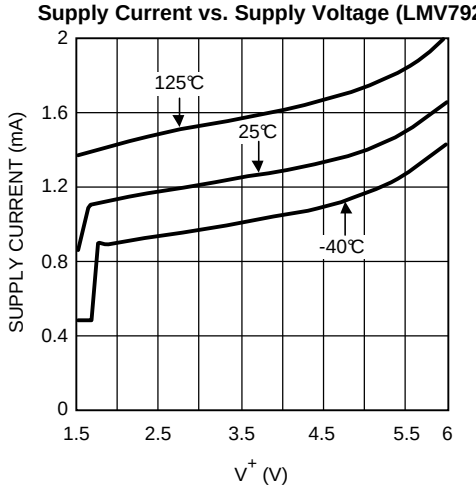


Figure 6.

Supply Current vs.\ Supply Voltage in Shutdown Mode

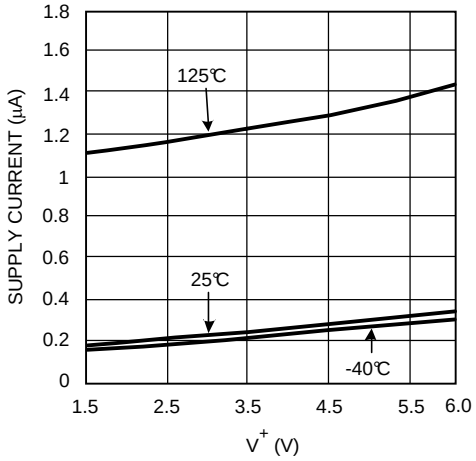


Figure 7.

V_{OS} vs. V_{CM}

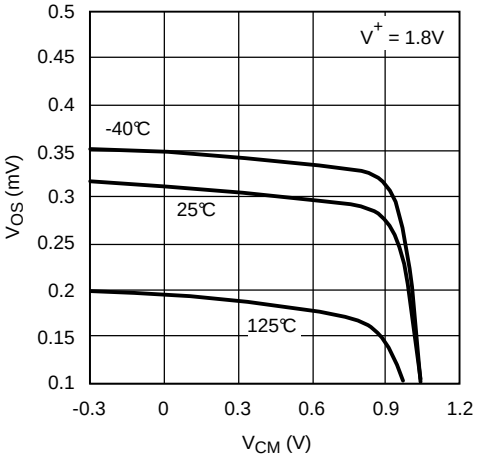


Figure 8.

V_{OS} vs. V_{CM}

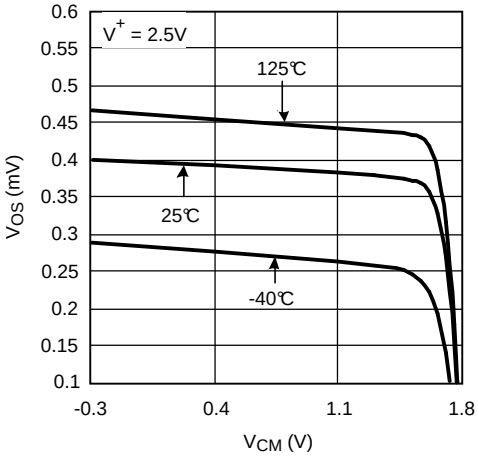


Figure 9.

V_{OS} vs. V_{CM}

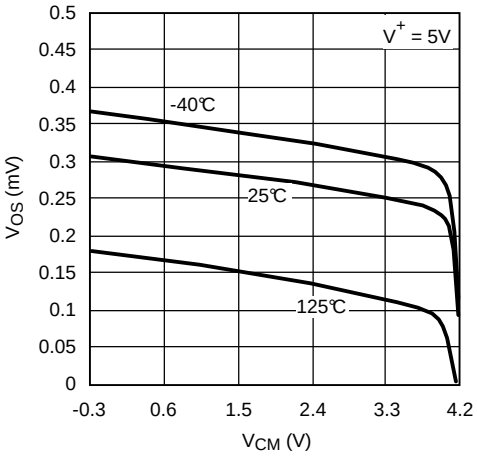


Figure 10.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = Supply Voltage = 5V, V_{CM} = V^+/2, V_{EN} = V^+.

V_{OS} vs. Supply Voltage

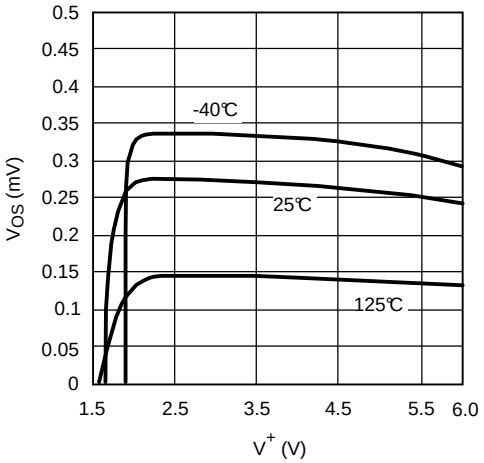


Figure 11.

Slew Rate vs. Supply Voltage

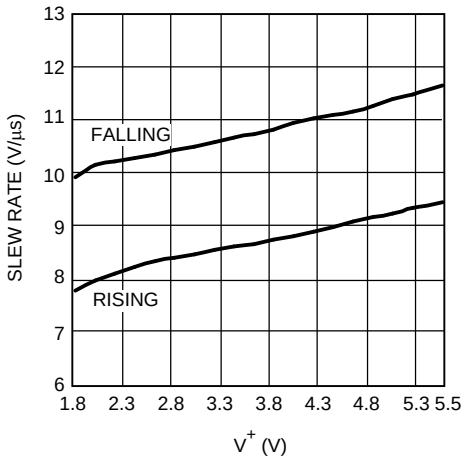


Figure 12.

Supply Current vs. Enable Pin Voltage (LMV791)

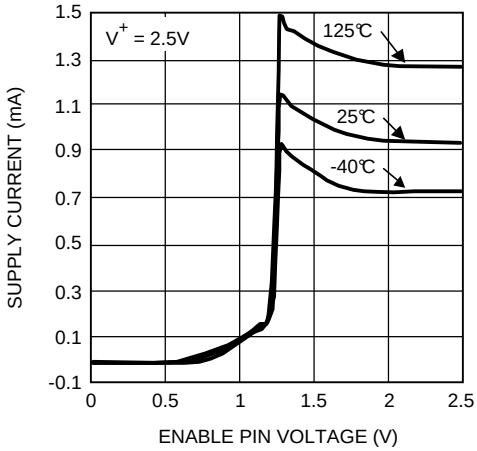


Figure 13.

Supply Current vs. Enable Pin Voltage(LMV791)

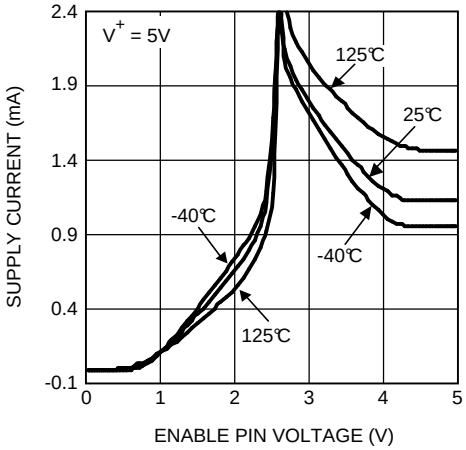


Figure 14.

Supply Current vs. Enable Pin Voltage (LMV792)

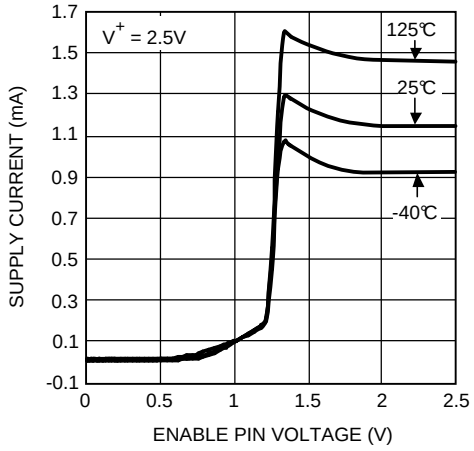


Figure 15.

Supply Current vs. Enable Pin Voltage (LMV792)

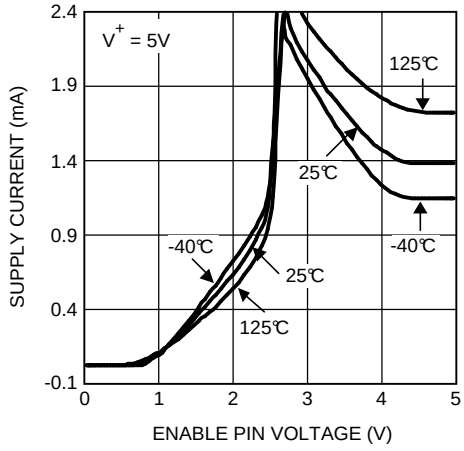


Figure 16.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = Supply Voltage = 5V, V_{CM} = V^+/2, V_{EN} = V^+.

Input Bias Current vs. V_{CM}

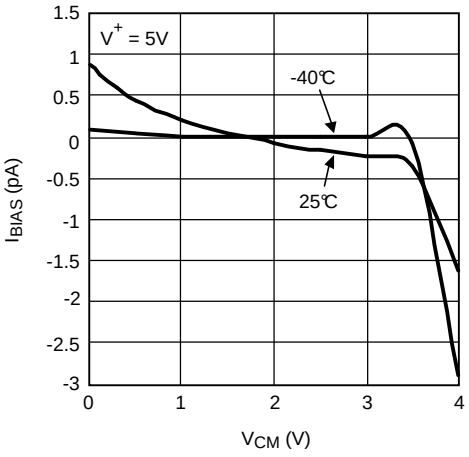


Figure 17.

Input Bias Current vs. V_{CM}

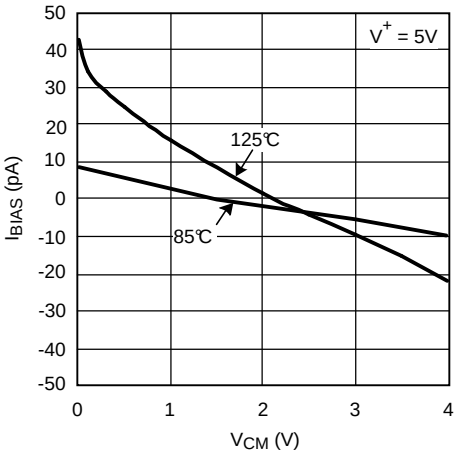


Figure 18.

Sourcing Current vs. Supply Voltage

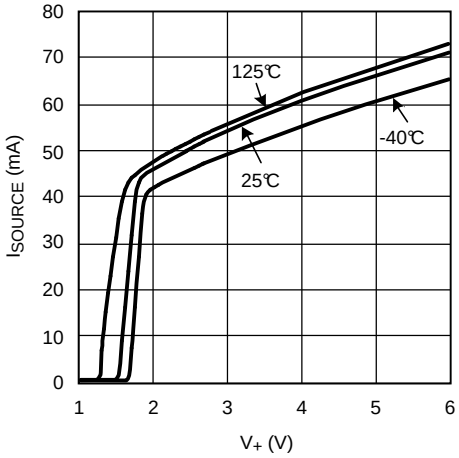


Figure 19.

Sinking Current vs. Supply Voltage

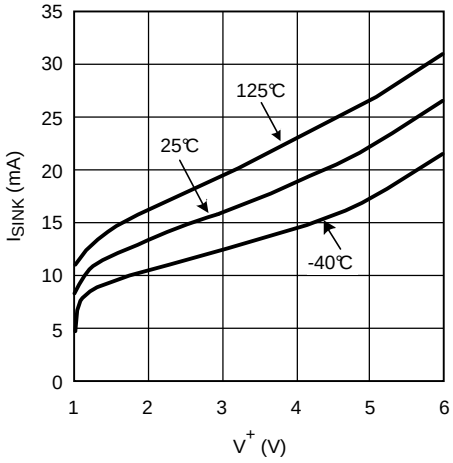


Figure 20.

Sourcing Current vs. Output Voltage

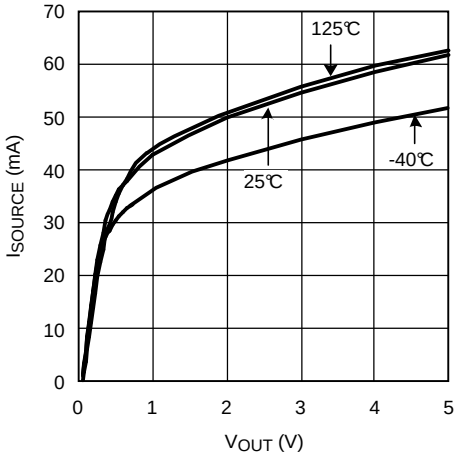


Figure 21.

Sinking Current vs. Output Voltage

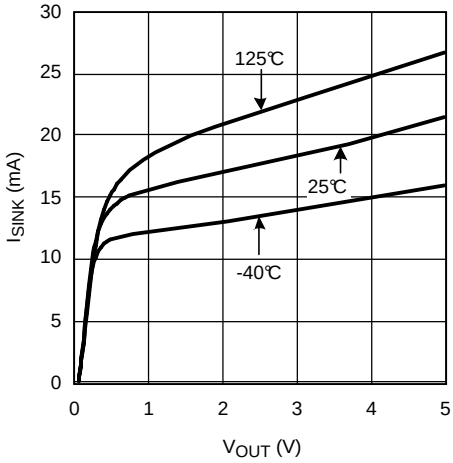


Figure 22.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = Supply Voltage = 5V, V_{CM} = V^+/2, V_{EN} = V^+.

Positive Output Swing vs. Supply Voltage

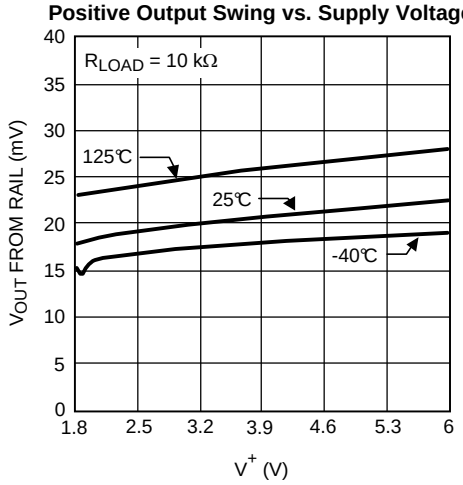


Figure 23.

Negative Output Swing vs. Supply Voltage

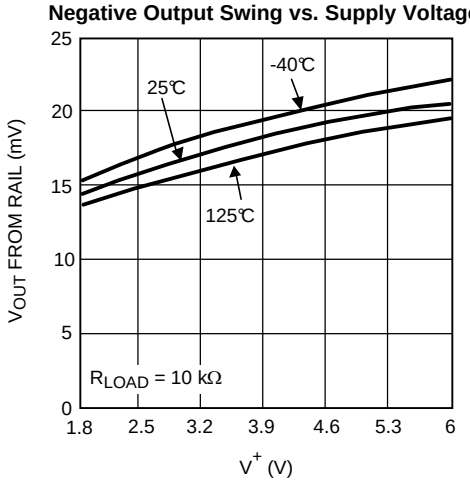


Figure 24.

Positive Output Swing vs. Supply Voltage

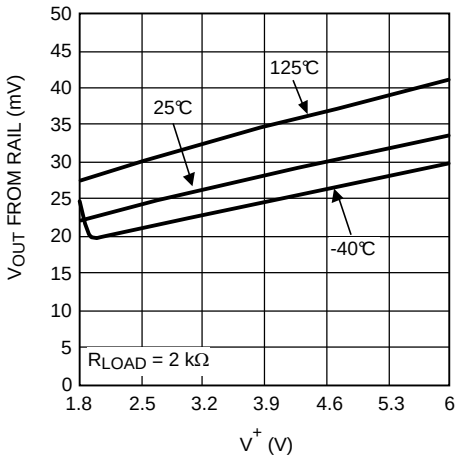


Figure 25.

Negative Output Swing vs. Supply Voltage

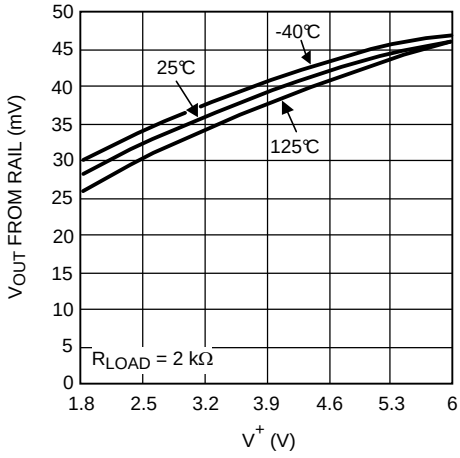


Figure 26.

Positive Output Swing vs. Supply Voltage

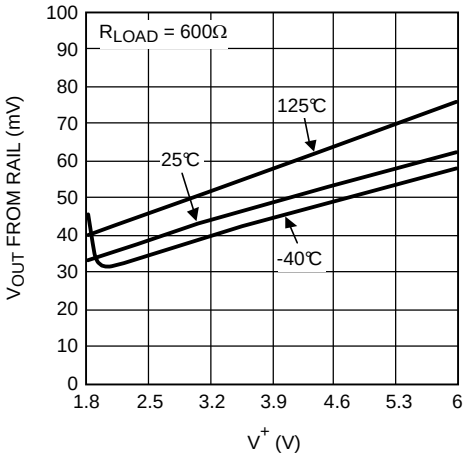


Figure 27.

Negative Output Swing vs. Supply Voltage

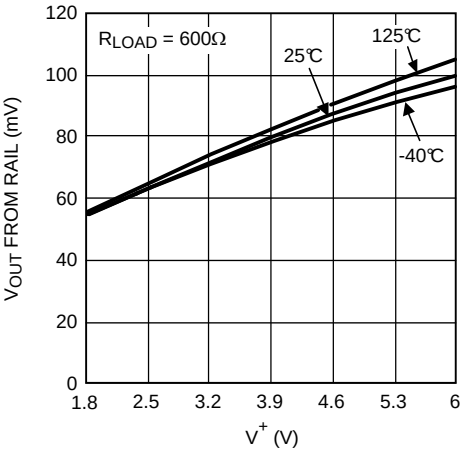


Figure 28.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = Supply Voltage = 5V, V_{CM} = V^+/2, V_{EN} = V^+.

Input Referred Voltage Noise vs. Frequency

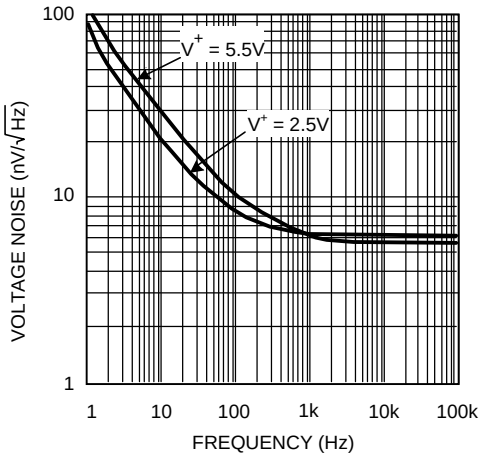


Figure 29.

Time Domain Voltage Noise

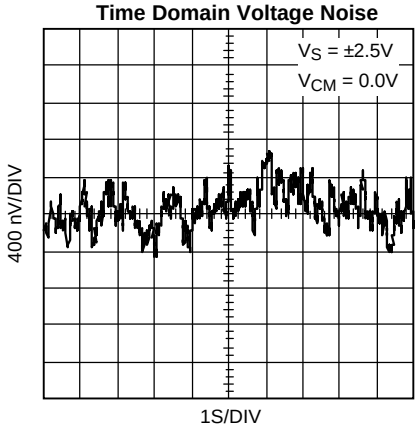


Figure 30.

Overshoot and Undershoot vs. C_{LOAD}

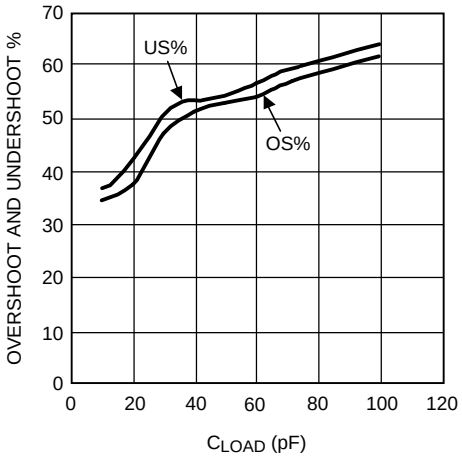


Figure 31.

THD+N vs. Peak-to-Peak Output Voltage (V_{OUT})

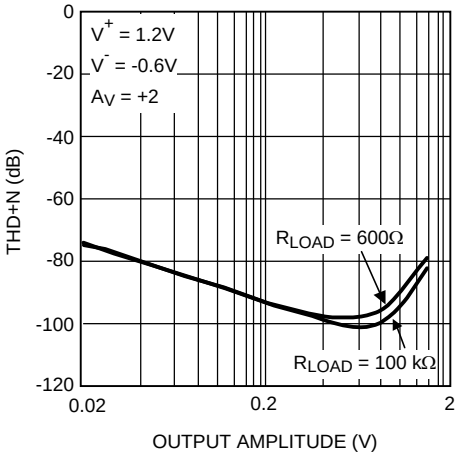


Figure 32.

THD+N vs. Peak-to-Peak Output Voltage (V_{OUT})

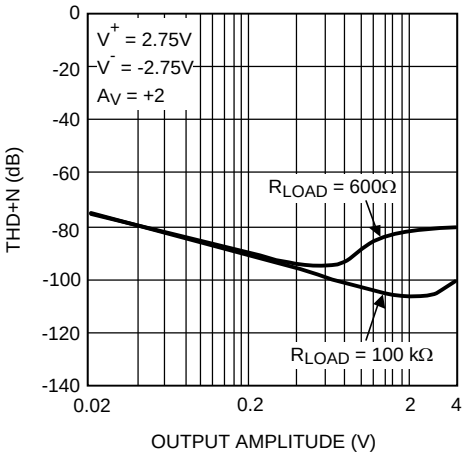


Figure 33.

THD+N vs. Frequency

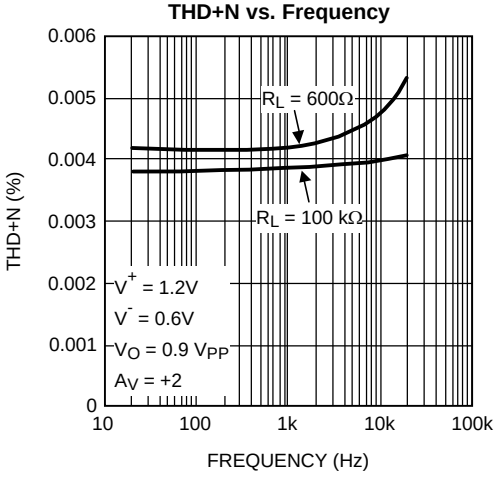


Figure 34.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = Supply Voltage = 5V, V_{CM} = V^+/2, V_{EN} = V^+.

THD+N vs. Frequency

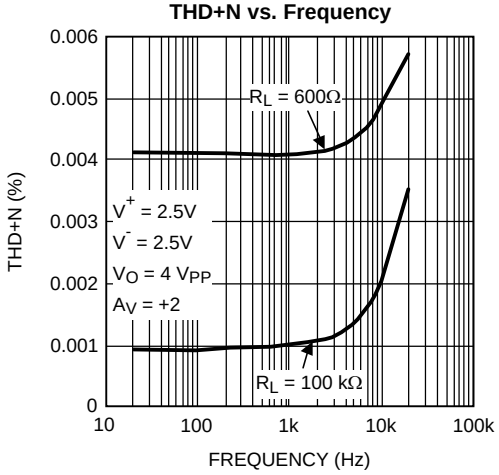


Figure 35.

Open Loop Gain and Phase with Capacitive Load

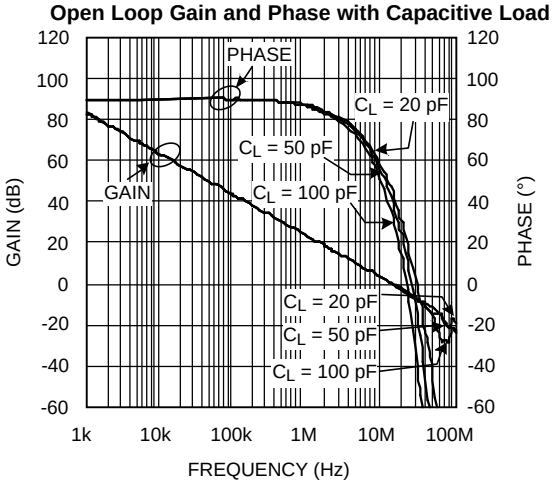


Figure 36.

Open Loop Gain and Phase with Resistive Load

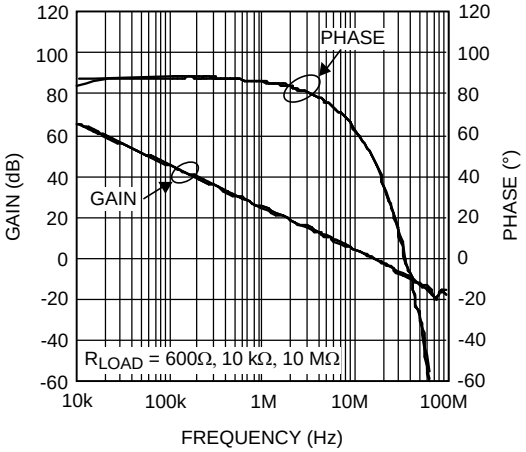


Figure 37.

Closed Loop Output Impedance vs. Frequency

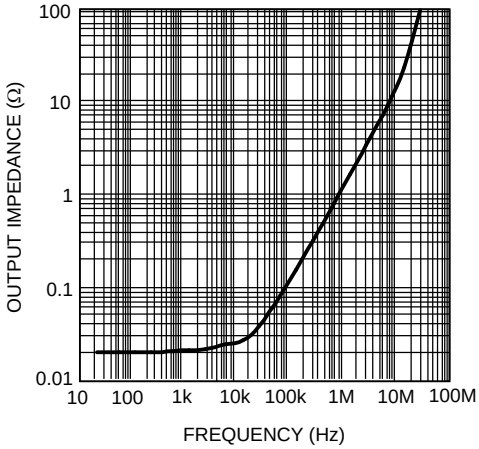


Figure 38.

Crosstalk Rejection

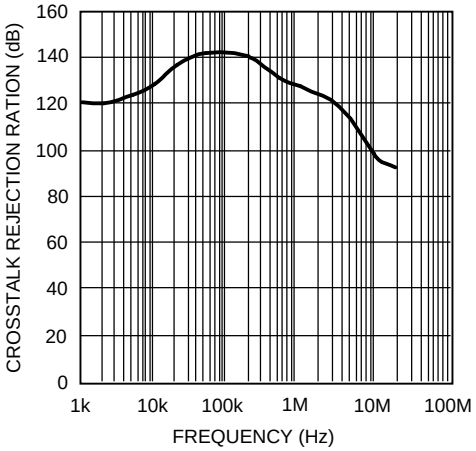


Figure 39.

Small Signal Transient Response, A_V = +1

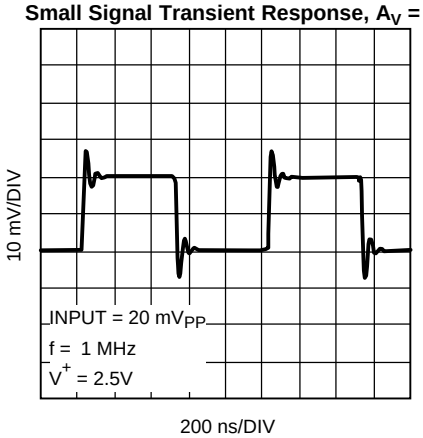


Figure 40.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = Supply Voltage = 5V, V_{CM} = V^+/2, V_{EN} = V^+.

Large Signal Transient Response, A_V = +1

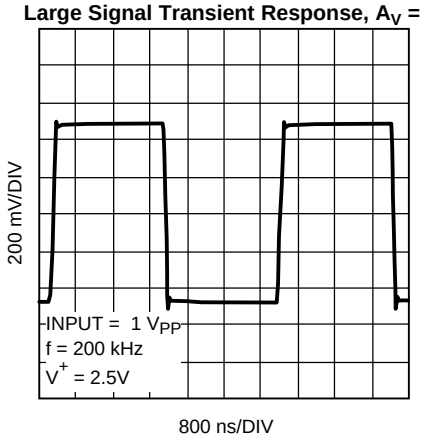


Figure 41.

Small Signal Transient Response, A_V = +1

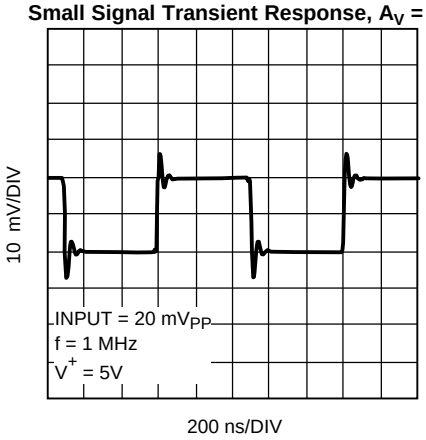


Figure 42.

Large Signal Transient Response, A_V = +1

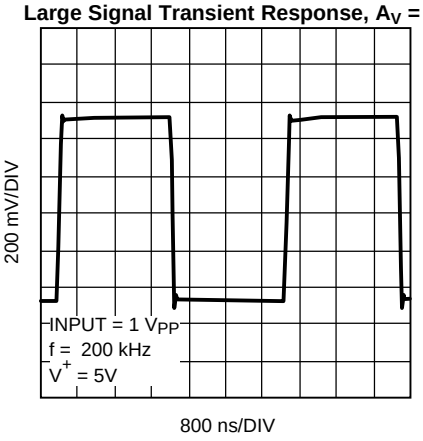


Figure 43.

Phase Margin vs. Capacitive Load (Stability)

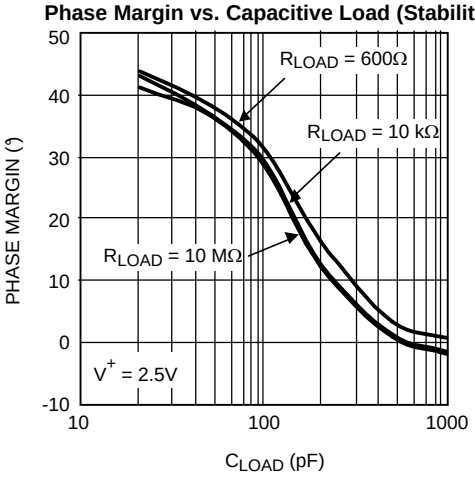


Figure 44.

Phase Margin vs. Capacitive Load (Stability)

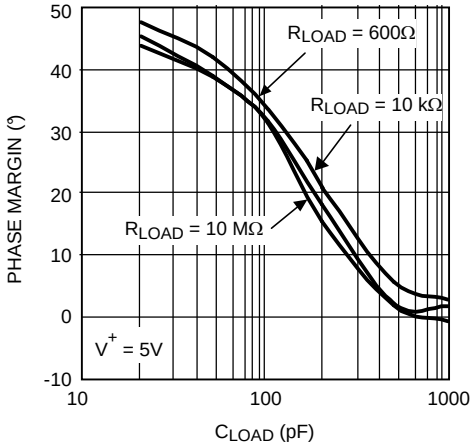


Figure 45.

Positive PSRR vs. Frequency

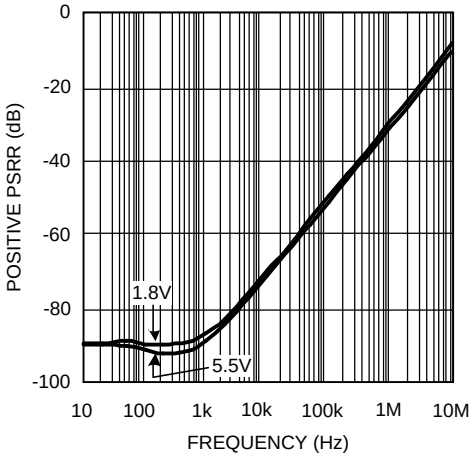


Figure 46.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = Supply Voltage = 5V, V_{CM} = V^+/2, V_{EN} = V^+.

Negative PSRR vs. Frequency

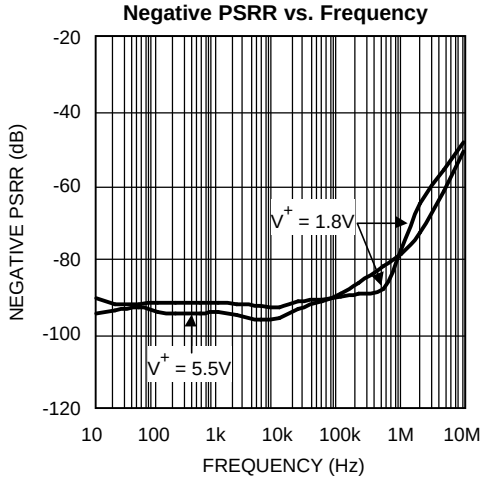


Figure 47.

CMRR vs. Frequency

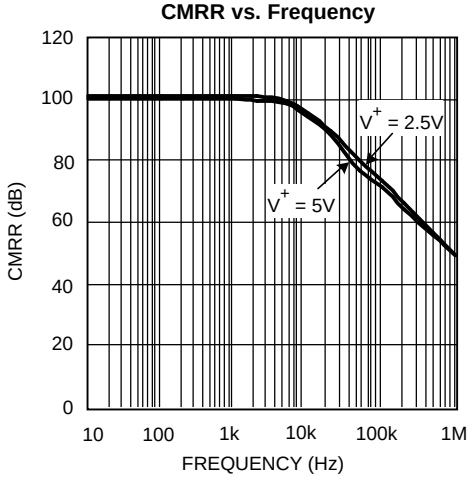


Figure 48.

Input Common Mode Capacitance vs. V_{CM}

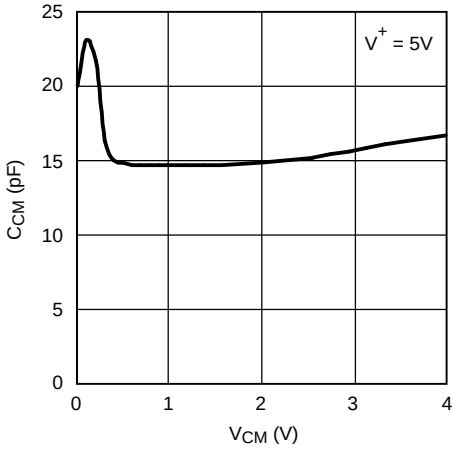


Figure 49.

APPLICATION INFORMATION

ADVANTAGES OF THE LMV791/LMV792

Wide Bandwidth at Low Supply Current

The LMV791 and LMV792 are high performance op amps that provide a unity gain bandwidth of 17 MHz while drawing a low supply current of 1.15 mA. This makes them ideal for providing wideband amplification in portable applications. The enable and shutdown feature can also be used to design more power efficient systems that offer wide bandwidth and high performance while consuming less average power.

Low Input Referred Noise and Low Input Bias Current

The LMV791/LMV792 have a very low input referred voltage noise density (5.8 nV/$\sqrt{Hz}$ at 1 kHz). A CMOS input stage ensures a small input bias current (100 fA) and low input referred current noise (0.01 pA/$\sqrt{Hz}$). This is very helpful in maintaining signal fidelity, and makes the LMV791 and LMV792 ideal for audio and sensor based applications.

Low Supply Voltage

The LMV791 and the LMV792 have performance ensured at 2.5V and 5V supply. The LMV791 family is ensured to be operational at all supply voltages between 2.0V and 5.5V, for ambient temperatures ranging from −40°C to 125°C, thus utilizing the entire battery lifetime. The LMV791 and LMV792 are also ensured to be operational at 1.8V supply voltage, for temperatures between 0°C and 125°C. This makes the LMV791 family ideal for usage in low-voltage commercial applications.

RRO and Ground Sensing

Rail-to-rail output swing provides maximum possible dynamic range at the output. This is particularly important when operating at low supply voltages. An innovative positive feedback scheme is used to boost the current drive capability of the output stage. This allows the LMV791 and the LMV792 to source more than 40 mA of current at 1.8V supply. This also limits the performance of the LMV791 family as comparators, and hence the usage of the LMV791 and the LMV792 in an open-loop configuration is not recommended. The input common-mode range includes the negative supply rail which allows direct sensing at ground in single supply operation.

Enable and Shutdown Features

The LMV791 family is ideal for battery powered systems. With a low supply current of 1.15 mA and a shutdown current of 140 nA typically, the LMV791 and LMV792 allow the designer to maximize battery life. The enable pin of the LMV791 and the LMV792 allows the op amp to be turned off and reduce its supply current to less than 1 µA. To power on the op amp the enable pin should be higher than V^+ - 0.5V, where V^+ is the positive supply. To disable the op amp, the enable pin voltage should be less than V^- + 0.5V, where V^- is the negative supply.

Small Size

The small footprint of the LMV791 and the LMV792 package saves space on printed circuit boards, and enables the design of smaller electronic products, such as cellular phones, pagers, or other portable systems. Long traces between the signal source and the opamp make the signal path susceptible to noise. By using a physically smaller LMV791 and LMV792 package, the opamp can be placed closer to the signal source, reducing noise pickup and increasing signal integrity.

CAPACITIVE LOAD TOLERANCE

The LMV791 and LMV792 can directly drive 120 pF in unity-gain without oscillation. The unity-gain follower is the most sensitive configuration to capacitive loading. Direct capacitive loading reduces the phase margin of amplifiers. The combination of the amplifier's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation. To drive a heavier capacitive load, the circuit in Figure 50 can be used.

In Figure 50, the isolation resistor R_{ISO} and the load capacitor C_L form a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of R_{ISO}. The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. Increased R_{ISO} would, however, result in a reduced output swing and short circuit current.

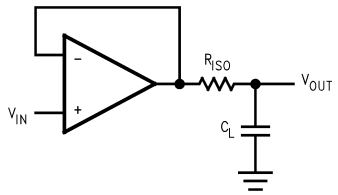


Figure 50. Isolation of C_L to Improve Stability

INPUT CAPACITANCE AND FEEDBACK CIRCUIT ELEMENTS

The LMV791 family has a very low input bias current (100 fA) and a low 1/f noise corner frequency (400 Hz), which makes it ideal for sensor applications. However, to obtain this performance a large CMOS input stage is used, which adds to the input capacitance of the op-amp, C_{IN}. Though this does not affect the DC and low frequency performance, at higher frequencies the input capacitance interacts with the input and the feedback impedances to create a pole, which results in lower phase margin and gain peaking. This can be controlled by being selective in the use of feedback resistors, as well as by using a feedback capacitance, C_F. For example, in the inverting amplifier shown in Figure 51, if C_{IN} and C_F are ignored and the open loop gain of the op amp is considered infinite then the gain of the circuit is $-R_2/R_1$. An op amp, however, usually has a dominant pole, which causes its gain to drop with frequency. Hence, this gain is only valid for DC and low frequency. To understand the effect of the input capacitance coupled with the non-ideal gain of the op amp, the circuit needs to be analyzed in the frequency domain using a Laplace transform.

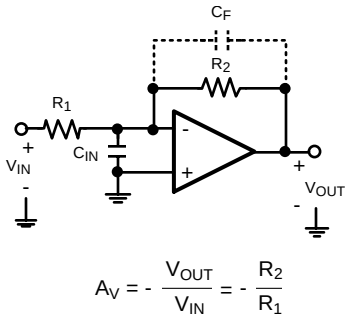


Figure 51. Inverting Amplifier

For simplicity, the op amp is modelled as an ideal integrator with a unity gain frequency of A_0 . Hence, its transfer function (or gain) in the frequency domain is A_0/s. Solving the circuit equations in the frequency domain, ignoring C_F for the moment, results in an expression for the gain shown in Equation 1.

$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{-R_2/R_1}{\left[1 + \frac{s}{\left(\frac{A_0 R_1}{R_1 + R_2}\right)} + \frac{s^2}{\left(\frac{A_0}{C_{IN} R_2}\right)}\right]} \tag{1}$$

It can be inferred from the denominator of the transfer function that it has two poles, whose expressions can be obtained by solving for the roots of the denominator and are shown in Equation 2.

$$P_{1,2} = \frac{-1}{2C_{IN}}\left[\frac{1}{R_1} + \frac{1}{R_2} \pm \sqrt{\left(\frac{1}{R_1} + \frac{1}{R_2}\right)^2 - \frac{4\,A_0 C_{IN}}{R_2}}\right] \tag{2}$$

Equation 2 shows that as the values of R_1 and R_2 are increased, the magnitude of the poles, and hence the bandwidth of the amplifier, is reduced. This theory is verified by using different values of R_1 and R_2 in the circuit shown in Figure 50 and by comparing their frequency responses. In Figure 52 the frequency responses for three different values of R_1 and R_2 are shown. When both R_1 and R_2 are 1 kΩ, the response is flattest and widest; whereas, it narrows and peaks significantly when both their values are changed to 10 kΩ or 30 kΩ. So it is advisable to use lower values of R_1 and R_2 to obtain a wider and flatter response. Lower resistances also help in high sensitivity circuits since they add less noise.

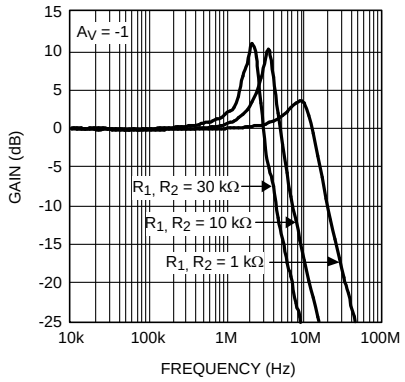


Figure 52. Gain Peaking Caused by Large R_1, R_2

A way of reducing the gain peaking is by adding a feedback capacitance C_F in parallel with R_2. This introduces another pole in the system and prevents the formation of pairs of complex conjugate poles which cause the gain to peak. Figure 53 shows the effect of C_F on the frequency response of the circuit. Adding a capacitance of 2 pF removes the peak, while a capacitance of 5 pF creates a much lower pole and reduces the bandwidth excessively.

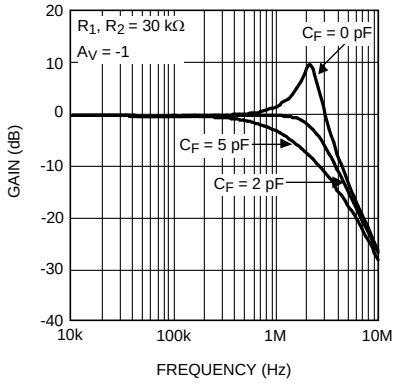


Figure 53. Gain Peaking Eliminated by C_F

AUDIO PREAMPLIFIER WITH BANDPASS FILTERING

With low input referred voltage noise, low supply voltage and low supply current, and a low harmonic distortion, the LMV791 family is ideal for audio applications. Its wide unity gain bandwidth allows it to provide large gain for a wide range of frequencies and it can be used to design a preamplifier to drive a load of as low as 600Ω with less than 0.01% distortion. Two amplifier circuits are shown in Figure 54 and Figure 55. Figure 54 is an inverting amplifier, with a 10 kΩ feedback resistor, R_2, and a 1kΩ input resistor, R_1, and hence provides a gain of −10. Figure 55 is a non-inverting amplifier, using the same values of $R_1$and R_2, and provides a gain of 11. In either of these circuits, the coupling capacitor C_{C1} decides the lower frequency at which the circuit starts providing gain, while the feedback capacitor C_F decides the frequency at which the gain starts dropping off. Figure 56 shows the frequency response of the inverting amplifier with different values of C_F.

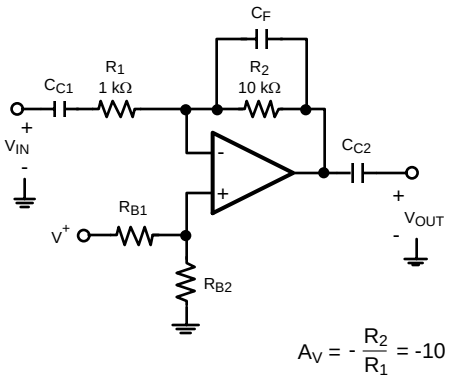


Figure 54. Inverting Audio Preamplifier

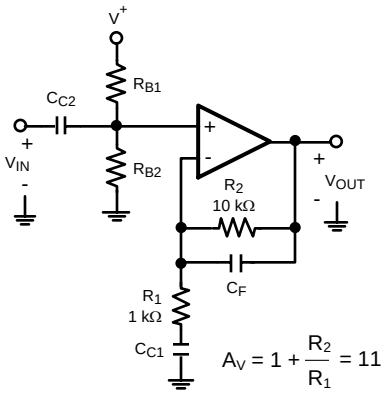


Figure 55. Non-inverting Audio Preamplifier

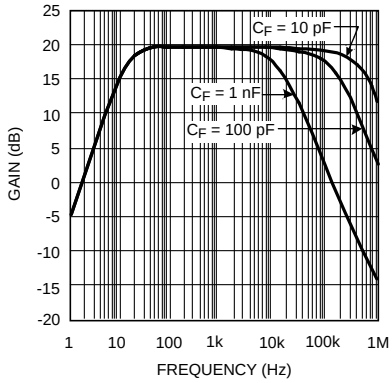


Figure 56. Frequency Response of the Inverting Audio Preamplifier

TRANSIMPEDANCE AMPLIFIER

CMOS input op amps are often used in transimpedance applications as they have an extremely high input impedance. A transimpedance amplifier converts a small input current into a voltage. This current is usually generated by a photodiode. The transimpedance gain, measured as the ratio of the output voltage to the input current, is expected to be large and wide-band. Since the circuit deals with currents in the range of a few nA, low noise performance is essential. The LMV791/LMV792 are CMOS input op amps providing wide bandwidth and low noise performance, and are hence ideal for transimpedance applications.

Usually, a transimpedance amplifier is designed on the basis of the current source driving the input. A photodiode is a very common capacitive current source, which requires transimpedance gain for transforming its miniscule current into easily detectable voltages. The photodiode and amplifier's gain are selected with respect to the speed and accuracy required of the circuit. A faster circuit would require a photodiode with lesser capacitance and a faster amplifier. A more sensitive circuit would require a sensitive photodiode and a high gain. A typical transimpedance amplifier is shown in Figure 57. The output voltage of the amplifier is given by the equation $V_{OUT} = -I_{IN}R_F$. Since the output swing of the amplifier is limited, R_F should be selected such that all possible values of I_{IN} can be detected.

The LMV791/LMV792 have a large gain-bandwidth product (17 MHz), which enables high gains at wide bandwidths. A rail-to-rail output swing at 5.5V supply allows detection and amplification of a wide range of input currents. A CMOS input stage with negligible input current noise and low input voltage noise allows the LMV791/LMV792 to provide high fidelity amplification for wide bandwidths. These properties make the LMV791/LMV792 ideal for systems requiring wide-band transimpedance amplification.

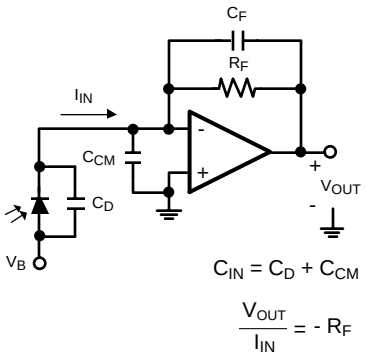


Figure 57. Photodiode Transimpedance Amplifier

As mentioned earlier, the following parameters are used to design a transimpedance amplifier: the amplifier gain-bandwidth product, A_0; the amplifier input capacitance, C_{CM}; the photodiode capacitance, C_D; the transimpedance gain required, R_F; and the amplifier output swing. Once a feasible R_F is selected using the amplifier output swing, these numbers can be used to design an amplifier with the desired transimpedance gain and a maximally flat frequency response.

An essential component for obtaining a maximally flat response is the feedback capacitor, C_F. The capacitance seen at the input of the amplifier, C_{IN}, combined with the feedback capacitor, R_F, generate a phase lag which causes gain-peaking and can destabilize the circuit. C_{IN} is usually just the sum of C_D and C_{CM}. The feedback capacitor C_F creates a pole, f_P in the noise gain of the circuit, which neutralizes the zero in the noise gain, f_Z, created by the combination of R_F and C_{IN}. If properly positioned, the noise gain pole created by C_F can ensure that the slope of the gain remains at 20 dB/decade till the unity gain frequency of the amplifier is reached, thus ensuring stability. As shown in Figure 58, f_P is positioned such that it coincides with the point where the noise gain intersects the op amp's open loop gain. In this case, f_P is also the overall 3 dB frequency of the transimpedance amplifier. The value of C_F needed to make it so is given by Equation 3. A larger value of C_F causes excessive reduction of bandwidth, while a smaller value fails to prevent gain peaking and instability.

$$C_F = \frac{1 + \sqrt{1 + 4\pi R_F C_{IN} A_0}}{2\pi R_F A_0} \quad (3)$$

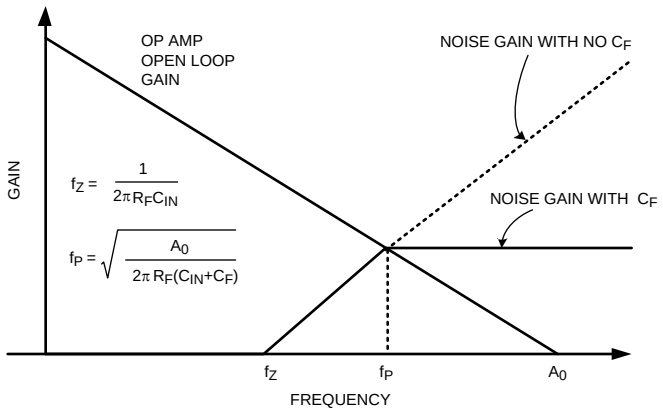


Figure 58. C_F Selection for Stability

Calculating C_F from Equation 3 can sometimes return unreasonably small values (<1 pF), especially for high speed applications. In these cases, its often more practical to use the circuit shown in Figure 59 in order to allow more reasonable values. In this circuit, the capacitance C_F' is (1+ R_B/R_A) time the effective feedback capacitance, C_F. A larger capacitor can now be used in this circuit to obtain a smaller effective capacitance.

For example, if a C_F of 0.5 pF is needed, while only a 5 pF capacitor is available, R_B and R_A can be selected such that R_B/R_A = 9. This would convert a C_F' of 5 pF into a C_F of 0.5 pF. This relationship holds as long as R_A << R_F.

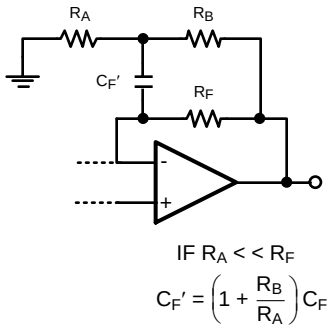


Figure 59. Obtaining Small C_F from large C_F'

LMV791 AS A TRANSIMPEDANCE AMPLIFIER

The LMV791 was used to design a number of amplifiers with varying transimpedance gains and source capacitances. The gains, bandwidths and feedback capacitances of the circuits created are summarized in Table 1. The frequency responses are presented in Figure 60 and Figure 61. The feedback capacitances are slightly different from the formula in Equation 3, since the parasitic capacitance of the board and the feedback resistor R_F had to be accounted for.

Table 1.

Transimpedance, A_{TI}	C_{IN}	C_F	3 dB Frequency
470000	50 pF	1.5 pF	350 kHz
470000	100 pF	2.0 pF	250 kHz
470000	200 pF	3.0 pF	150 kHz
47000	50 pF	4.5 pF	1.5 MHz
47000	100 pF	6.0 pF	1 MHz
47000	200 pF	9.0 pF	700 kHz

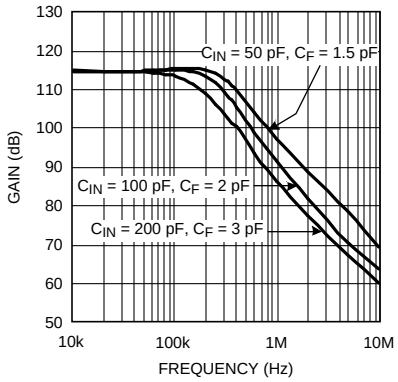


Figure 60. Frequency Response for A_{TI} = 470000

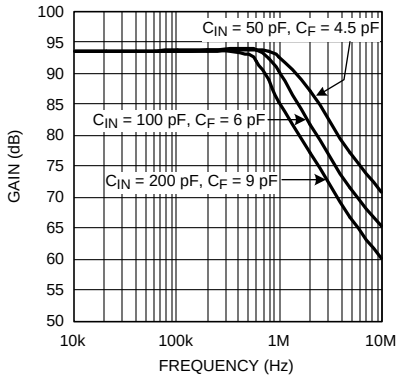


Figure 61. Frequency Response for A_{TI} = 47000

HIGH GAIN WIDEBAND TRANSIMPEDANCE AMPLIFIER USING THE LMV792

The LMV792, dual, low noise, wide bandwidth, CMOS input op amp IC can be used for compact, robust and integrated solutions for sensing and amplifying wide-band signals obtained from sensitive photodiodes. One of the two op amps available can be used to obtain transimpedance gain while the other can be used for amplifying the output voltage to further enhance the transimpedance gain. The wide bandwidth of the op amps (17 MHz) ensures that they are capable of providing high gain for a wide range of frequencies. The low input referred noise (5.8 nV/$\sqrt{Hz}$) allows the amplifier to deliver an output with a high SNR (signal to noise ratio). The small VSSOP-10 footprint saves space on printed circuit boards and allows ease of design in portable products.

The circuit shown in Figure 62, has the first op amp acting as a transimpedance amplifier with a gain of 47000, while the second stage provides a voltage gain of 10. This provides a total transimpedance gain of 470000 with a −3 dB bandwidth of about 1.5 MHz, for a total input capacitance of 50 pF. The frequency response for the circuit is shown in Figure 63

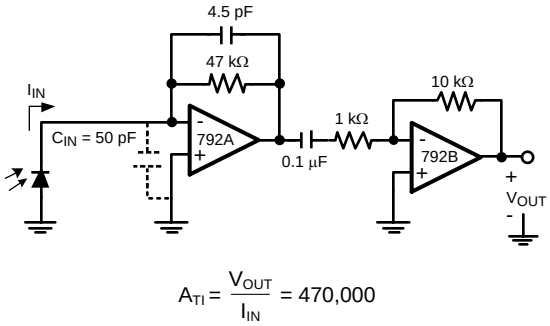


Figure 62. 1.5 MHz Transimpedance Amplifier, with A_{TI} = 470000

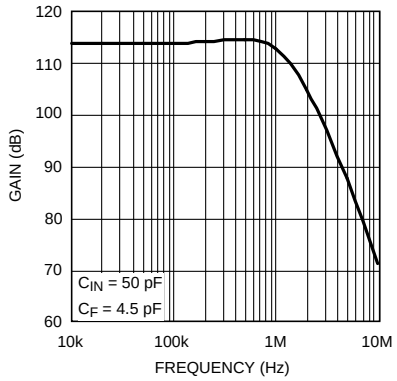


Figure 63. 1.5 MHz Transimpedance Amplifier Frequency Response

SENSOR INTERFACES

The low input bias current and low input referred noise of the LMV791 and LMV792 make them ideal for sensor interfaces. These circuits are required to sense voltages of the order of a few µV, and currents amounting to less than a nA, and hence the op amp needs to have low voltage noise and low input bias current. Typical applications include infra-red (IR) thermometry, thermocouple amplifiers and pH electrode buffers. Figure 64 is an example of a typical circuit used for measuring IR radiation intensity, often used for estimating the temperature of an object from a distance. The IR sensor generates a voltage proportional to I, which is the intensity of the IR radiation falling on it. As shown in Figure 64, K is the constant of proportionality relating the voltage across the IR sensor (V_{IN}) to the radiation intensity, I. The resistances R_A and R_B are selected to provide a high gain to amplify this voltage, while C_F is added to filter out the high frequency noise.

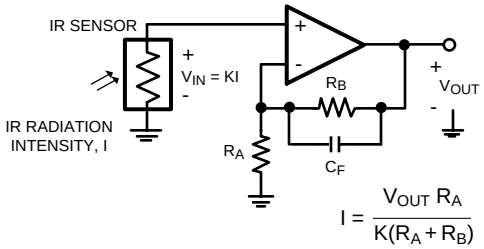


Figure 64. IR Radiation Sensor

REVISION HISTORY

Changes from Revision E (March 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	21

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMV791MK	ACTIVE	SOT	DDC	6	1000	TBD	Call TI	Call TI	-40 to 125	AS1A	Samples
LMV791MK/NOPB	ACTIVE	SOT	DDC	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AS1A	Samples
LMV791MKX/NOPB	ACTIVE	SOT	DDC	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AS1A	Samples
LMV792MM	ACTIVE	VSSOP	DGS	10	1000	TBD	Call TI	Call TI	-40 to 125	AX2A	Samples
LMV792MM/NOPB	ACTIVE	VSSOP	DGS	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AX2A	Samples
LMV792MMX	ACTIVE	VSSOP	DGS	10	3500	TBD	Call TI	Call TI	-40 to 125	AX2A	Samples
LMV792MMX/NOPB	ACTIVE	VSSOP	DGS	10	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		AX2A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

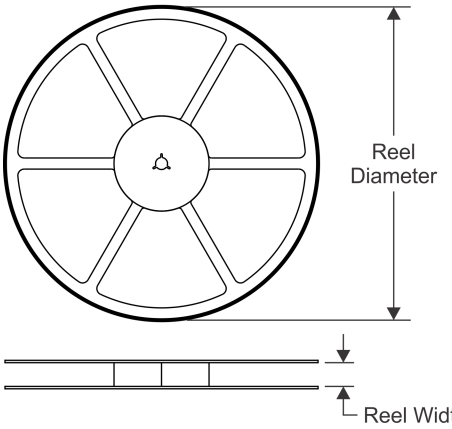
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

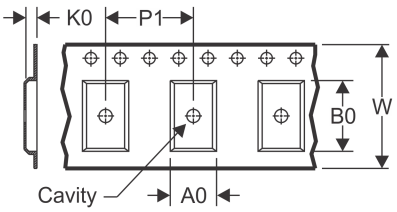
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

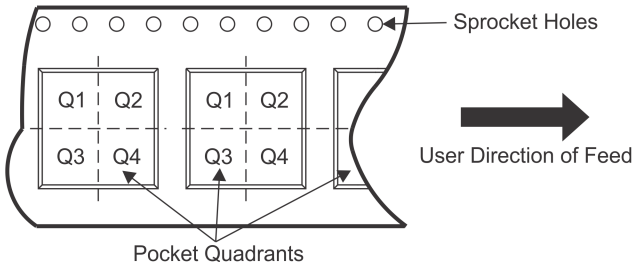


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

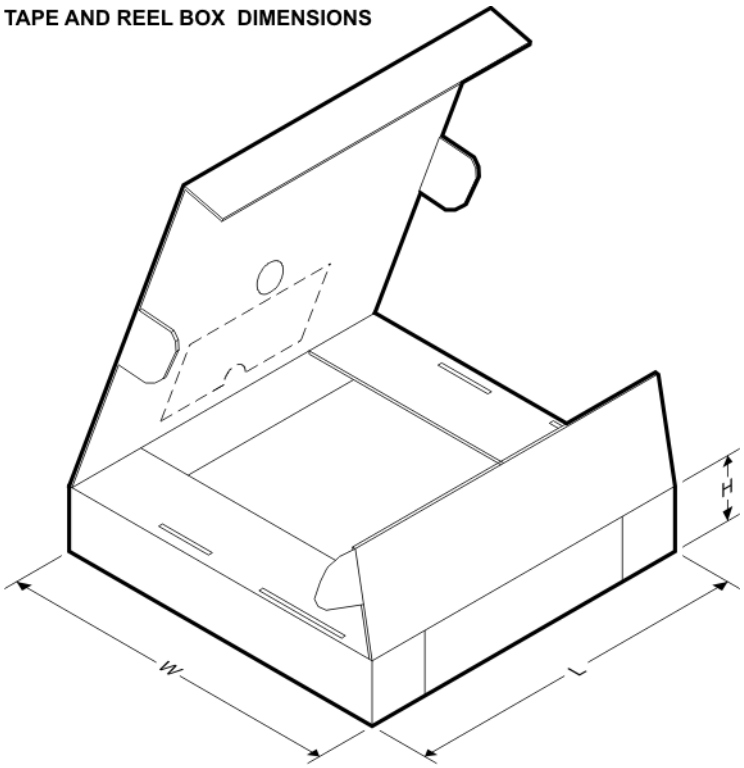
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV791MK	SOT	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV791MK/NOPB	SOT	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV791MKX/NOPB	SOT	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV792MM	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV792MM/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV792MMX	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

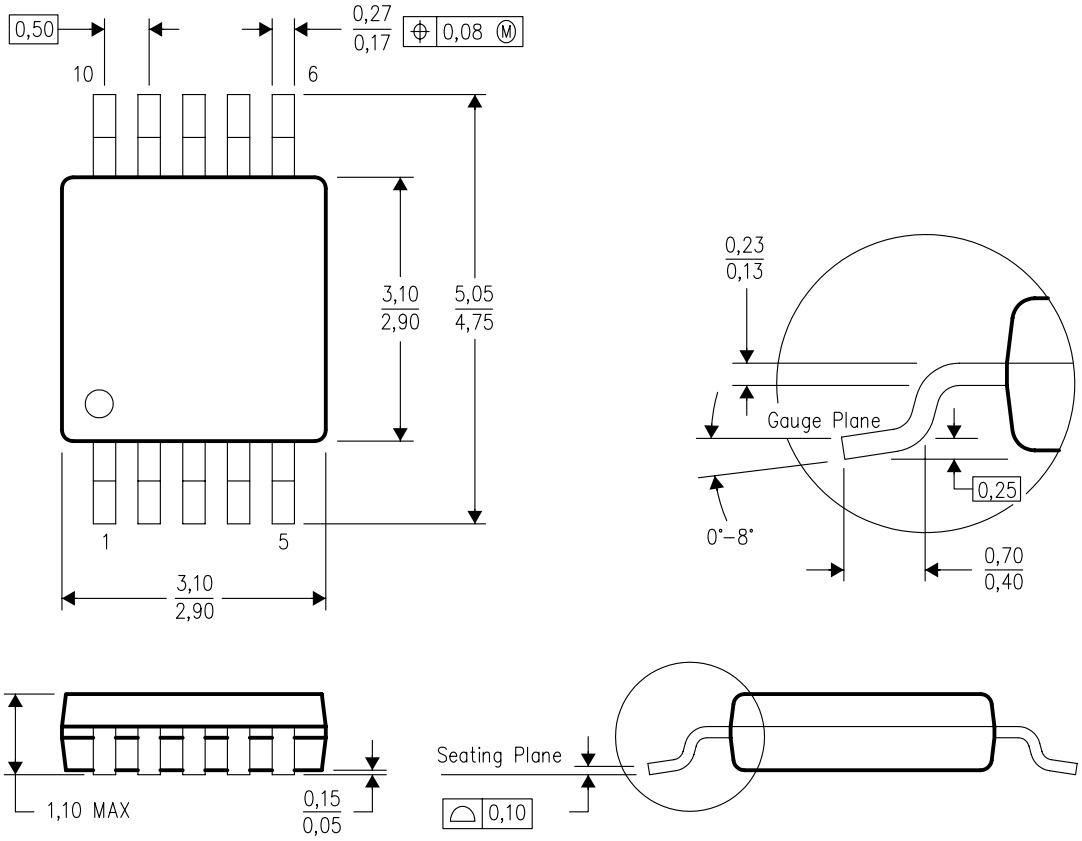
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV791MK	SOT	DDC	6	1000	210.0	185.0	35.0
LMV791MK/NOPB	SOT	DDC	6	1000	210.0	185.0	35.0
LMV791MKX/NOPB	SOT	DDC	6	3000	210.0	185.0	35.0
LMV792MM	VSSOP	DGS	10	1000	210.0	185.0	35.0
LMV792MM/NOPB	VSSOP	DGS	10	1000	210.0	185.0	35.0
LMV792MMX	VSSOP	DGS	10	3500	367.0	367.0	35.0

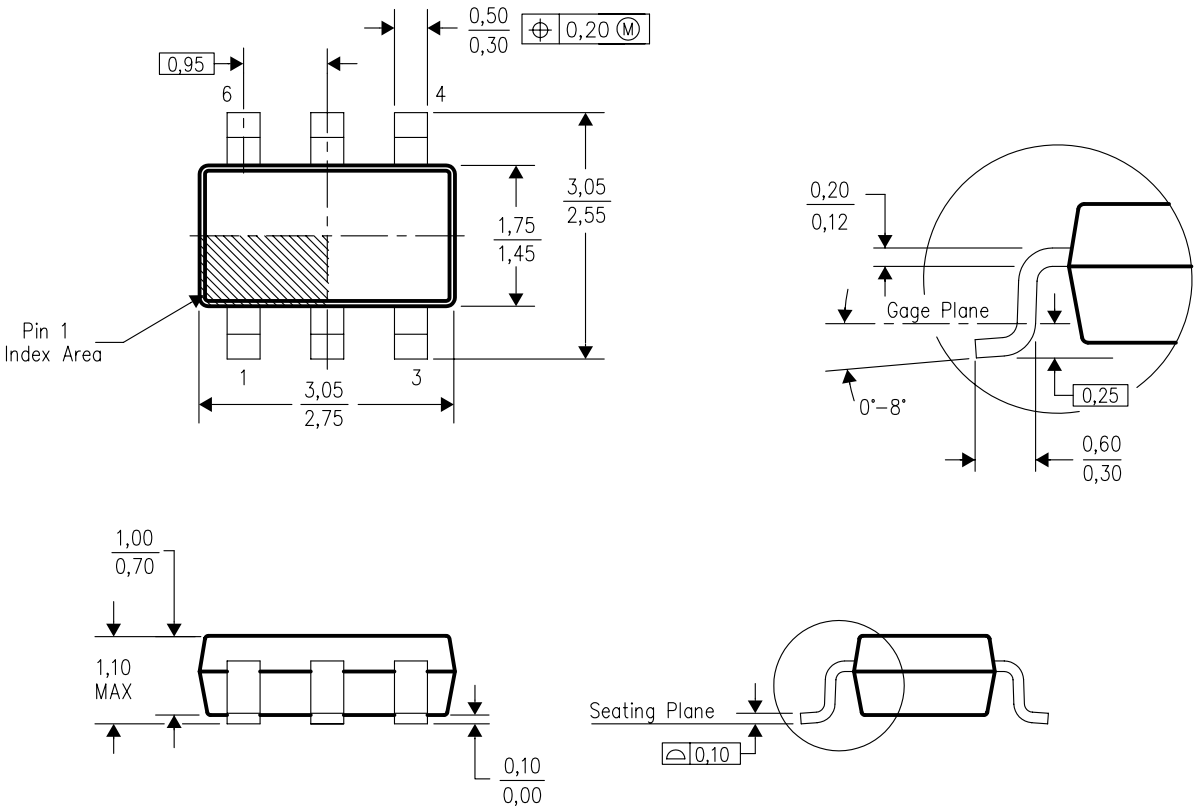
DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

DDC (R–PDSO–G6) PLASTIC SMALL–OUTLINE



4204403–3/E 06/05

NOTES:
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B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–193 variation AA (6 pin).

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