LM118JAN Operational Amplifier

Check for Samples: LM118JAN

FEATURES

- **15 MHz Small Signal Bandwidth**
- **Ensured 50V/µs Slew Rate**
- **Maximum Bias Current of 250 nA**
- **Operates from Supplies of ±5V to ±20V**
- **Internal Frequency Compensation**
- **Input and Output Overload Protected**
- **Pin Compatible with General Purpose Op Amps**

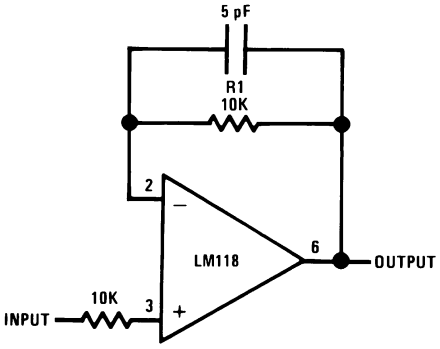
DESCRIPTION

The LM118 is a precision high speed operational amplifier designed for applications requiring wide bandwidth and high slew rate. It features a factor of ten increase in speed over general purpose devices without sacrificing DC performance.

The LM118 has internal unity gain frequency compensation. This considerably simplifies its application since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feed forward compensation will boost the slew rate to over 150V/µs and almost double the bandwidth. Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the 0.1% settling time to under 1 µs.

The high speed and fast settling time of this op amp makes it useful in A/D converters, oscillators, active filters, sample and hold circuits, or general purpose amplifiers. This device is easy to apply and offers an order of magnitude better AC performance than industry standards such as the LM709.

Fast Voltage Follower



Do not hard-wire as voltage follower (R1 ≥ 5 kΩ)

Connection Diagram

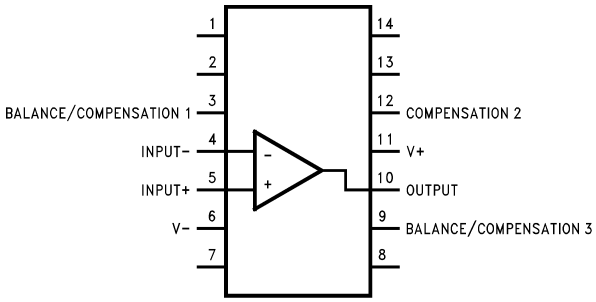
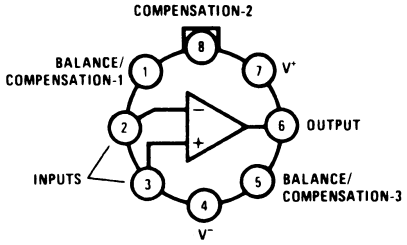


Figure 1. CDIP Package
Top View
See Package Number J0014A



Pin connections shown on schematic diagram and typical applications are for TO-5 package.

Figure 2. TO Package
Top View
See Package Number LMC0008C

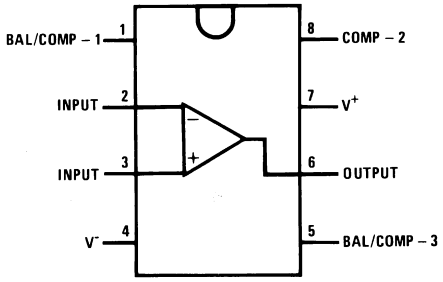


Figure 3. CDIP Package
Top View
See Package Number NAB0008A

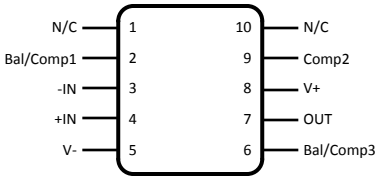
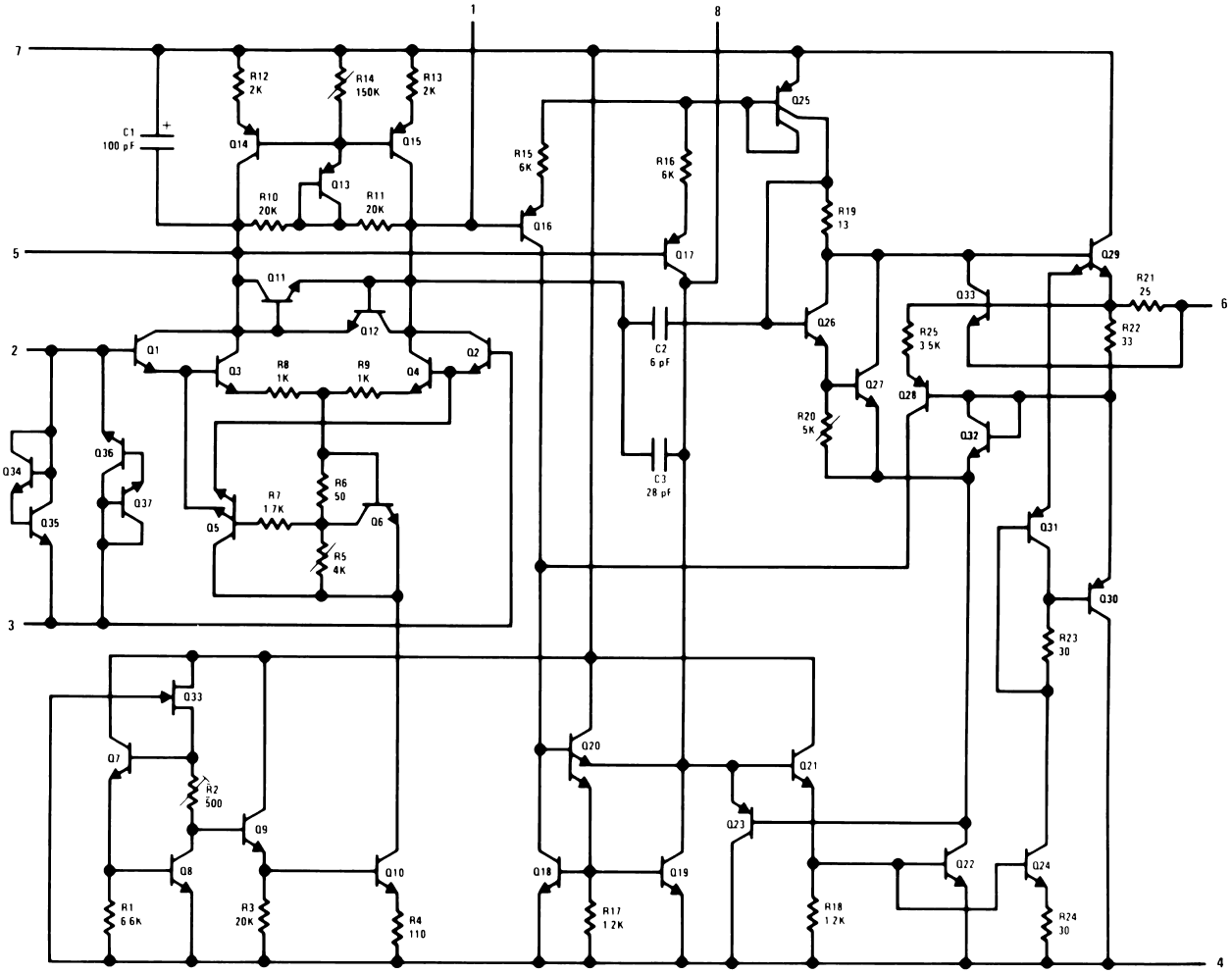


Figure 4. CLGA Package
Top View
See Package Number NAD0010A

Schematic Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

Supply Voltage			±20V
Power Dissipation(2)		8 LD TO	750mW
		8LD CDIP	1000mW
		14LD CDIP	1250mW
		10LD CLGA	600mW
Differential Input Current(3)			±10 mA
Input Voltage(4)			±15V
Output Short-Circuit Duration			Continuous
Operating Temperature Range			$-55°C \le T_A \le +125°C$
Thermal Resistance	θ_{JA}	8 LD TO (Still Air @ 0.5W)	160°C/W
		8 LD TO (500LF / Min Air flow @ 0.5W)	86°C/W
		8LD CDIP (Still Air @ 0.5W)	120°C/W
		8LD CDIP (500LF / Min Air flow @ 0.5W)	66°C/W
		14LD CDIP (Still Air @ 0.5W)	87°C/W
		14LD CDIP (500LF / Min Air flow @ 0.5W)	51°C/W
		10LD CLGA (Still Air @ 0.5W)	198°C/W
		10LD CLGA (500LF / Min Air flow @ 0.5W)	124°C/W
	θ_{JC}	8 LD TO	48°C/W
		8LD CDIP	17°C/W
		14LD CDIP	17°C/W
		10LD CLGA	22°C/W
Storage Temperature Range			$-65°C \le T_A \le +150°C$
Lead Temperature (Soldering, 10 seconds)			300°C
ESD Tolerance(5)			2000V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

(3) The inputs are shunted with back-to-back diodes for over voltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

(4) For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

(5) Human body model, 1.5 kΩ in series with 100 pF.

Quality Conformance Inspection

Mil-Std-883, Method 5005; Group A

Subgroup	Description	Temp°C
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55
12	Settling time at	25
13	Settling time at	125
14	Settling time at	-55

LM118JAN Electrical Characteristics DC Parameters

The following conditions apply to all the following parameters, unless otherwise specified.

DC: V_{CC} = ±20V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	$+V_{CC}$ = 35V, $-V_{CC}$ = -5V, V_{CM} = -15V		-4.0	4.0	mV	1
				-6.0	6.0	mV	2, 3
		$+V_{CC}$ = 5V, $-V_{CC}$ = -35V, V_{CM} = 15V		-4.0	4.0	mV	1
				-6.0	6.0	mV	2, 3
		V_{CM} = 0V		-4.0	4.0	mV	1
				-6.0	6.0	mV	2, 3
		$+V_{CC}$ = 5V, $-V_{CC}$ = -5V, V_{CM} = 0V		-4.0	4.0	mV	1
				-6.0	6.0	mV	2, 3
I_{IO}	Input Offset Current	$+V_{CC}$ = 35V, $-V_{CC}$ = -5V, V_{CM} = -15V, R_S = 100KΩ	See(1)	-40	40	nA	1
			See(1)	-80	80	nA	2, 3
		$+V_{CC}$ = 5V, $-V_{CC}$ = -35V, V_{CM} = 15V, R_S = 100KΩ	See(1)	-40	40	nA	1
			See(1)	-80	80	nA	2, 3
		V_{CM} = 0V, R_S = 100KΩ	See(1)	-40	40	nA	1
			See(1)	-80	80	nA	2, 3
		$+V_{CC}$ = 5V, $-V_{CC}$ = -5V, V_{CM} = 0V, R_S = 100KΩ	See(1)	-40	40	nA	1
			See(1)	-80	80	nA	2, 3
$\pm I_{IB}$	Input Bias Current	$+V_{CC}$ = 35V, $-V_{CC}$ = -5V, V_{CM} = -15V, R_S = 100KΩ	See(1)	1.0	250	nA	1, 2
			See(1)	1.0	400	nA	3
		$+V_{CC}$ = 5V, $-V_{CC}$ = -35V, V_{CM} = 15V, R_S = 100KΩ	See(1)	1.0	250	nA	1, 2
			See(1)	1.0	400	nA	3
		V_{CM} = 0V, R_S = 100KΩ	See(1)	1.0	250	nA	1, 2
			See(1)	1.0	400	nA	3
		$+V_{CC}$ = 5V, $-V_{CC}$ = -5V, V_{CM} = 0V, R_S = 100KΩ	See(1)	1.0	250	nA	1, 2
			See(1)	1.0	400	nA	3

(1) Slash Sheet: R_S = 20KΩ, tested with R_S = 100KΩ for better resolution.

LM118JAN Electrical Characteristics DC Parameters (continued)

The following conditions apply to all the following parameters, unless otherwise specified.

DC: V_{CC} = ±20V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
+PSRR	Power Supply Rejection Ratio	+V_{CC} = 10V, -V_{CC} = -20V		-100	100	µV/V	1
				-150	150	µV/V	2, 3
-PSRR	Power Supply Rejection Ratio	+V_{CC} = 20V, -V_{CC} = -10V		-100	100	µV/V	1
				-150	150	µV/V	2, 3
CMRR	Common Mode Rejection Ratio	V_{CM} = ±15V, V_{CC} = ± 35V to ±5V		80		dB	1, 2, 3
+V_{IO} adj.	Offset Null			7.0		mV	1, 2, 3
-V_{IO} adj.	Offset Null				-7.0	mV	1, 2, 3
Delta V_{IO} / Delta T	Temperature Coefficient of Input Offset Voltage	25°C ≤ T_A ≤ 125°C	See(2)	-50	50	µV/°C	2
		-55°C ≤ T_A ≤ 25°C	See(2)	-50	50	µV/°C	3
Delta I_{IO} / Delta T	Temperature Coefficient of Input Offset Current	25°C ≤ T_A ≤ 125°C	See(2)	-1000	1000	pA/°C	2
		-55°C ≤ T_A ≤ 25°C	See(2)	-1000	1000	pA/°C	3
+I_{OS}	Short Circuit Current	+V_{CC} = 15V, -V_{CC} = -15V, t ≤ 25mS, V_{CM} = -15V		-65		mA	1, 2, 3
-I_{OS}	Short Circuit Current	+V_{CC} = 15V, -V_{CC} = -15V, t ≤ 25mS, V_{CM} = 15V			65	mA	1, 2
					80	mA	3
I_{CC}	Power Supply Current	+V_{CC} = 15V, -V_{CC} = -15V			8.0	mA	1
					7.0	mA	2
					9.0	mA	3
+V_{Opp}	Output Voltage Swing	R_L = 10KΩ, V_{CM} = -20V		17		V	4, 5, 6
		R_L = 2KΩ, V_{CM} = -20V		16		V	4, 5, 6
-V_{Opp}	Output Voltage Swing	R_L = 10KΩ, V_{CM} = 20V			-17	V	4, 5, 6
		R_L = 2KΩ, V_{CM} = 20V			-16	V	4, 5, 6
+A_{VS}	Open Loop Voltage Gain	V_O = 15V, R_L = 2KΩ	See(3)	50		V/mV	4
			See(3)	32		V/mV	5, 6
		V_O = 15V, R_L = 10KΩ	See(3)	50		V/mV	4
			See(3)	32		V/mV	5, 6
-A_{VS}	Open Loop Voltage Gain	V_O = -15V, R_L = 2KΩ	See(3)	50		V/mV	4
			See(3)	32		V/mV	5, 6
		V_O = -15V, R_L = 10KΩ	See(3)	50		V/mV	4
			See(3)	32		V/mV	5, 6
A_{VS}	Open Loop Voltage Gain	±V_{CC} = ±5V, V_O = ±2V, R_L = 2KΩ	See(3)	10		V/mV	4, 5, 6
		±V_{CC} = ±5V, V_O = ±2V, R_L = 10KΩ	See(3)	10		V/mV	4, 5, 6

(2) Calculated parameter.
(3) Datalog in K = V/mV

LM118JAN Electrical Characteristics AC Parameters

The following conditions apply to all the following parameters, unless otherwise specified.

AC: V_{CC} = ±20V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
NI_{BB}	Noise Input Broadband	BW = 10Hz to 5KHz, R_S = 0Ω			25	μV_{RMS}	7
NI_{PC}	Noise Input Popcorn	BW = 10Hz to 5KHz, R_S = 20KΩ			80	μV_{PK}	7
TR_{tR}	Transient Response: Rise Time	V_I = 50mV, PRR = 1KHz			40	nS	7, 8A, 8B
TR_{OS}	Transient Response: Overshoot	V_I = 50mV, PRR = 1KHz			50	%	7, 8A, 8B
+SR	Slew Rate	A_V = 1, V_I = -5V to +5V		50		V/µS	7, 8B
				40		V/µS	8A
-SR	Slew Rate	A_V = 1, V_I = +5V to -5V		50		V/µS	7, 8B
				40		V/µS	8A
$+t_S$	Settling Time	V_I = -5V to +5V	See(1)		800	nS	12
			See(1)		1200	nS	13, 14
$-t_S$	Settling Time	V_I = +5V to -5V	See(1)		800	nS	12
			See(1)		1200	nS	13, 14

(1) Errorband = ±2%.

LM118JAN Electrical Characteristics DC Drift Parameters

The following conditions apply to all the following parameters, unless otherwise specified.

DC: V_{CC} = ±20V

Delta calculations performed on JAN S devices at group B, subgroup 5 only.

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	V_{CM} = 0V		-1.0	1.0	mV	1
$±I_{IB}$	Input Bias Current	V_{CM} = 0V, R_S = 100KΩ		-25	25	nA	1

Typical Performance Characteristics

Input Current

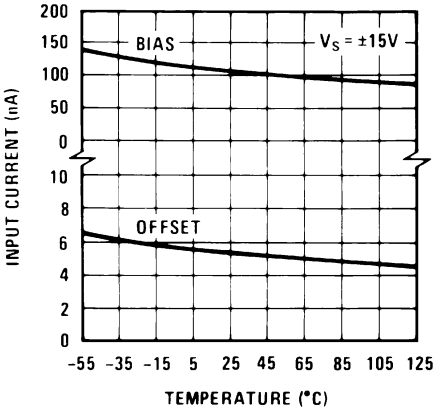


Figure 5.

Voltage Gain

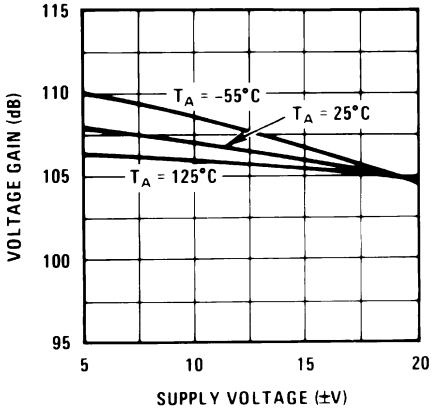


Figure 6.

Power Supply Rejection

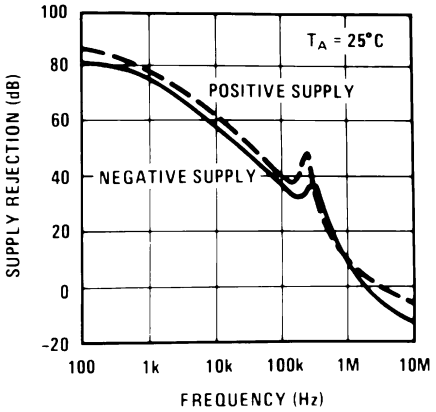


Figure 7.

Input Noise Voltage

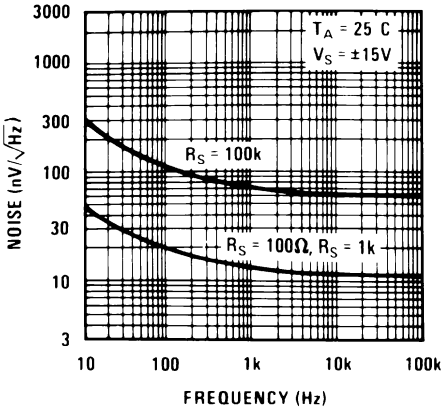


Figure 8.

Common Mode Rejection

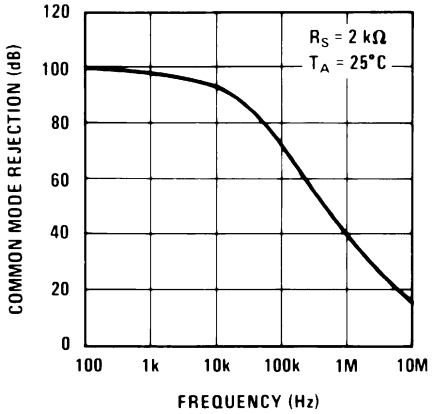


Figure 9.

Supply Current

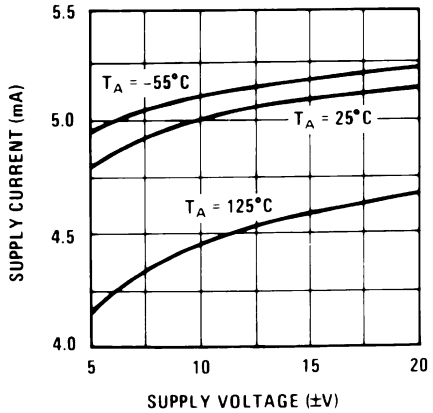


Figure 10.

Typical Performance Characteristics (continued)

Closed Loop Output Impedance

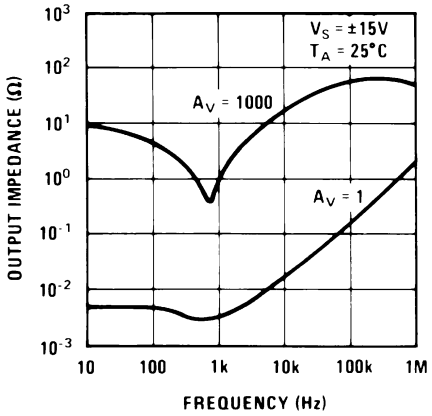


Figure 11.

Current Limiting

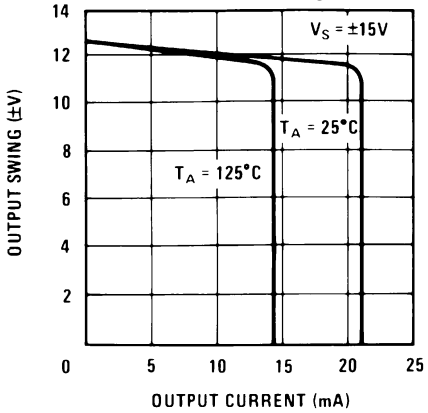


Figure 12.

Input Current

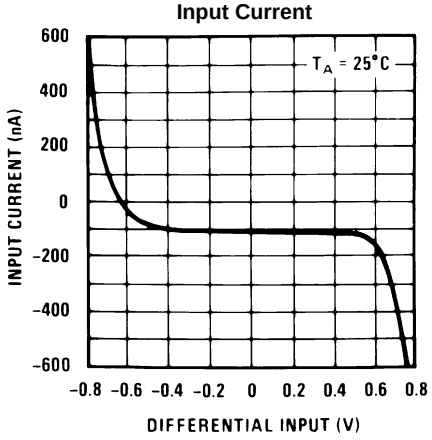


Figure 13.

Unity Gain Bandwidth

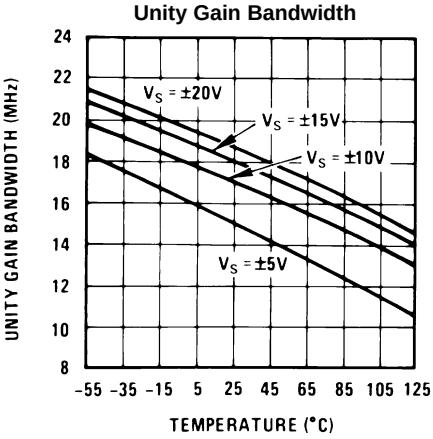


Figure 14.

Voltage Follower Slew Rate

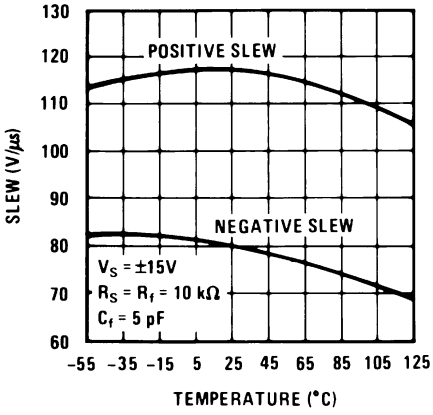


Figure 15.

Inverter Settling Time

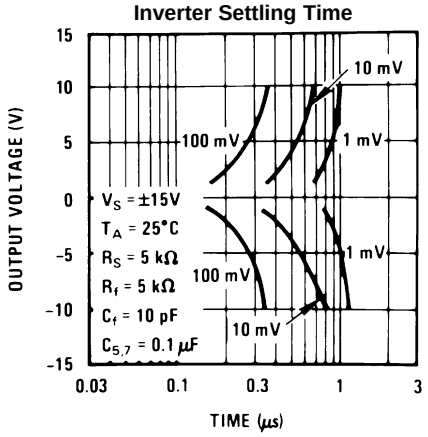


Figure 16.

Typical Performance Characteristics (continued)

Large Signal Frequency Response

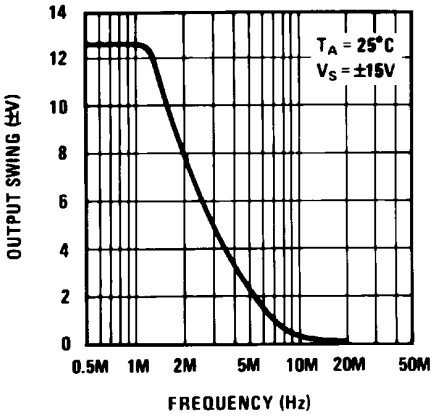


Figure 17.

Open Loop Frequency Response

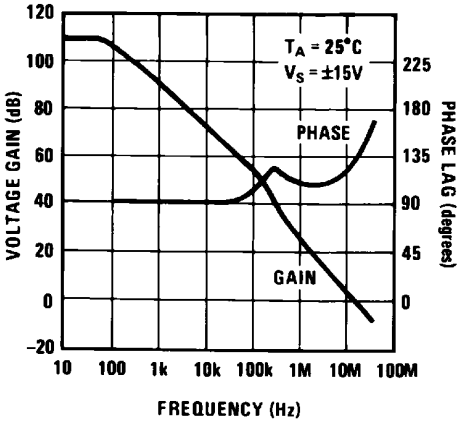


Figure 18.

Voltage Follower Pulse Response

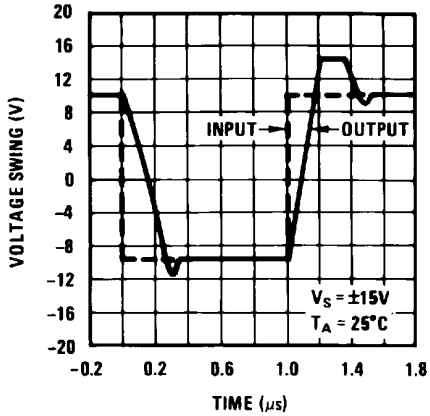


Figure 19.

Large Signal Frequency Response

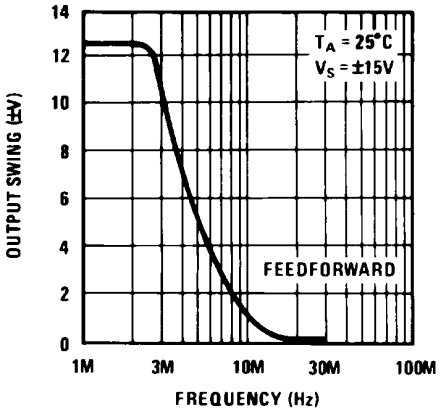


Figure 20.

Open Loop Frequency Response

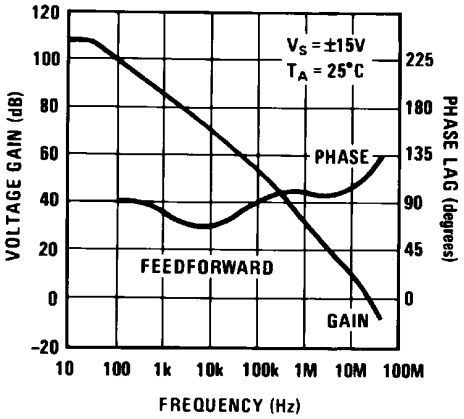


Figure 21.

Inverter Pulse Response

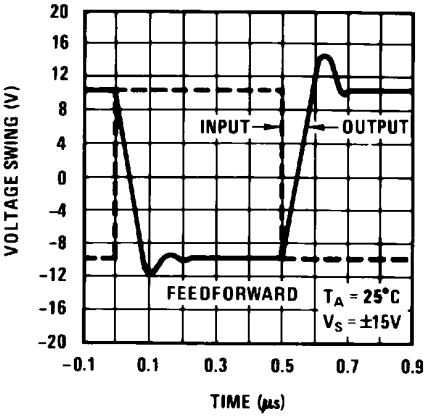
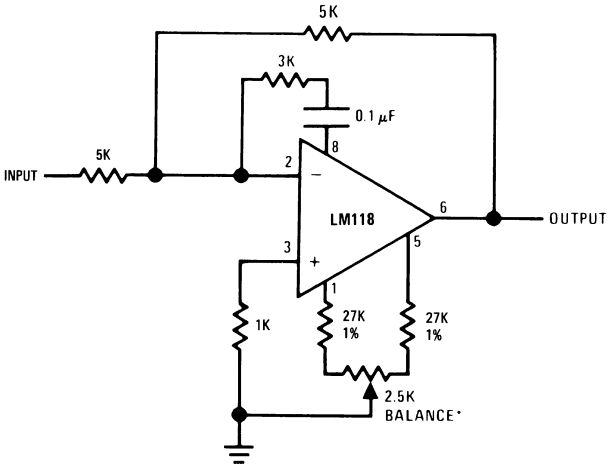


Figure 22.

AUXILIARY CIRCUITS

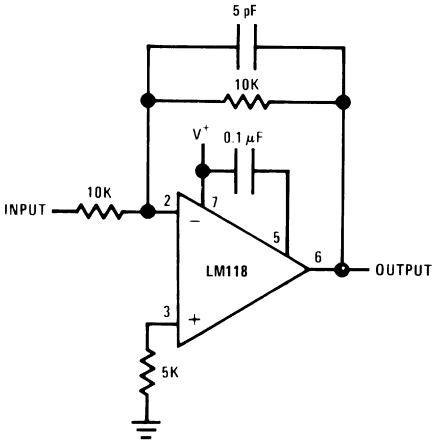
Figure 23. Feedforward Compensation for Greater Inverting Slew Rate



*Balance circuit necessary for increased slew.

Slew rate typically 150V/µs.

Figure 24. Compensation for Minimum Settling Time



Slew and settling time to 0.1% for a 10V step change is 800 ns.

Figure 25. Offset Balancing

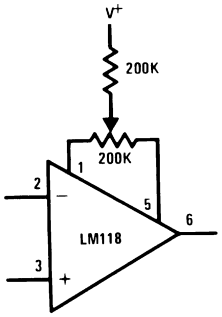


Figure 26. Isolating Large Capacitive Loads

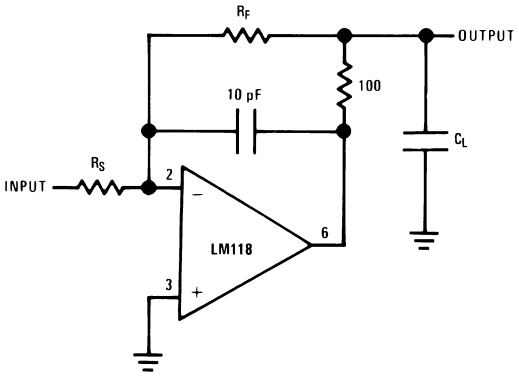
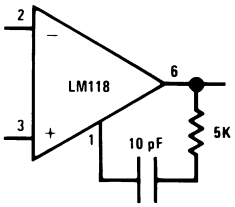


Figure 27. Overcompensation



Typical Applications

Figure 28. Fast Voltage Follower

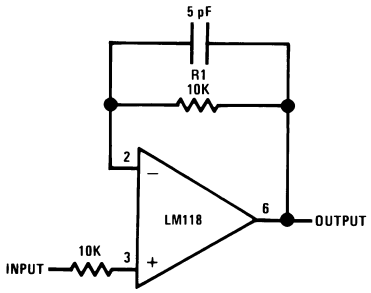
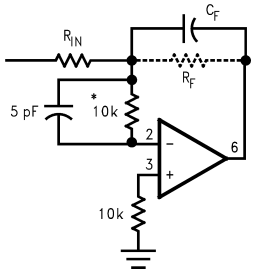


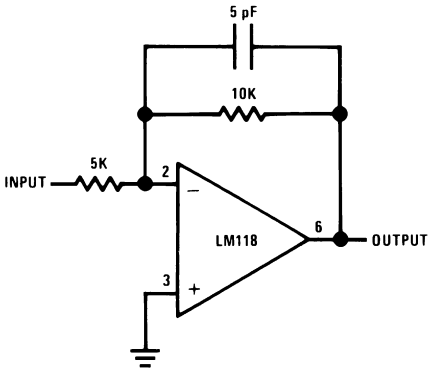
Figure 29. Integrator or Slow Inverter



C_F = Large
(C_F ≥ 50 pF)
*Do not hard-wire as integrator or slow inverter; insert a 10k-5 pF network in series with the input, to prevent oscillation.

(1) Do not hard-wire as voltage follower (R1 ≥ 5 kΩ)

Fast Summing Amplifier



Differential Amplifier

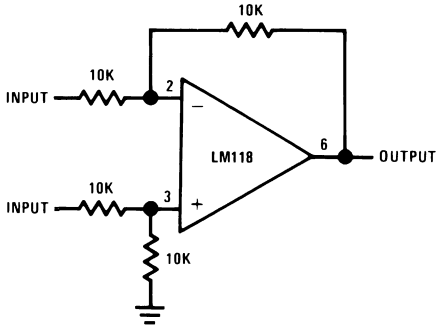


Figure 30. Fast Sample and Hold

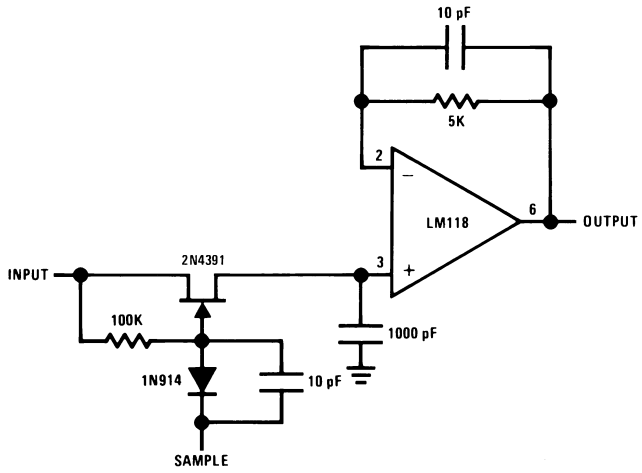
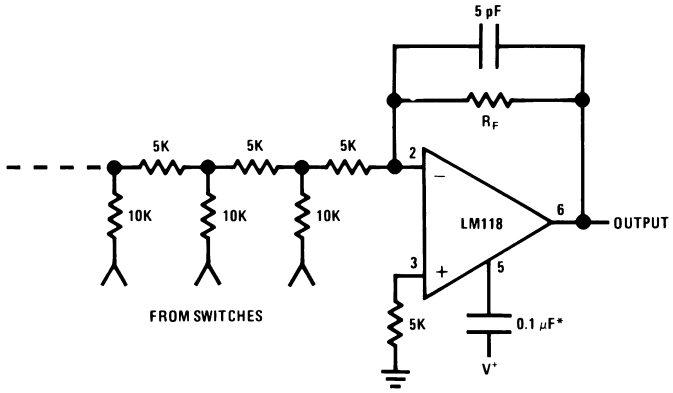
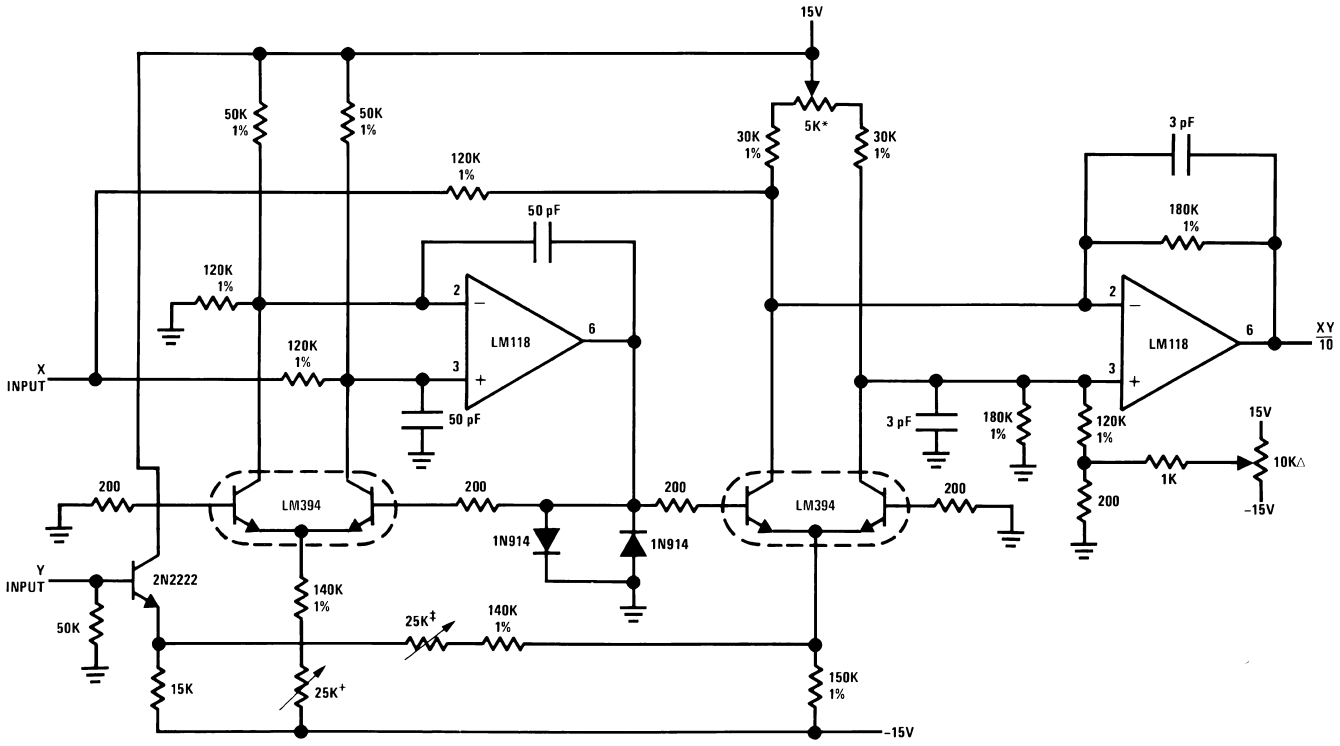


Figure 31. D/A Converter Using Ladder Network



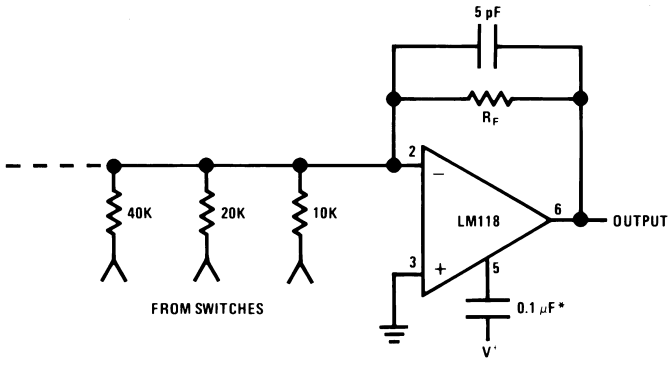
*Optional—Reduces settling time.

Figure 32. Four Quadrant Multiplier



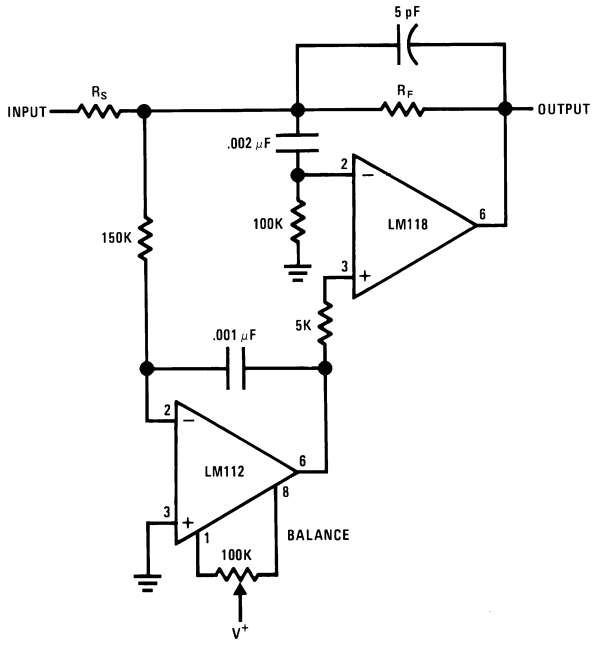
ΔOutput zero.
*"Y" zero
+"X" zero
‡Full scale adjust.

Figure 33. D/A Converter Using Binary Weighted Network

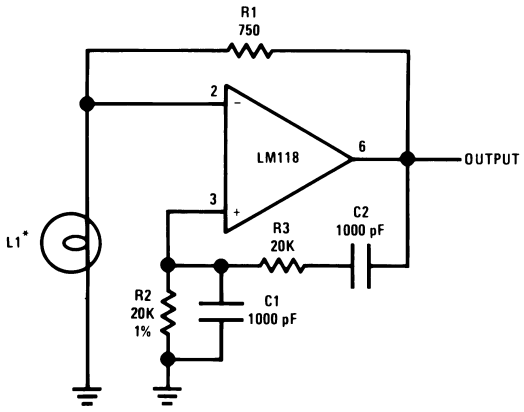


*Optional—Reduces settling time.

Figure 34. Fast Summing Amplifier with Low Input Current



Wein Bridge Sine Wave Oscillator



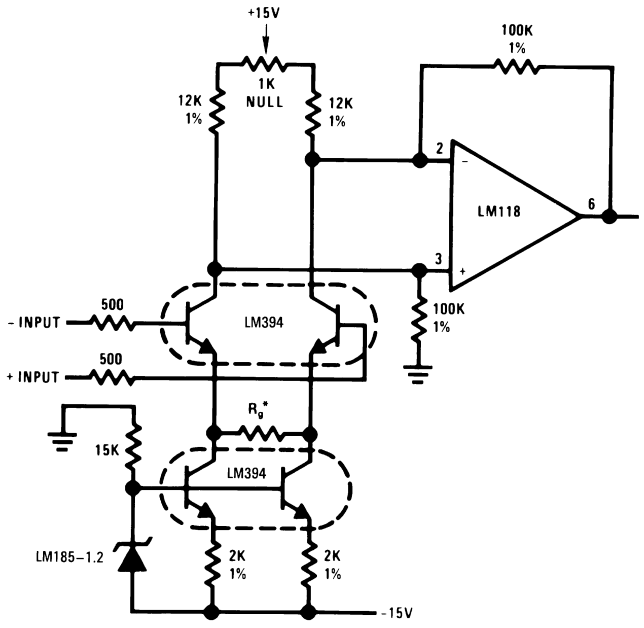
*L1—10V—14 mA bulb ELDEMA 1869

R1 = R2

C1 = C2

$$f = \frac{1}{2\pi R2\, C1}$$

Instrumentation Amplifier



*Gain $\geq \frac{200K}{R_g}$ for $1.5K \leq R_g \leq 200K$

REVISION HISTORY SECTION

Date Released	Revision	Section	Originator	Changes
07/12/05	A	New Release, Corporate format	L. Lytle	1 MDS data sheet, MJLM118–X Rev 0A0 was converted into the Corp. datasheet format. MDS datasheet will be archived.
03/20/2013	A	All Sections		Changed layout of National Data Sheet to TI format

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
JL118BPA	ACTIVE	CDIP	NAB	8	40	TBD	Call TI	Call TI	-55 to 125	JL118BPA Q JM38510/ 10107BPA ACO 10107BPA >T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

OTHER QUALIFIED VERSIONS OF LM118JAN, LM118JAN-SP :

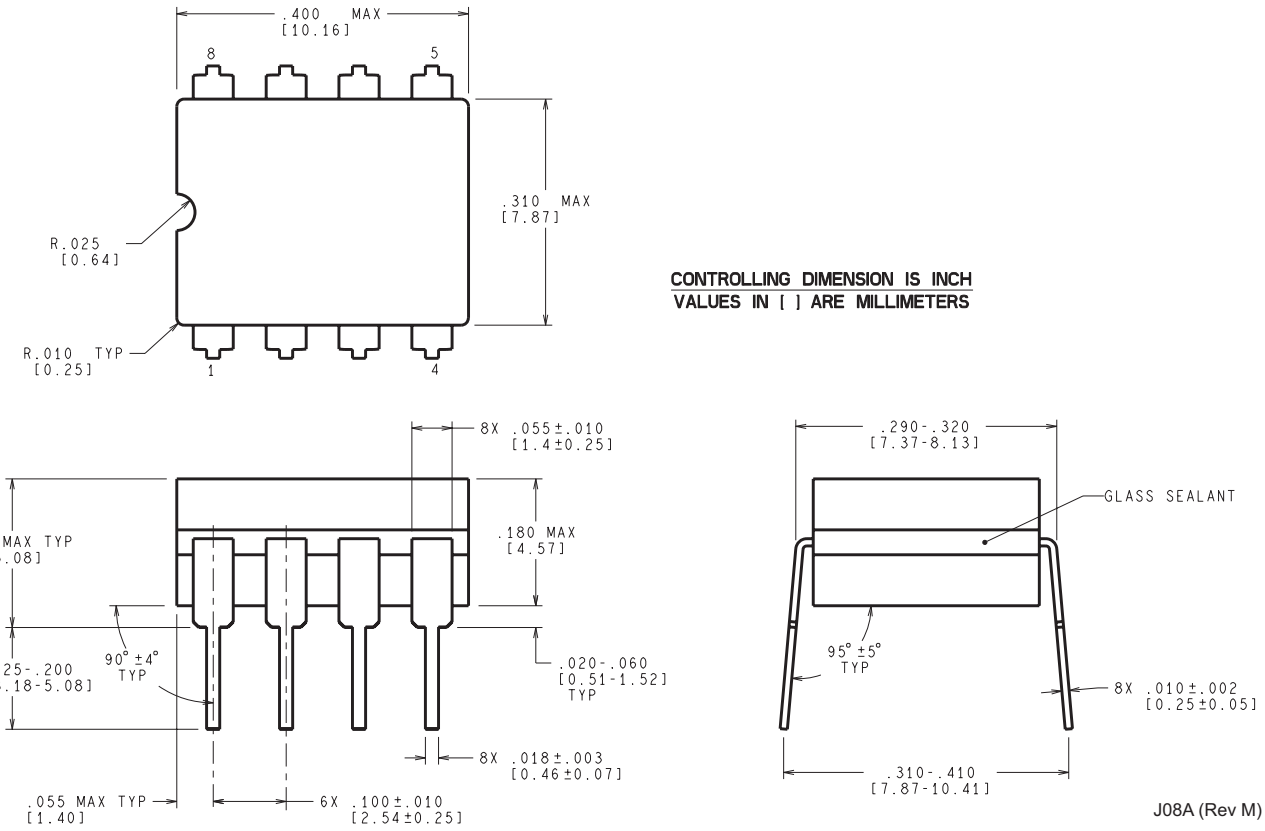
- Military: LM118JAN

- Space: LM118JAN-SP

NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

NAB0008A


.400 MAX
[10.16]
8
5
.310 MAX
[7.87]
R.025
[0.64]
R.010 TYP
[0.25]
1
4
CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
8X .055±.010
[1.4±0.25]
.200 MAX TYP
[5.08]
.180 MAX
[4.57]
8X .125-.200
[3.18-5.08]
90° ±4°
TYP
.020-.060
[0.51-1.52]
TYP
8X .018±.003
[0.46±0.07]
.055 MAX TYP
[1.40]
6X .100±.010
[2.54±0.25]
.290-.320
[7.37-8.13]
GLASS SEALANT
95° ±5°
TYP
8X .010±.002
[0.25±0.05]
.310-.410
[7.87-10.41]
J08A (Rev M)

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265