

LM119JAN High Speed Dual Comparator

Check for Samples: [LM119JAN](#)

FEATURES

- Two independent comparators
- Operates from a single 5V supply
- Typically 80 ns response time at $\pm 15V$
- Minimum fan-out of 2 each side
- Maximum input current of 1 μA over temperature
- Inputs and outputs can be isolated from system ground
- High common mode slew rate

DESCRIPTION

The LM119 is a precision high speed dual comparator fabricated on a single monolithic chip. It is designed to operate over a wide range of supply voltages down to a single 5V logic supply and ground. Further, it has higher gain and lower input currents than devices such as the LM710. The uncommitted collector of the output stage makes the LM119 compatible with RTL, DTL and TTL as well as capable of driving lamps and relays at currents up to 25 mA.

Although designed primarily for applications requiring operation from digital logic supplies, the LM119 is fully specified for power supplies up to $\pm 15V$. It features faster response than the LM111 at the expense of higher power dissipation. However, the high speed, wide operating voltage range and low package count make the LM119 much more versatile than older devices such as the LM711.

Connection Diagram

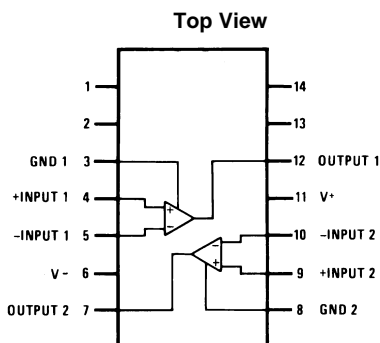
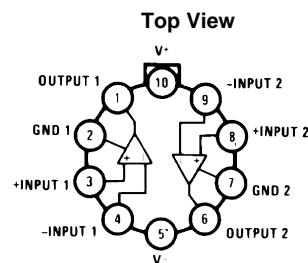


Figure 1. CDIP Package
See Package Number J0014A



Case is connected to pin 5 (V-).

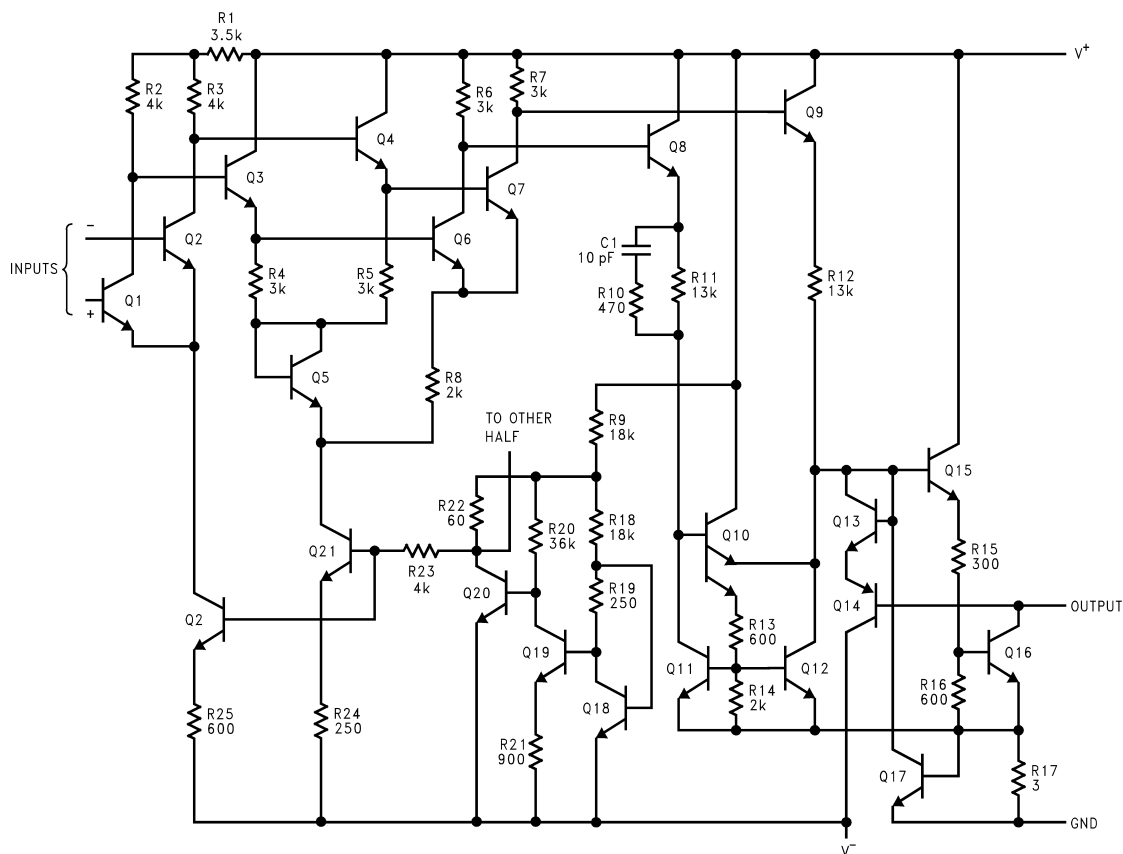
Figure 2. TO-100 Package
See Package Number LME0010C



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Schematic Diagram



Do not operate the LM119 with more than 16V between GND and V



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings ⁽¹⁾

Total Supply Voltage	36V
Output to Negative Supply Voltage	36V
Ground to Negative Supply Voltage	25V
Ground to Positive Supply Voltage	18V
Differential Input Voltage	±5V
Input Voltage ⁽²⁾	±15V
Power Dissipation ⁽³⁾	500 mW
Output Short Circuit Duration	10 sec
Storage Temperature Range	-65°C ≤ T _A ≤ 150°C
Operating Ambient Temperature Range	-55°C ≤ T _A ≤ 125°C
Maximum Junction Temperature (T _J)	150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Thermal Resistance θ_{JA}	
LME0010C Package (Still Air)	162°C/W
LME0010C Package (500LF/Min Air flow)	88°C/W
J0014A Package (Still Air)	94°C/W
J0014A Package (500LF/Min Air flow)	52°C/W
Thermal Resistance θ_{JC}	
LME0010C Package	31°C/W
J0014A Package	11°C/W
Package Weight	
LME0010C Package, J0014A Package	TBD
ESD rating ⁽⁴⁾	800V

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- (2) For supply voltages less than ±15V the absolute maximum input voltage is equal to the supply voltage.
- (3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is P_{Dmax} = (T_{Jmax} - T_A)/ θ_{JA} or the number given in the Absolute Maximum Ratings, whichever is lower.
- (4) Human Body model, 1.5K Ω in series with 100pF.

Table 1. Quality Conformance Inspection ⁽¹⁾

Subgroup	Description	Temp °C
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55
12	Settling time at	25
13	Settling time at	125
14	Settling time at	-55

- (1) Mil-Std-883, Method 5005 - Group A

Electrical Characteristics DC Parameters

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	$+V_{CC} = 15V, -V_{CC} = -15V,$ $V_{CM} = 0V, R_S = 50\Omega$		-4.0	4.0	mV	1
				-7.0	7.0	mV	2, 3
		$+V_{CC} = 27V, -V_{CC} = -3V,$ $V_{CM} = -12V, R_S = 50\Omega$		-4.0	4.0	mV	1
				-7.0	7.0	mV	2, 3
		$+V_{CC} = 3V, -V_{CC} = -27V,$ $V_{CM} = 12V, R_S = 50\Omega$		-4.0	4.0	mV	1
		-7.0	7.0	mV	2, 3		
I_{IO}	Input Offset Current	$+V_{CC} = 15V, -V_{CC} = -15V,$ $V_{CM} = 0V$		-75	+75	nA	1, 2
				-100	+100	nA	3
		$+V_{CC} = 27V, -V_{CC} = -3V,$ $V_{CM} = -12V$		-75	+75	nA	1, 2
				-100	+100	nA	3
		$+V_{CC} = 3V, -V_{CC} = -27V,$ $V_{CM} = 12V$		-75	+75	nA	1, 2
		-100	+100	nA	3		
$+I_{CC}$	Power Supply Current	$+V_{CC} = 15V, -V_{CC} = -15V$			10	mA	1, 2
					11.5	mA	3
$-I_{CC}$	Power Supply Current	$+V_{CC} = 15V, -V_{CC} = -15V$		-5.0		mA	1
				-4.5		mA	2
				-6.0		mA	3
$\pm I_{IB}$	Input Bias Current	$+V_{CC} = 15V, -V_{CC} = -15V,$ $V_{CM} = 0V$		-0.1	500	nA	1, 2
				-0.1	1000	nA	3
		$+V_{CC} = 27V, -V_{CC} = -3V,$ $V_{CM} = -12V$		-0.1	750	nA	1, 2
				-0.1	1000	nA	3
		$+V_{CC} = 3V, -V_{CC} = -27V,$ $V_{CM} = 12V$		-0.1	750	nA	1, 2
		-0.1	1000	nA	3		
CMRR	Common Mode Rejection	$-12V \leq V_{CM} \leq +12V,$ $-27V \leq -V_{CC} \leq -3V,$ $3V \leq +V_{CC} \leq 27V, R_S = 50\Omega$		90		dB	1, 2, 3
V_{OL}	Low Level Output Voltage	$+V_{CC} = 3.5V, -V_{CC} = -1V,$ $V_{CM} = 1V, V_{IO} = 7mV,$ $I_O = 3.2mA$			0.4	V	1, 2
					0.6	V	3
		$+V_{CC} = 2.25V, -V_{CC} = -2.25V,$ $V_{CM} = 2.25V, V_{IO} = 7mV,$ $I_O = 3.2mA$			0.4	V	1, 2
					0.6	V	3
		$+V_{CC} = 27V, -V_{CC} = -3V,$ $V_{CM} = -12V, V_{IO} = 7mV,$ $I_O = 25mA$			1.5	V	1, 2, 3
$+V_{CC} = 3V, -V_{CC} = -27V,$ $V_{CM} = 12V, V_{IO} = 7mV,$ $I_O = 25mA$			1.5	V	1, 2, 3		
I_{CEX}	Output Leakage Current	$+V_{CC} = 18V, -V_{CC} = -18V,$ $V_O = 18V$		-1.0	2.0	μA	1
				-1.0	10	μA	2
A_V	Voltage Gain (Collector)	$+V_{CC} = 15V, -V_{CC} = -15V,$ $V_O = 1.5V \text{ to } 11.5V$	(1)	10		K	4
			(1)	5.0		K	5, 6

(1) K = V/mV.

Electrical Characteristics AC Parameters

The following conditions apply to all the following parameters, unless otherwise specified.

AC: $\pm 15V$, $C_L = 50pF$

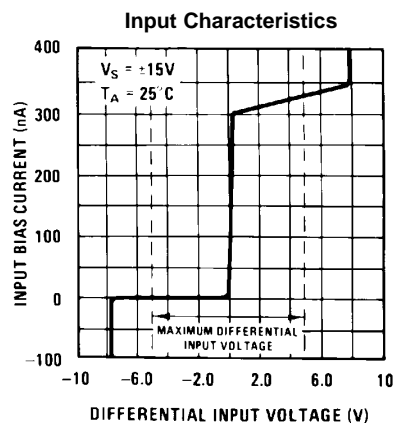
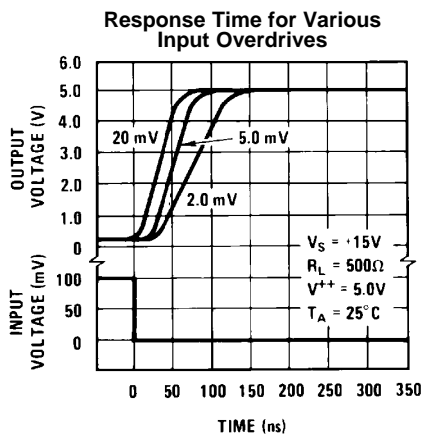
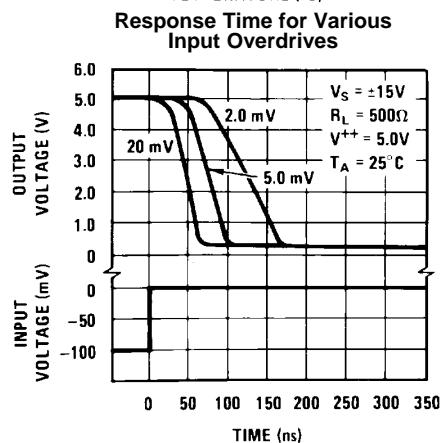
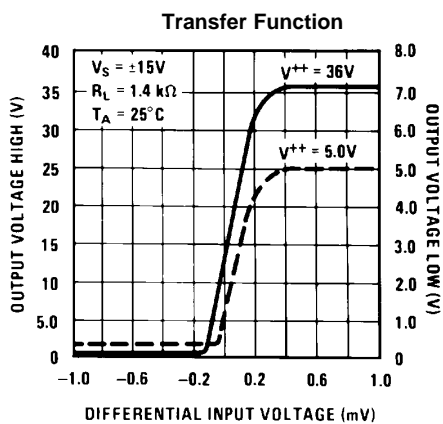
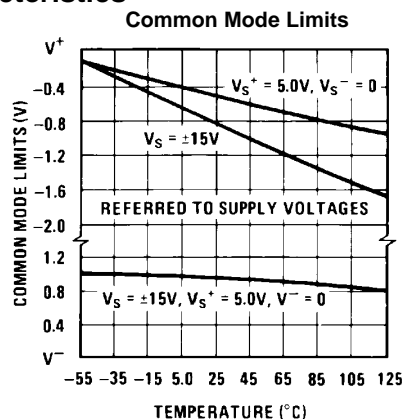
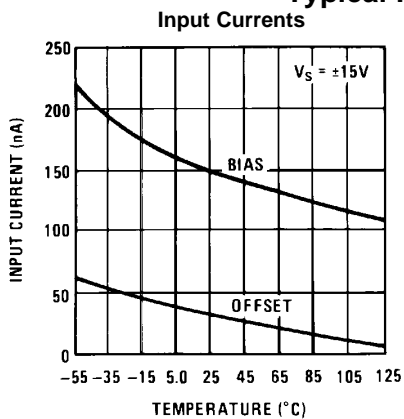
Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
$t_{R_{LHC}}$	Response Time (Collector Output)	V_{OD} (overdrive) = +5mV, $V_I = 100mV$			125	nS	9
$t_{R_{HLC}}$	Response Time (Collector Output)	V_{OD} (overdrive) = -5mV, $V_I = 100mV$			160	nS	9

Electrical Characteristics DC Drift Parameters

Delta calculations performed at Group B-5

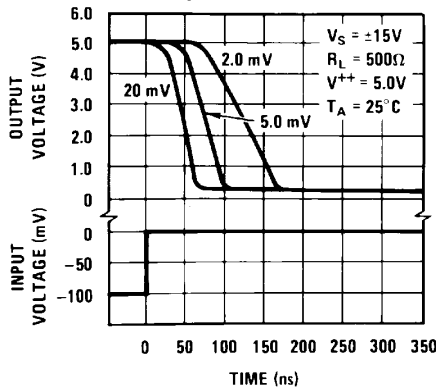
Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	$+V_{CC} = 15V$, $-V_{CC} = -15V$, $V_{CM} = 0V$, $R_S = 50\Omega$		-1.0	1.0	mV	1
		$+V_{CC} = 27V$, $-V_{CC} = -3V$, $V_{CM} = -12V$, $R_S = 50\Omega$		-1.0	1.0	mV	1
		$+V_{CC} = 3V$, $-V_{CC} = -27V$, $V_{CM} = 12V$, $R_S = 50\Omega$		-1.0	1.0	mV	1
$\pm I_{IB}$	Input Bias Current	$+V_{CC} = 15V$, $-V_{CC} = -15V$, $V_{CM} = 0V$		-50	50	nA	1
		$+V_{CC} = 27V$, $-V_{CC} = -3V$, $V_{CM} = -12V$		-50	50	nA	1
		$+V_{CC} = 3V$, $-V_{CC} = -27V$, $V_{CM} = 12V$		-50	50	nA	1

Typical Performance Characteristics

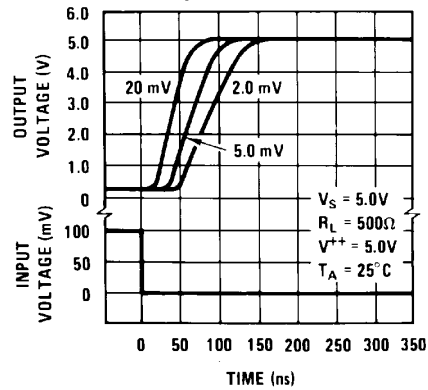


Typical Performance Characteristics (continued)

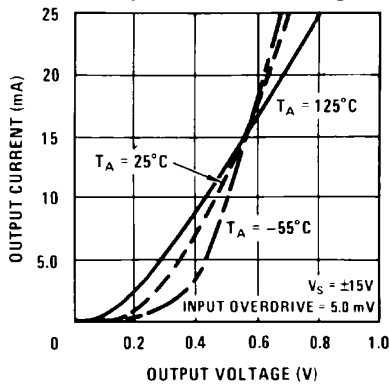
Response Time for Various Input Overdrives



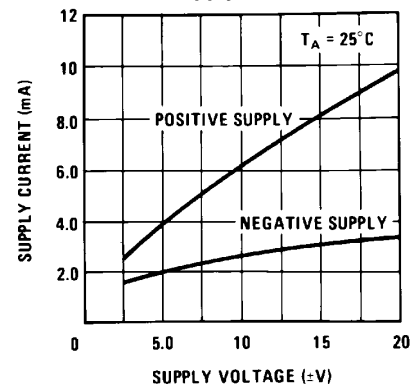
Response Time for Various Input Overdrives



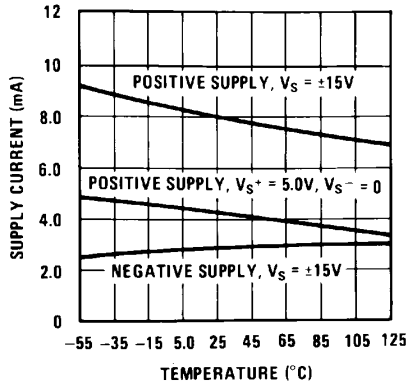
Output Saturation Voltage



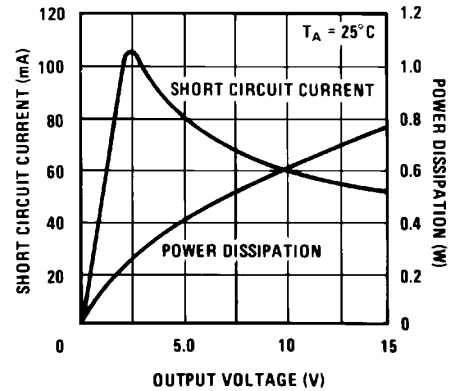
Supply Current



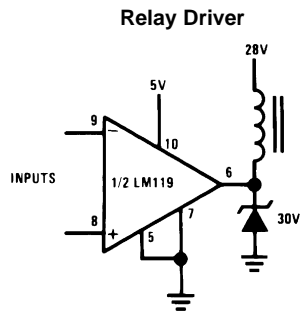
Supply Current



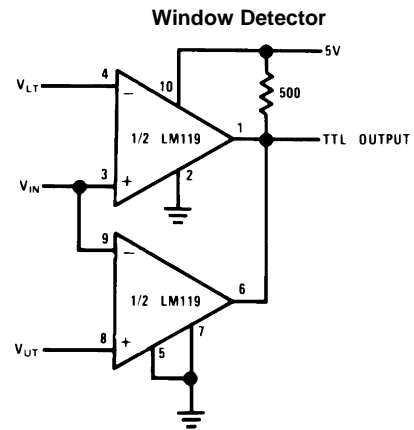
Output Limiting Characteristics



TYPICAL APPLICATIONS



Pin numbers are for TO-100 package.



$$V_{OUT} = 5V \text{ for } V_{LT} \leq V_{IN} \leq V_{UT}$$

$$V_{OUT} = 0 \text{ for } V_{IN} \leq V_{LT} \text{ or } V_{IN} \geq V_{UT}$$

REVISION HISTORY

Date Released	Revision	Section	Changes
7/0105	A	New release to corporate format	1 MDS datasheet converted into one corporate data sheet format MJLM119-X Rev. OBL will be archived.
09/24/2010	B	Obsolete Data Sheet	Revision B, End of Life on Product/NSID Dec. 2009 Obsolete Data Sheet

Changes from Revision A (April 2013) to Revision B
Page

- Changed layout of National Data Sheet to TI format **8**

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