

LMP8275 High Common Mode, Gain of 20, Precision Voltage Difference Amplifier

Check for Samples: [LMP8275](#)

FEATURES

- Typical Values, $T_A = 25^\circ\text{C}$
- Input Offset Voltage: $\pm 2\text{ mV Max}$
- TCVoS: $\pm 30\ \mu\text{V}/^\circ\text{C Max}$
- CMRR: 80 dB Min
- Output Voltage Swing: Rail-to-Rail
- Bandwidth: 80 kHz
- Operating Temperature Range (Ambient): $-40^\circ\text{C to } 125^\circ\text{C}$
- Supply Voltage: 4.75V to 5.5V
- Supply Current: 1 mA

APPLICATIONS

- Fuel Injection Control
- High and Low Side Driver Configuration Current Sensing
- Power Management Systems

TYPICAL APPLICATION

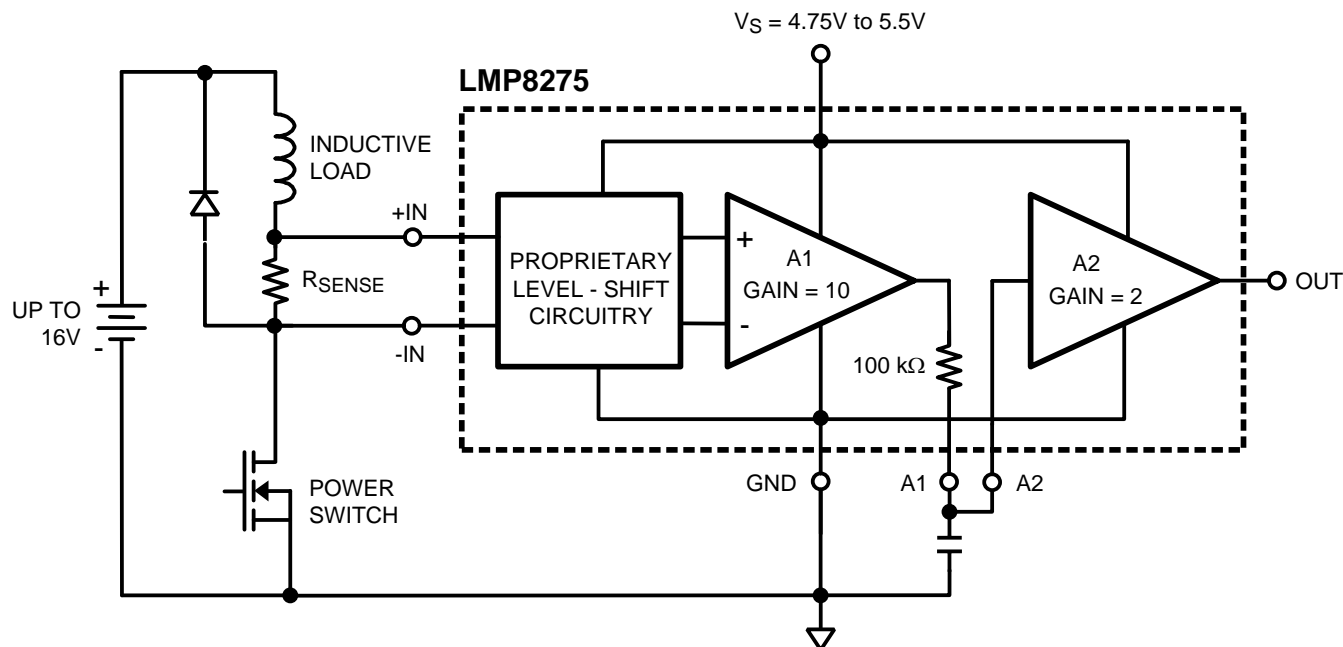


Figure 1. Low Side Current Sensing



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾⁽²⁾

ESD Tolerance ⁽³⁾	Human Body Model	For +IN and -IN	±4000V
		For all other pins	±2000V
	Machine Model		200V
Supply Voltage (V_S - GND)			5.75V
Common Mode Voltage on +IN and -IN	Transient (400 ms)		-7V to 45V
Storage Temperature Range			-65°C to +150°C
Junction Temperature ⁽⁴⁾			+150°C
Soldering Information	Infrared or Convection (20 sec)		235°C
	Wave Soldering Lead Temp. (10 sec)		260°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the [Electrical Characteristics](#) Tables.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) Human Body Model is 1.5 k Ω in series with 100 pF. Machine Model is 0 Ω in series with 200 pF.
- (4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

OPERATING RATINGS ⁽¹⁾

Temperature Range			
Packaged Device ⁽²⁾			-40°C to +125°C
Supply Voltage (V_S -GND)			4.75V to 5.5V
Package Thermal Resistance (θ_{JA} ⁽²⁾)	8-Pin SOIC		190°C/W

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the [Electrical Characteristics](#) Tables.
- (2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

5V ELECTRICAL CHARACTERISTICS ⁽¹⁾

Unless otherwise specified, all are limits specified for $T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $\text{GND} = 0\text{V}$, $-2\text{V} \leq V_{\text{CM}} \leq 16\text{V}$, $R_L = \text{Open}$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min	Typ ⁽²⁾	Max	Units
V_{OS}	Input Offset Voltage	$V_{\text{CM}} = V_S/2$			± 0.25	± 2.0	mV
TCV_{OS}	Input Offset Voltage Drift	$V_{\text{CM}} = V_S/2$	$25^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		± 20	± 30	$\mu\text{V}/^\circ\text{C}$
			$-40^\circ\text{C} \leq T_A \leq 25^\circ\text{C}$		± 20	± 35	
$A_2 I_B$	Input Bias Current of A2	See ⁽³⁾			-20		fA
						± 20	nA
I_S	Supply Current				1.0	1.2 1.4	mA
R_{CM}	Input Impedance Common Mode			160	200	240	k Ω
R_{DM}	Input Impedance Differential Mode			320	400	480	k Ω
CMVR	Input Common-Mode Voltage Range			-2		+16	V
DC CMRR	DC Common Mode Rejection Ratio	$0^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	$-2\text{V} \leq V_{\text{CM}} \leq 16\text{V}$	80	103		dB
		$-40^\circ\text{C} \leq T_A \leq 0^\circ\text{C}$	$-2\text{V} \leq V_{\text{CM}} \leq 16\text{V}$	77			
AC CMRR	AC Common Mode Rejection Ratio ⁽⁴⁾	$-2\text{V} \leq V_{\text{CM}} \leq 16\text{V}$	$f = 1\text{ kHz}$	80	95		dB
		$-2\text{V} \leq V_{\text{CM}} \leq 16\text{V}$	$f = 10\text{ kHz}$		78		
PSRR	Power Supply Rejection Ratio	$4.75\text{V} \leq V_S \leq 5.5\text{V}$		70	80		dB
$R_{\text{F-INT}}$	Filter Resistor			97	100	103	k Ω
$\text{TCR}_{\text{F-INT}}$	Filter Resistor Drift				± 20		ppm/ $^\circ\text{C}$
A_V	Total Gain			19.8	20	20.2	V/V
	Gain Drift				± 2	± 25	ppm/ $^\circ\text{C}$
A_{V1}	A1 Gain			9.9	10	10.1	V/V
A_{V2}	A2 Gain			1.98	2.0	2.02	V/V
$A_1 V_{\text{OUT}}$	A1 Output Voltage Swing		VOL		0.004	0.01	V
			VOH	4.80	4.95		
$A_2 V_{\text{OUT}}$	A2 Output Voltage Swing ⁽⁵⁾⁽⁶⁾	$R_L = 100\text{ k}\Omega$ on Output	VOL		0.007	0.02	V
			VOH	4.80	4.99		
		$R_L = 10\text{ k}\Omega$ on Output	VOL		0.03		V
			VOH		4.95		
SR	Slew Rate ⁽⁷⁾				0.7		V/ μs
BW	Bandwidth				80		kHz
Noise	0.1 Hz to 10 Hz				5.7		μV_{PP}
	Spectral Density	$f = 1\text{ kHz}$			452		nV/ $\sqrt{\text{Hz}}$

- (1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.
- (2) Typical values represent the parametric norm at the time of characterization.
- (3) Positive current corresponds to current flowing into the device.
- (4) AC Common Mode Signal is a 16 V_{PP} sine-wave (0V to 16V) at the given frequency
- (5) For VOL, R_L is connected to V_S and for VOH, R_L is connected to GND.
- (6) For this test input is driven from A1 stage.
- (7) Slew rate is the average of the rising and falling slew rates.

CONNECTION DIAGRAM

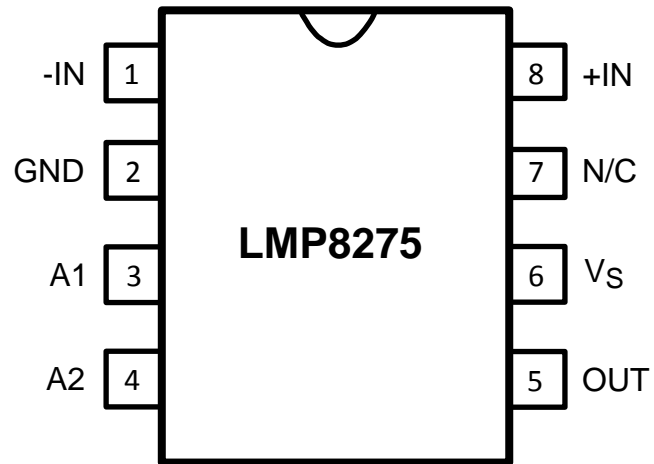


Figure 2. 8-Pin SOIC (Top View)
See D Package

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified: $T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $V_{CM} = V_S/2$

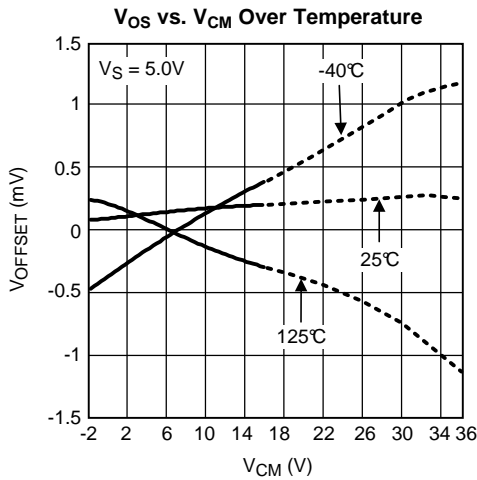


Figure 3.

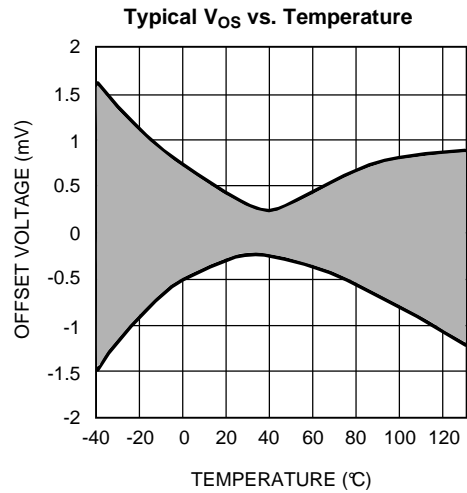


Figure 4.

Input Bias Current Over Temperature (A1 Inputs)

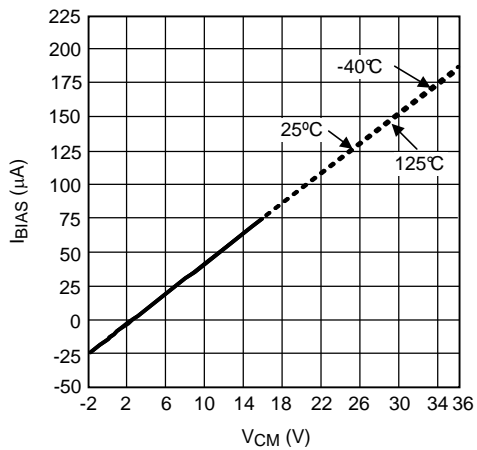


Figure 5.

Input Bias Current Over Temperature (A2 Input)

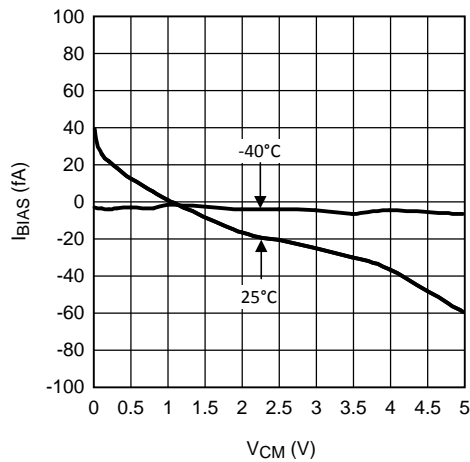


Figure 6.

Input Bias Current Over Temperature (A2 Input)

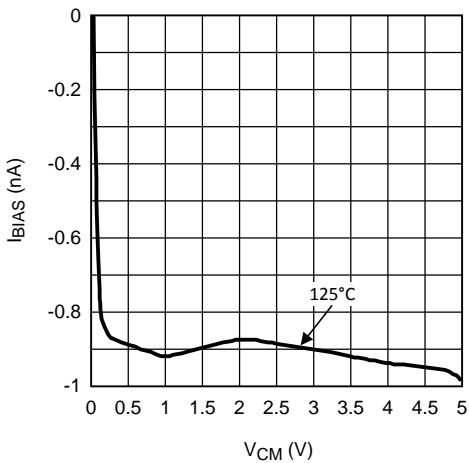


Figure 7.

Input Referred Voltage Noise vs. Frequency

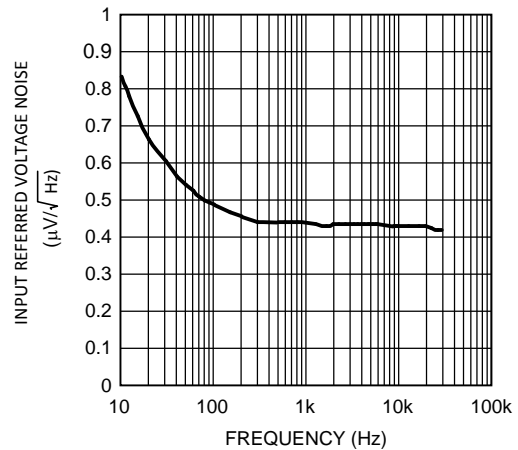


Figure 8.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: $T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $V_{CM} = V_S/2$

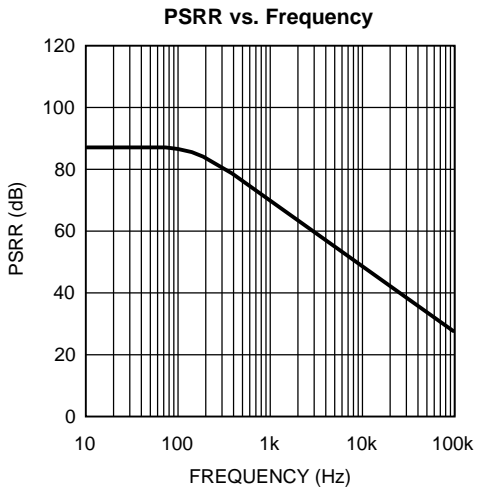


Figure 9.

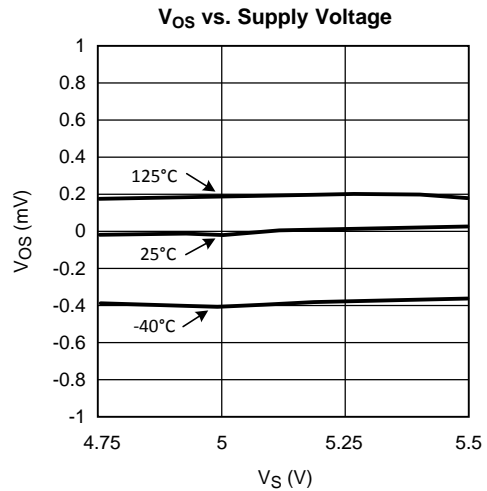


Figure 10.

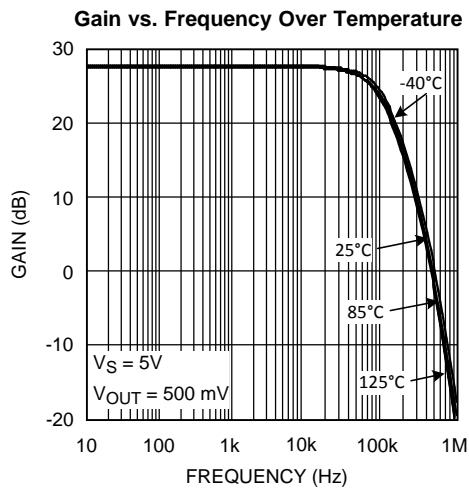


Figure 11.

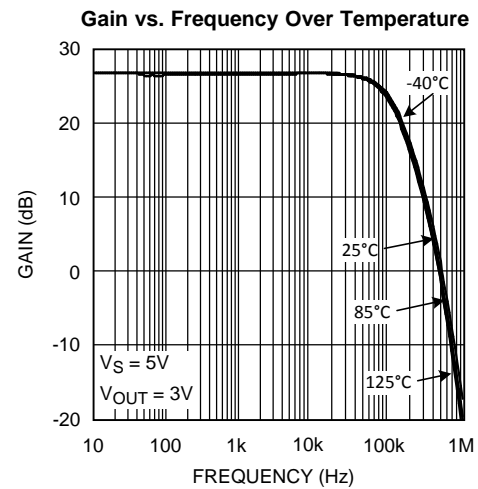


Figure 12.

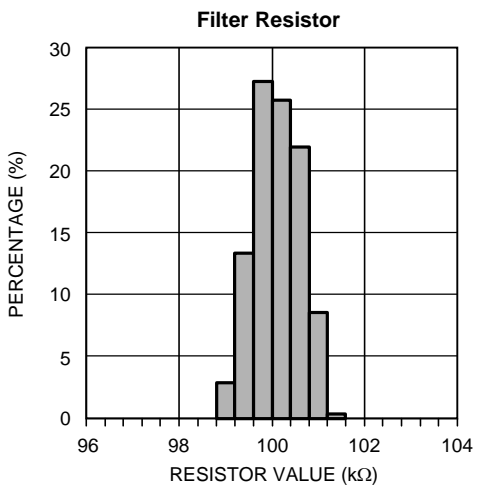


Figure 13.

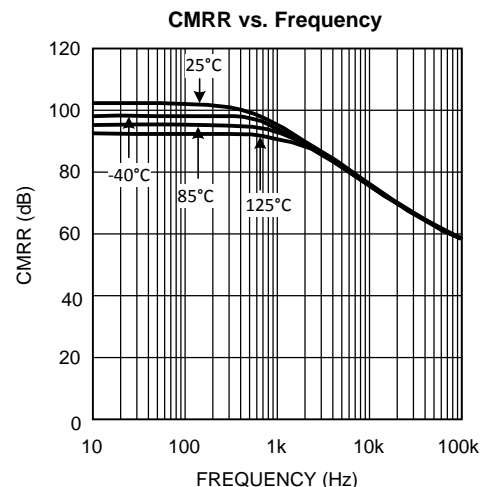


Figure 14.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: $T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $V_{CM} = V_S/2$

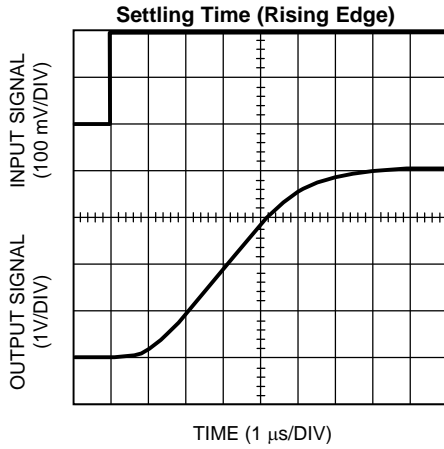


Figure 15.

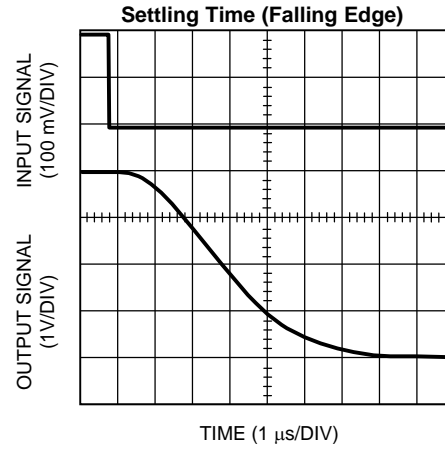


Figure 16.

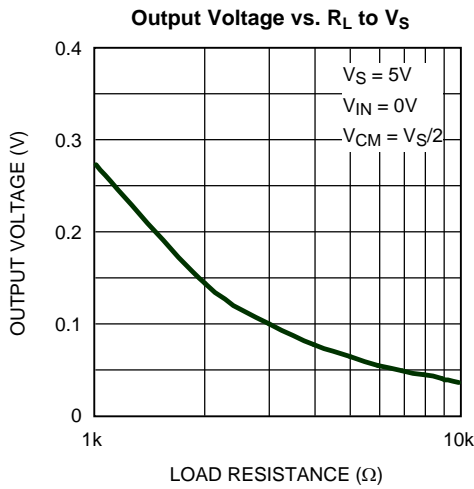


Figure 17.

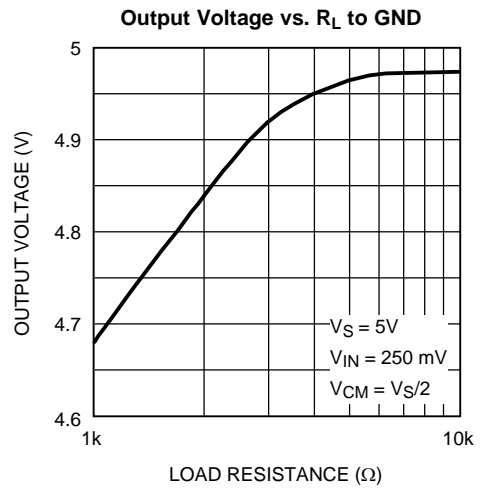


Figure 18.

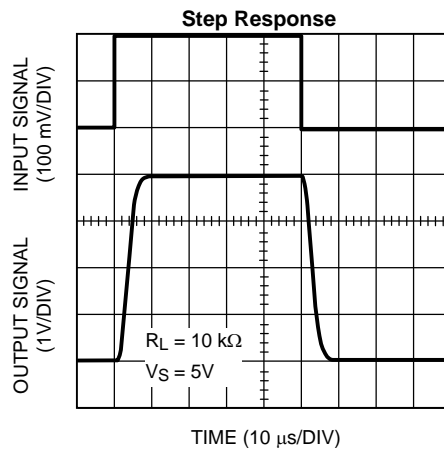


Figure 19.

APPLICATION NOTE

LMP8275

The LMP8275 is a single supply amplifiers with a fixed gain of 20 and a common mode voltage range of -2V to 16V. The fixed gain is achieved in two separate stages, a preamplifier with gain of +10 and a second stage amplifier with gain of +2. A block diagram of the LMP8275 is shown in Figure 20.

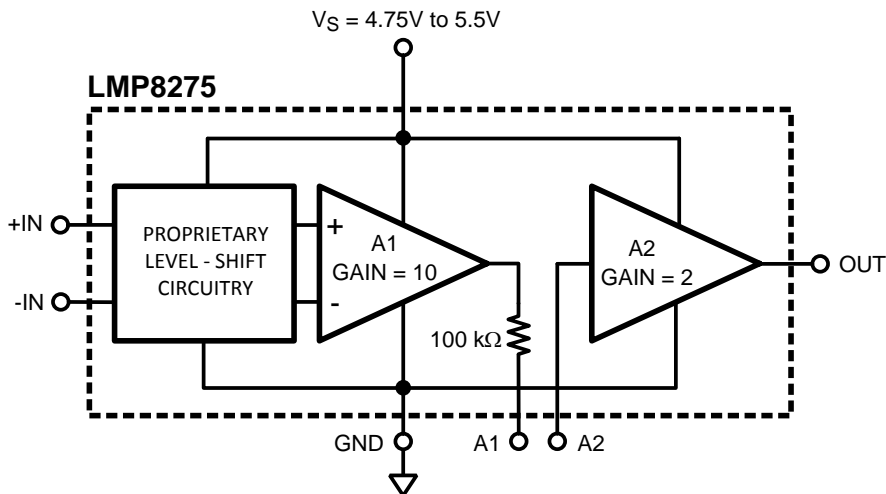


Figure 20. LMP8275

The overall offset of the LMP8275 is minimized by trimming amplifier A1. This is done in such a way that the output referred offset of A1 cancels the input referred offset of A2 or $10V_{OS1} = -V_{OS2}$.

Because of this offset voltage relationship, the offset of each individual amplifier stage may be more than the limit specified for the overall system in the datasheet tables. If the signal going from A1 to A2 is amplified or attenuated (by use of amplifiers and resistors), the overall LMP8275 offset will be affected as a result. Filtering the signal between A1 and A2 or simply connecting the two pins will not change the offset of the LMP8275.

Referencing input referred offset voltages, the following relationship holds:

$$\frac{(10V_{OS1}) + (V_{OS2})}{10} = V_{OS} (\text{LMP8275}) \quad (1)$$

If the signal on pin 3 is scaled, attenuated or amplified, by a factor **X**, then the offset of the overall system will become:

$$\frac{(10V_{OS1}) \times (X) + (V_{OS2})}{10 (X)} = V_{OS} (\text{LMP8275}) \quad (2)$$

POWER SUPPLY DECOUPLING

In order to decouple the LMP8275 from AC noise on the power supply, it is recommended to use a 0.1 μF on the supply pin. It is best to use a 0.1 μF capacitor in parallel with a 10 μF capacitor. This will generate an AC path to ground for most frequency ranges and will greatly reduce the noise introduced by the power supply.

SECOND ORDER LOW PASS FILTER

The LMP8275 can be effectively used to build a second order Sallen-Key low pass filter. The general filter is shown in [Figure 21](#)

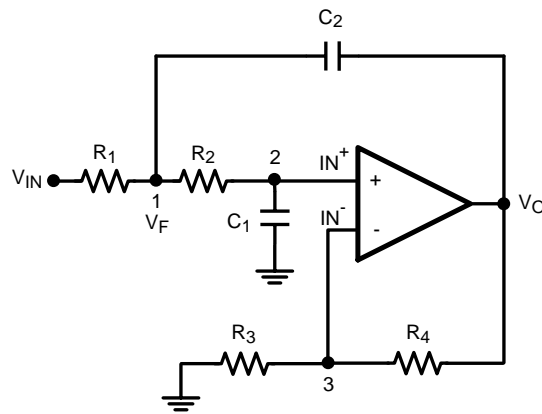


Figure 21. Second Order Low-Pass Filter

With the general transfer function:

$$\frac{V_O}{V_{IN}} = \frac{K}{M - KN}$$

where

$$M = s^2 C_1 C_2 R_1 R_2 + s(R_1 C_1 + R_1 C_2 + C_1 R_2) + 1$$

$$N = s C_2 R_1$$

and

$$\frac{1}{K} = \frac{1}{A_{VOL}} + \frac{R_3}{R_3 + R_4} \tag{3}$$

K represents the sum of DC closed loop gain and the non-ideal behavior of the operational amplifier. Assuming ideal behavior, the equation for K reduces simply to the DC gain, which is +2 for the LMP8275.

The LMP8275 can be used to realize this configuration as shown in [Figure 22](#):

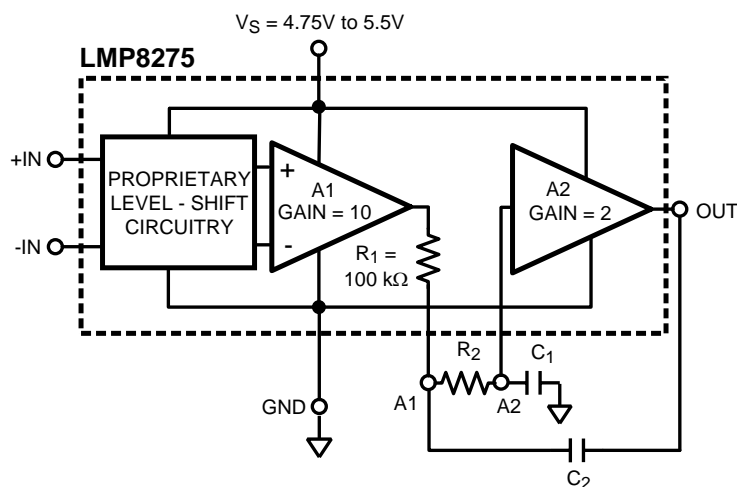


Figure 22. Low-Pass Filter With LMP8275

Assuming ideal behavior, the equation for K reduces simply to the DC gain, which is set for +2 for the LMP8270.

Using Equation 3, the filter parameters can be calculated as follows:

$$\omega_o = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

$$f_c = \frac{1}{2\pi \sqrt{R_1 R_2 C_1 C_2}}$$

$$Q = \frac{\sqrt{R_1 R_2 C_1 C_2}}{R_1 C_1 + R_2 C_1 + (1-K)R_1 C_2} \quad (4)$$

for the LMP8275, $R_1 = 100 \text{ k}\Omega$. Setting $R_1 = R_2$ and $C_1 = C_2$ results in a low pass filter with $Q = 1$. Since the values of resistors are predetermined, the corner frequency of this implementation of the filter depends on the capacitor values.

GAINS OTHER THAN 20

The LMP8275 has an internal gain of +20; however this gain can be modified. The signal path between the two amplifiers is available as external pins.

GAINS LESS THAN 20

Figure 23 shows the configuration used to reduce the LMP8275 gain.

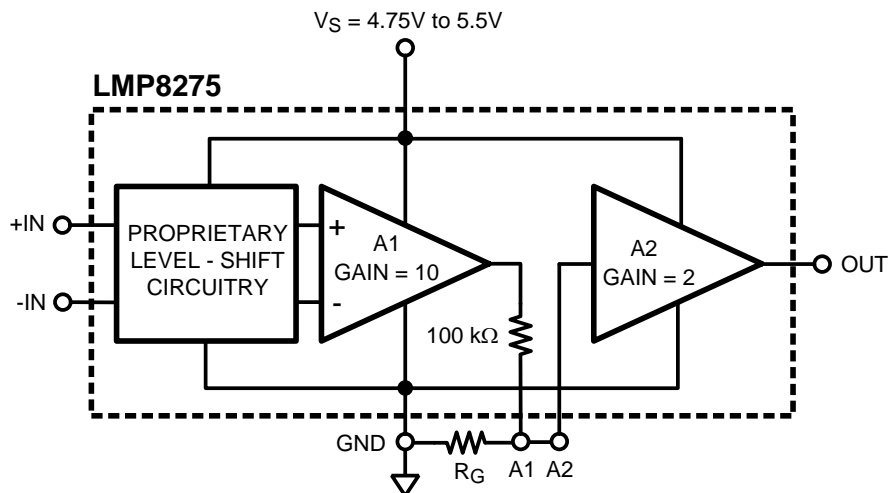


Figure 23. Gains Less Than 20

Where:

$$\text{GAIN (NEW)} = \frac{20 R_G}{R_G + 100 \text{ k}\Omega} \quad (5)$$

and

$$R_G = (100 \text{ k}\Omega) \frac{\text{GAIN (NEW)}}{20 - \text{GAIN (NEW)}} \quad (6)$$

GAINS GREATER THAN 20

A higher gain can be achieved by using positive feedback on the second stage amplifier, A2, of LMP8275. Figure 24 shows the configuration:

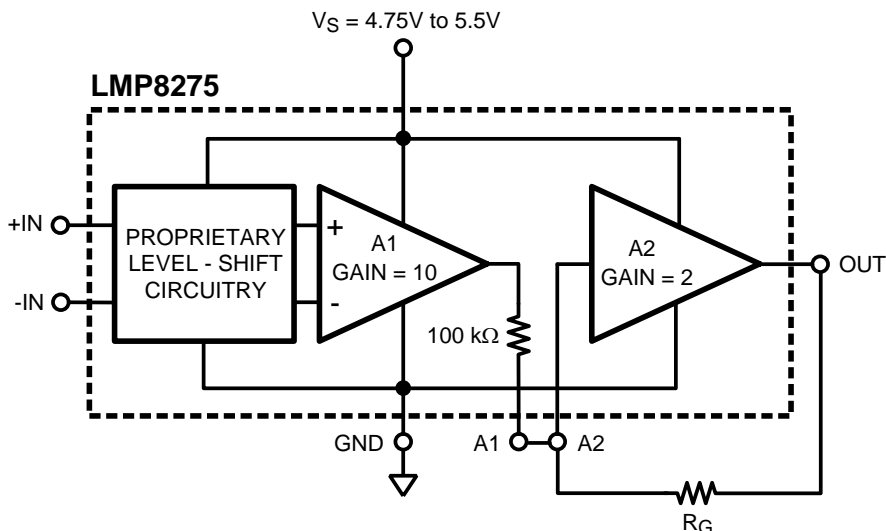


Figure 24. Gains Greater Than 20

The total gain is given by:

$$\text{GAIN (NEW)} = \frac{20 R_G}{R_G - 100 \text{ k}\Omega} \quad (7)$$

Which can be rearranged to calculate R_G :

$$R_G = (100 \text{ k}\Omega) \frac{\text{GAIN (NEW)}}{\text{GAIN (NEW)} - 20} \quad (8)$$

The inverting gain of the second amplifier is set at 2, giving the total system a gain of 20. The non-inverting gain which is achieved through positive gain can be less than or equal to this gain without any issues. This implies a total gain of 40 or less is easily achievable. Once the positive gain surpasses the negative gain, the system might oscillate.

As the value of gain resistor, R_G , approaches that of the internal 100 k Ω resistor, maintaining gain accuracy will become more challenging. This is because Gain (new) is inversely proportional to $(R_G - 100 \text{ k}\Omega)$, see Equation 7. As $R_G \rightarrow 100 \text{ k}\Omega$, the denominator of Equation 7 gets smaller. This smaller value will be comparable to the tolerance of the 100 k Ω resistor and R_G and hence the gain will be dominated by accuracy level of these resistors and the gain tolerance will be determined by the tolerance of the external resistor used for R_G and the 3% tolerance of the internal 100 k Ω resistor.

CURRENT LOOP RECEIVER

Many types of process control instrumentation use 4 to 20 mA transmitters to transmit the sensor's analog value to a central control room. The LMP8275 can be used as a current loop receiver as shown in Figure 25.

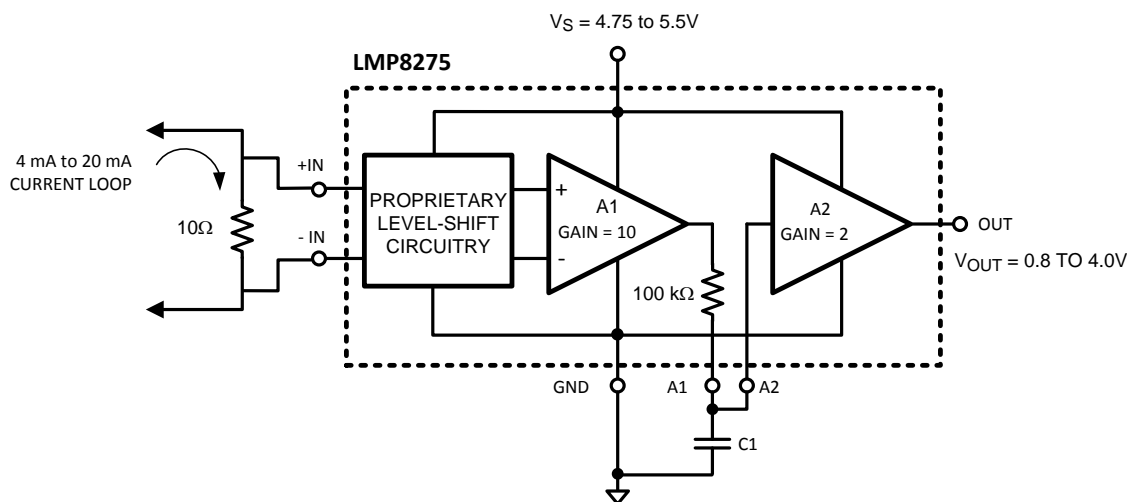


Figure 25. Current Loop Receiver

HIGH SIDE CURRENT SENSING

High side current measurement requires a differential amplifier with gain. Here the DC voltage source represent a common mode voltage with the +IN input at the supply voltage and the -IN input very close to the supply voltage. The LMP8275 can be used with a common mode voltage, V_{DC} in this case, of up to 16V.

The LMP8275 can be used for high side current sensing. The large common mode voltage range of this device allows it to sense signals outside of its supply voltage range. Also, the LMP8275 has very high CMRR, which enables it to sense very small signals in the presence of larger common mode signals. The system in [Figure 26](#) couples these two characteristics of the LMP8275 in an automotive application. The signal through R_{S1} is detected and amplified by the LMP8275 in the presence of a common mode signal of up to 16V with the highest accuracy.

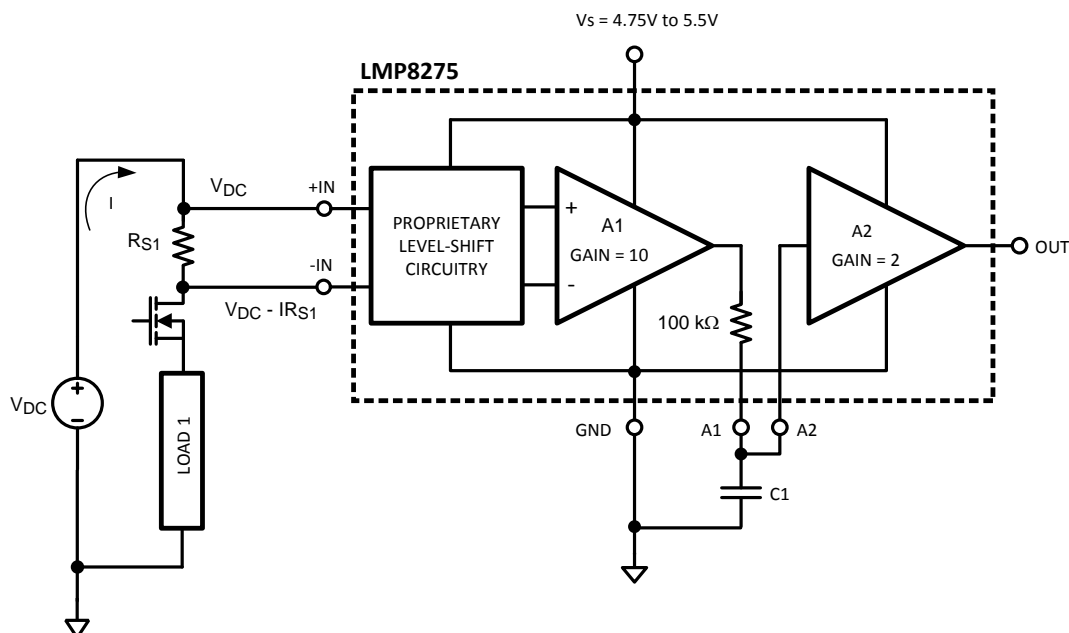


Figure 26. High Side Current Sensing

LOW SIDE CURRENT SENSING

Low side current measurements can cause a problem for operational amplifiers by exceeding the negative common mode voltage limit of the device. In [Figure 27](#), the load current is returning to the power source through a common connection that has a parasitic resistance. The voltage drop across the parasitic resistances can cause the ground connection of the measurement circuits to be at a positive voltage with respect to the common side of the sense resistor. This will result in one or both of the inputs being negative with respect to the measurement circuit's ground. The LMP8275 has a wide input common mode voltage range of $-2V$ to $16V$ and will function in this condition.

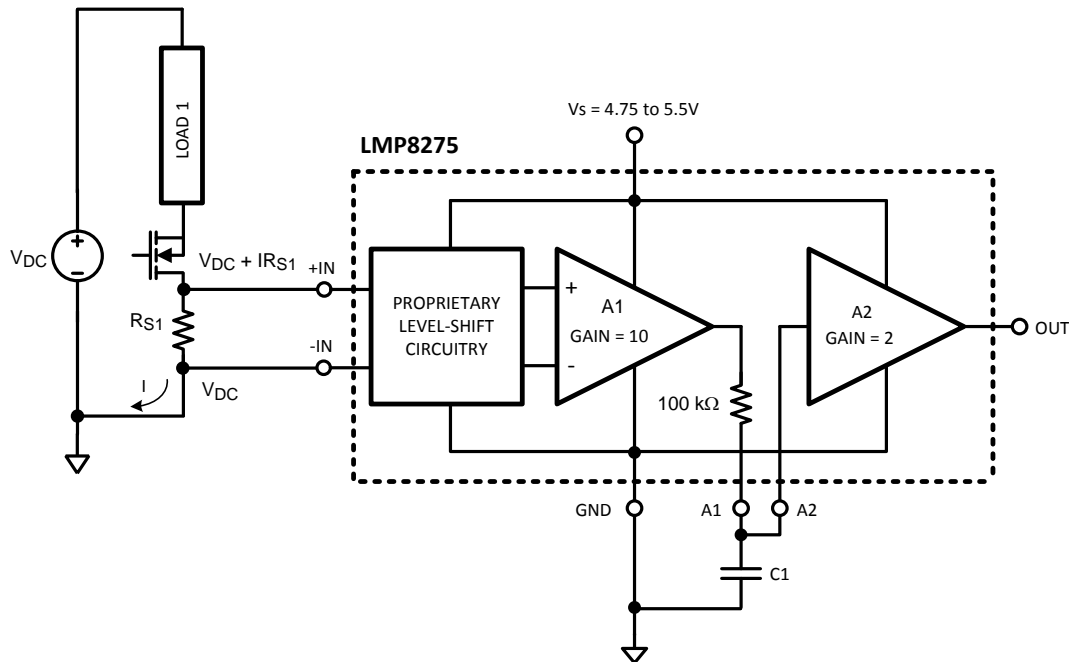


Figure 27. Low Side Current Sensing

REVISION HISTORY

Changes from Revision F (April 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	13

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