LM10QML Operational Amplifier and Voltage Reference

Check for Samples: LM10QML

FEATURES

- **Input Offset Voltage: 2.0 mV (max)**
- **Input Offset Current: 0.7 nA (max)**
- **Input Bias Current: 20 nA (max)**
- **Reference Regulation: 0.1% (max)**
- **Offset Voltage Drift: 2μV/°C**
- **Reference Drift: 0.002%/°C**

DESCRIPTION

The LM10 is a monolithic linear IC consisting of a precision reference, an adjustable reference buffer and an independent, high quality op amp.

The unit can operate from a total supply voltage as low as 1.1V or as high as 40V, drawing only 270μA. A complementary output stage swings within 15 mV of the supply terminals or will deliver ±20 mA output current with ±0.4V saturation. Reference output can be as low as 200 mV.

The circuit is recommended for portable equipment and is completely specified for operation from a single power cell. In contrast, high output-drive capability, both voltage and current, along with thermal overload protection, suggest it in demanding general-purpose applications.

The device is capable of operating in a floating mode, independent of fixed supplies. It can function as a remote comparator, signal conditioner, SCR controller or transmitter for analog signals, delivering the processed signal on the same line used to supply power. It is also suited for operation in a wide range of voltage- and current-regulator applications, from low voltages to several hundred volts, providing greater precision than existing ICs.

Connection and Functional Diagram

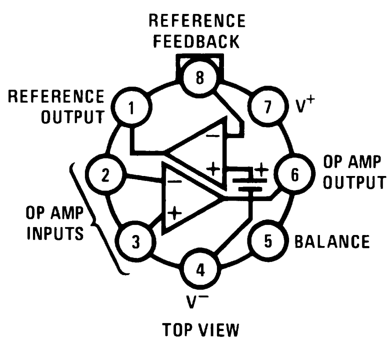


Figure 1. TO Package (NEV)
Package Number NEV0008A

Figure 2. Operational Amplifier Schematic — (Pin numbers are for 8-pin packages)

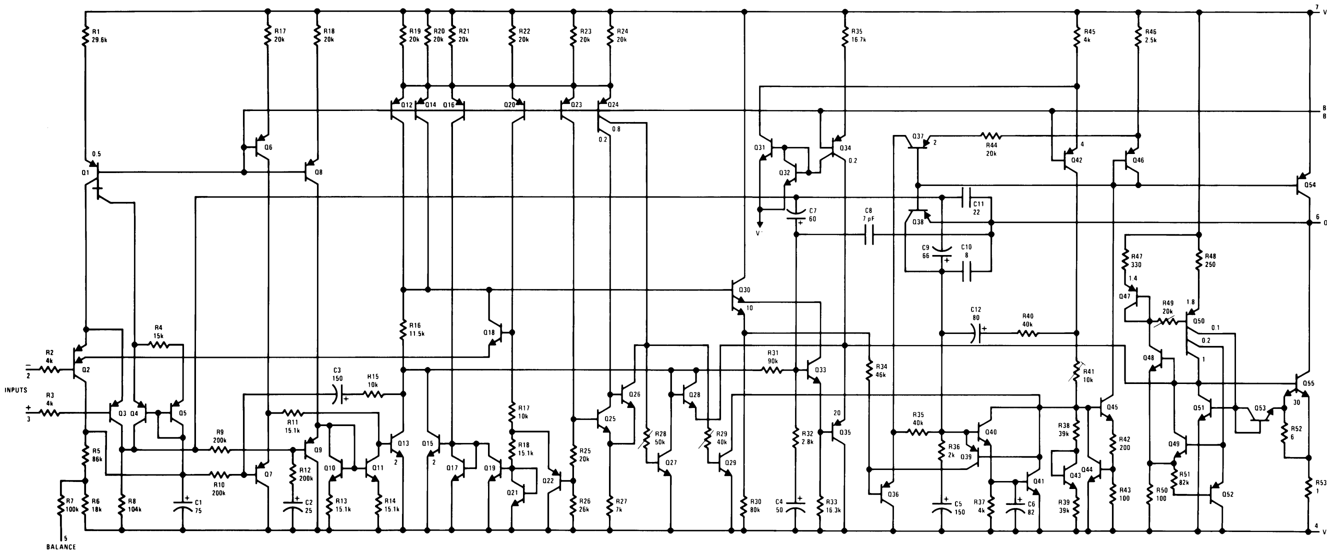
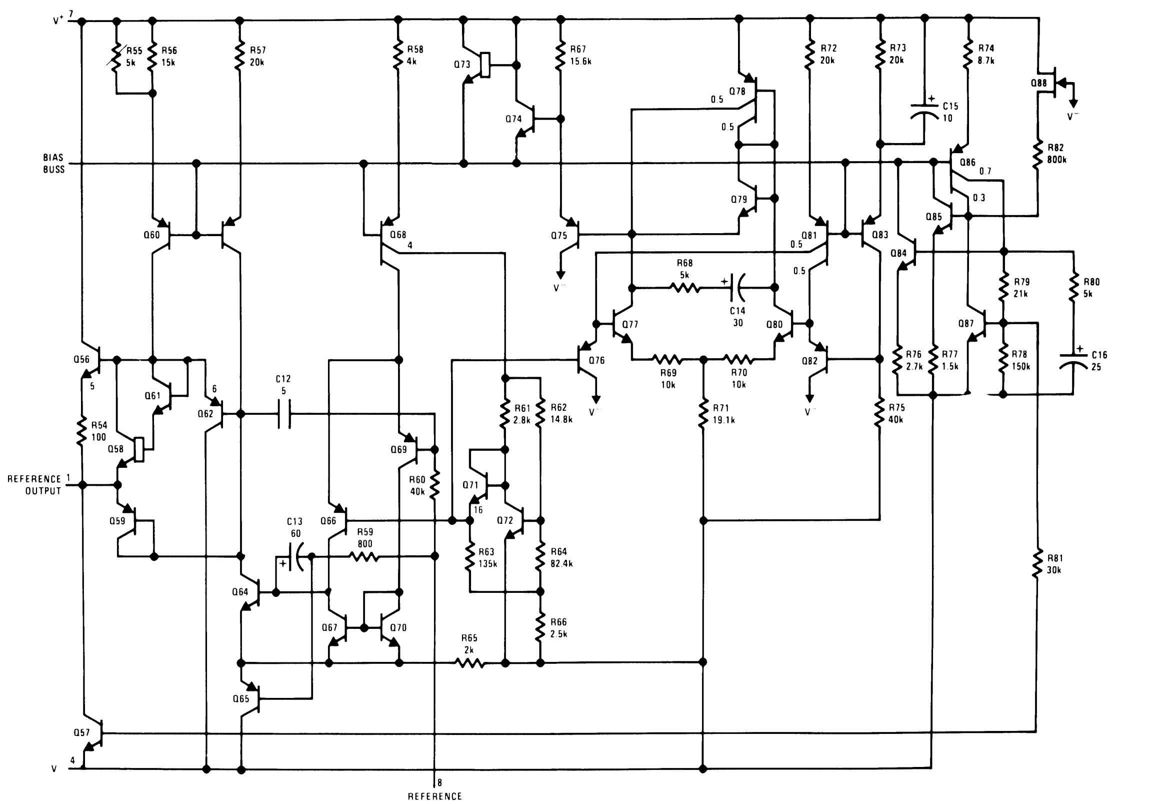


Figure 3. Reference and Internal Regulator Schematic — (Pin numbers are for 8-pin packages)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Total Supply Voltage			45V
Differential Input Voltage (2)			±40V
Power Dissipation (P_{Dmax}) (3)			Internally Limited
Output Short-circuit Duration (4)			Continuous
Storage Temperature Range			−55°C ≤ T_A ≤ +150°C
Maximum Junction Temperature (T_{Jmax})			150°C
Lead Temperature (Soldering 10 seconds)			300°C
Thermal Resistance	θ_{JA}	Still Air	150°C
		500LF/Min Air flow	45°C
	θ_{JC}		45°C
ESD			Rating to be determined

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) The Input voltage can exceed the supply voltages provided that the voltage from the input to any other terminal does not exceed the maximum differential input voltage and excess dissipation is accounted for when $V_I < V_S^-$.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower..
(4) Internal thermal limiting prevents excessive heating that could result in sudden failure, but the IC can be subjected to accelerated stress with a shorted output and worst-case conditions.

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp °C
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

LM10H Electrical Characteristics DC Parameters

The following conditions apply to all the following parameters, unless otherwise specified.
DC: At room temperature 1.2V ≤ V_S ≤ 45V, V_S^- ≤ V_{CM} ≤ V± 0.85V.
DC: At temperature extremes 1.3V ≤ V_S ≤ 45V, V_S^- ≤ V_{CM} ≤ V± 1.0V.

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	I_O = 0mA		-2.0	2.0	mV	1
				-3.0	3.0	mV	2, 3
		V_S = 1.2V, I_O = ±2mA		-3.0	3.0	mV	1
		V_S = 1.3V, I_O = ±2mA		-4.0	4.0	mV	2, 3
		V_S = 4V, I_O = ±20mA		-3.0	3.0	mV	1
		V_S = 4V, I_O = ±15mA		-4.0	4.0	mV	2, 3
I_{IO}	Input Offset Current			-0.7	0.7	nA	1
				-1.5	1.5	nA	2, 3
I_{IB}	Input Bias Current				20	nA	1
					30	nA	2, 3
CMRR	Common Mode Rejection	V_S = 45V, -20V ≤ V_{CM} ≤ 24.2V		93		dB	1
				87		dB	2, 3
PSRR	Supply Voltage Rejection	V_S^+ = 0.85V, -0.35V ≥ V_S^- ≥ -44.2V		90		dB	1
		V_S^+ = 1V, -0.3V ≥ V_S^- ≥ -44.2V		84		dB	2, 3
		0.85V ≤ V_S^+ ≤ 44.6V, V_S^- = -0.35V		96		dB	1
		1V ≤ V_S^+ ≤ 44.6V, V_S^- = -0.3V		90		dB	2, 3
V_{RLine}	Line Regulation	I_{Ref} = 1mA		91		dB	1
				85		dB	2, 3
V_{RLoad}	Load Regulation	V_S = 1.2V, 0 ≤ I_O ≤ 1mA		60		dB	1
		V_S = 1.3V, 0 ≤ I_O ≤ 1mA		57		dB	2, 3
I_S	Supply Current				400	µA	1
					500	µA	2, 3
A_V	Large Signal Voltage Gain	V_S = ±20V, I_O = 0A, V_O = ± 19.95V		120		K	4
				80		K	5, 6
		V_S = ±2V, I_O = ±20mA, V_O = ±1.4V		5.0		K	4
		V_S = ±2V, I_O = ±15mA, V_O = ±1.4V		1.5		K	5, 6
		V_S^+ = 0.85V, V_{CM} = -0.25V V_S^- = -0.35V, I_O = ±2mA, -0.15V ≤ V_O ≤ 0.65V,		1.5		K	4
		V_S^+ = 1V, V_{CM} = -0.35V V_S^- = -0.3V, I_O = ±2mA, +0.05V ≤ V_O ≤ 0.65V,		0.5		K	5, 6
A_{VSH}	Shunt Gain	1.1V ≤ V_{OUT} ≤ 6.1V, -5mA ≤ I_{OUT} ≤ -0.1mA	See [(1)]	14		K	4
		1.2V ≤ V_{OUT} ≤ 6.2V, -5mA ≤ I_{OUT} ≤ -0.1mA	See [(1)]	6.0		K	5, 6
		1.4V ≤ V_{OUT} ≤ 6.4V, -5mA ≤ I_{OUT} ≤ -0.1mA	See [(1)]	8.0		K	4
		1.4V ≤ V_{OUT} ≤ 6.4V, -20mA ≤ I_{OUT} ≤ -0.1mA	See [(1)]	4.0		K	5, 6

(1) This defines operation in floating applications such as the bootstrapped regulator or two-wire transmitter. Output is connected to the V_S^+ terminal of the IC and input common mode is referred to V_S^-(see Typical Applications -). Effect of larger output-voltage swings with higher load resistance can be accounted for by adding the positive-supply rejection error.

LM10H Electrical Characteristics DC Parameters (continued)

The following conditions apply to all the following parameters, unless otherwise specified.
DC: At room temperature $1.2V \leq V_S \leq 45V$, $V_S^- \leq V_{CM} \leq V\pm 0.85V$.
DC: At temperature extremes $1.3V \leq V_S \leq 45V$, $V_S^- \leq V_{CM} \leq V\pm 1.0V$.

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
A_V	Amplifier Gain	$0.2V \leq V_{Ref} \leq 35V$, $I_{Ref} = 1mA$		50		K	
				23		K	
V_{Sense}	Feedback Sense Voltage	$0.2V \leq V_{Ref} \leq 35V$, $0 \leq I_{Ref} \leq 1$ mA		195	205	mV	
				194	206	mV	
I_{Sense}	Feedback Current				50	nA	
					65	nA	
ΔI_S	Supply Current Change	$0.5V \leq V_O \leq 25V$		-75	75	µA	
		$V_S = 5V$, $4.5V \leq V_O \leq 5V$		-60	60	µA	
R_I	Input Resistance		See (2)		250	KΩ	
			See (2)		150	KΩ	

(2) Specified parameter, not tested,

Definition of Terms

Input offset voltage: That voltage which must be applied between the input terminals to bias the unloaded output in the linear region.

Input offset current: The difference in the currents at the input terminals when the unloaded output is in the linear region.

Input bias current: The absolute value of the average of the two input currents.

Input resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Large signal voltage gain: The ratio of the specified output voltage swing to the change in differential input voltage required to produce it.

Shunt gain: The ratio of the specified output voltage swing to the change in differential input voltage required to produce it with the output tied to the V_S^+ terminal of the IC. The load and power source are connected between the V_S^+ and V_S^- terminals, and input common-mode is referred to the V_S^- terminal.

Common-mode rejection: The ratio of the input voltage range to the change in offset voltage between the extremes.

Supply-voltage rejection: The ratio of the specified supply-voltage change to the change in offset voltage between the extremes.

Line regulation: The average change in reference output voltage over the specified supply voltage range.

Load regulation: The change in reference output voltage from no load to that load specified.

Feedback sense voltage: The voltage, referred to V_S^-, on the reference feedback terminal while operating in regulation.

Reference amplifier gain: The ratio of the specified reference output change to the change in feedback sense voltage required to produce it.

Feedback current: The absolute value of the current at the feedback terminal when operating in regulation.

Supply current: The current required from the power source to operate the amplifier and reference with their outputs unloaded and operating in the linear range.

Typical Performance Characteristics (Op Amp)

Input Current

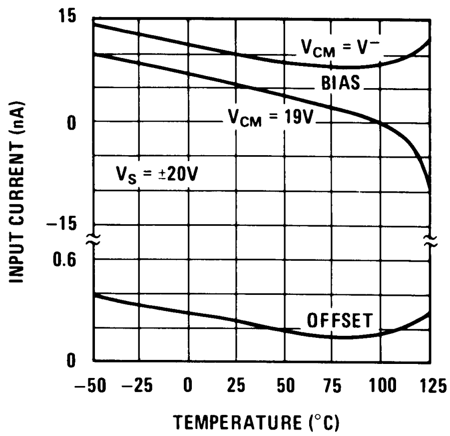


Figure 4.

Common Mode Limits

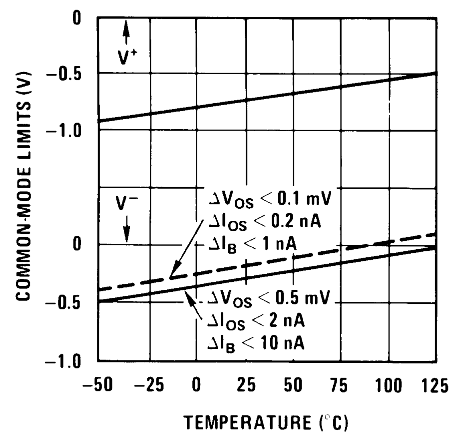


Figure 5.

Output Voltage Drift

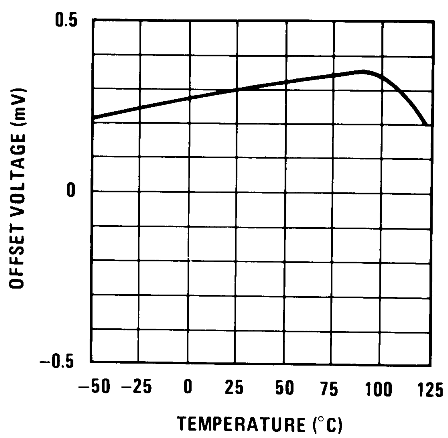


Figure 6.

Input Noise Voltage

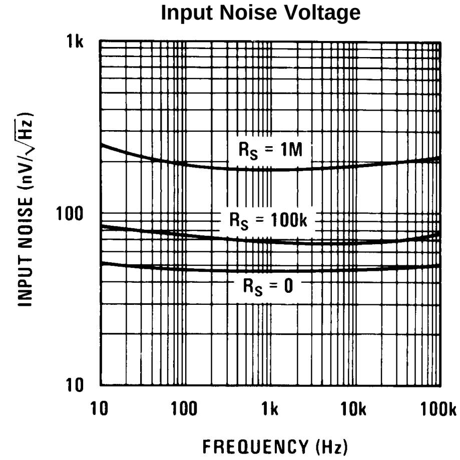


Figure 7.

DC Voltage Gain

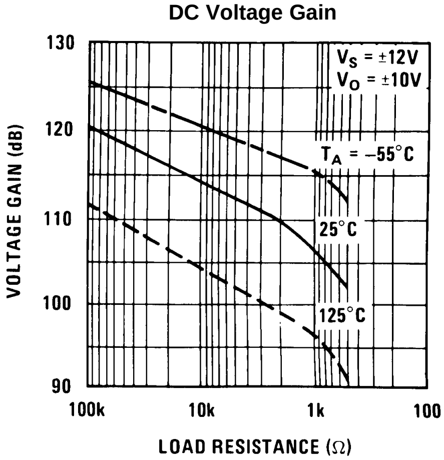


Figure 8.

Transconductance

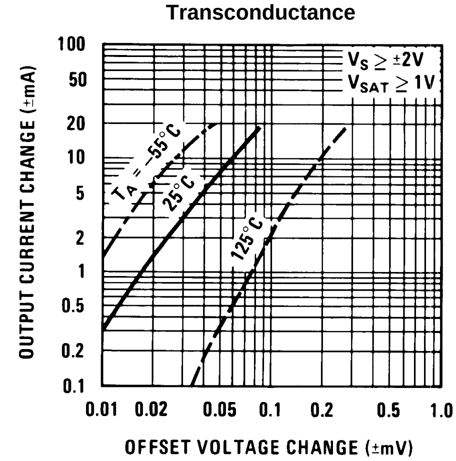


Figure 9.

Typical Performance Characteristics (Op Amp) (continued)

Output Saturation Characteristics

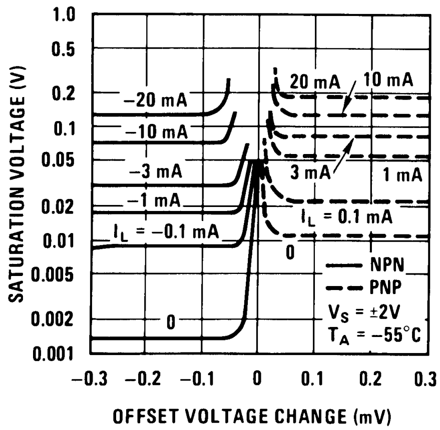


Figure 10.

Output Saturation Characteristics

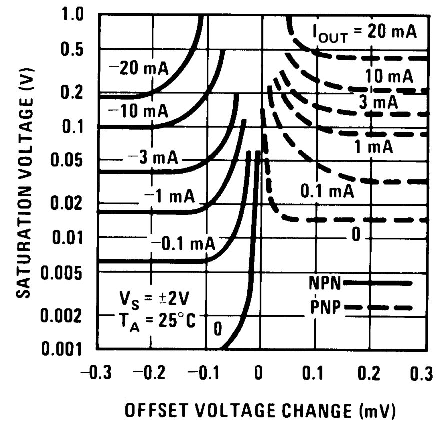


Figure 11.

Output Saturation Characteristics

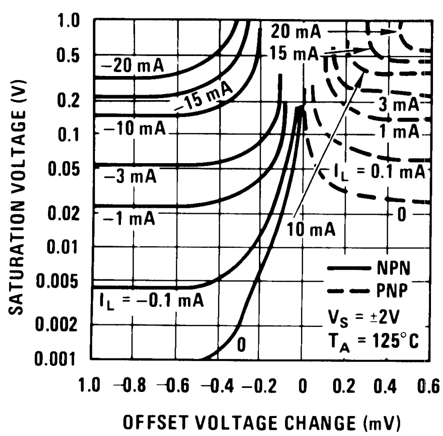


Figure 12.

Minimum Supply Voltage

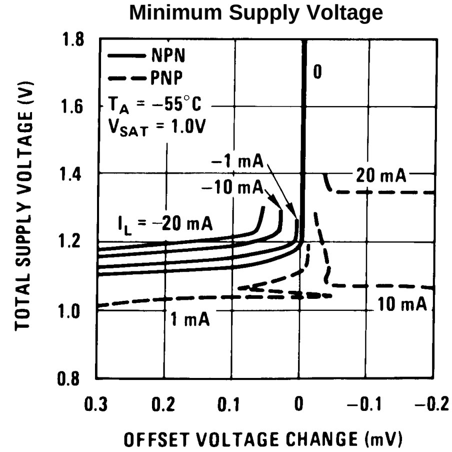


Figure 13.

Minimum Supply Voltage

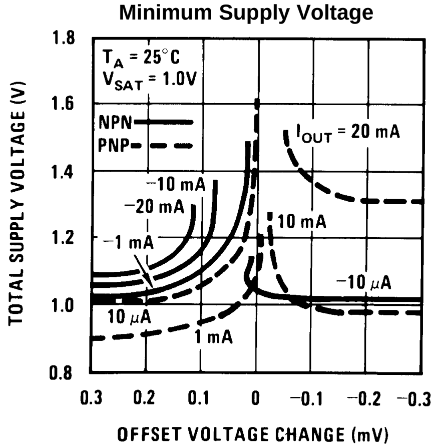


Figure 14.

Minimum Supply Voltage

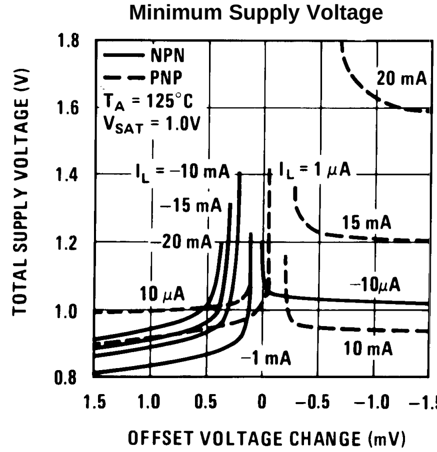


Figure 15.

Typical Performance Characteristics (Op Amp) (continued)

Frequency Response

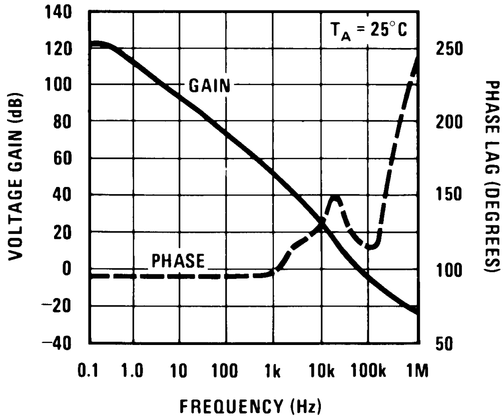


Figure 16.

Output Impedance

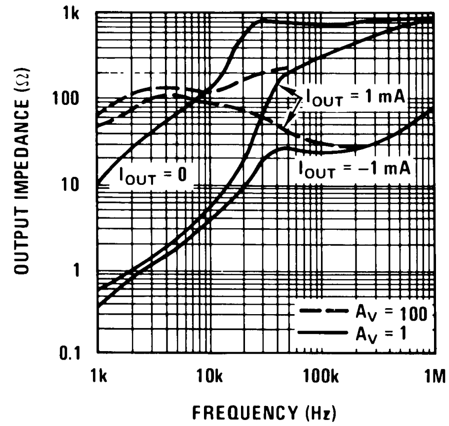


Figure 17.

Typical Stability Range

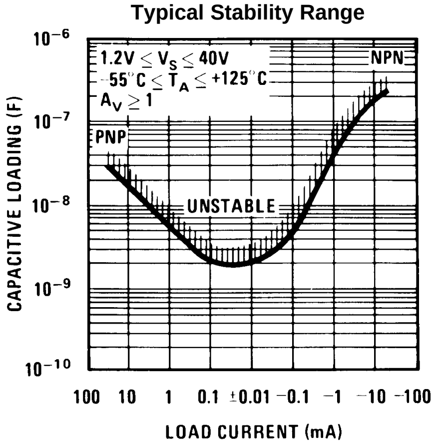


Figure 18.

Large Signal Response

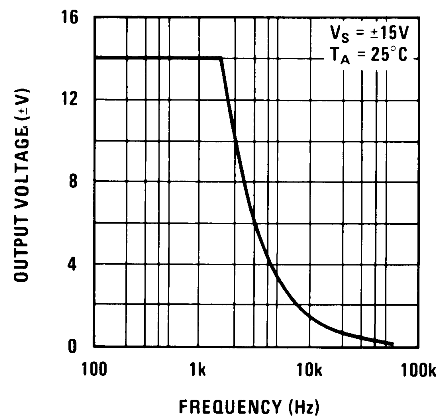


Figure 19.

Comparator Response Time For Various Input Overdrives

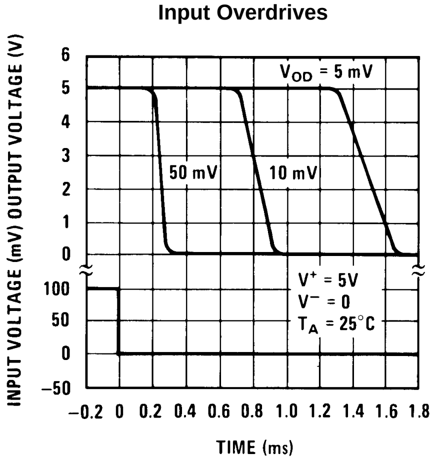


Figure 20.

Comparator Response Time For Various Input Overdrives

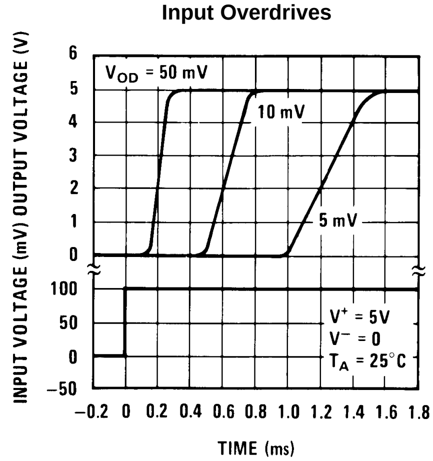


Figure 21.

Typical Performance Characteristics (Op Amp) (continued)

Follower Pulse Response

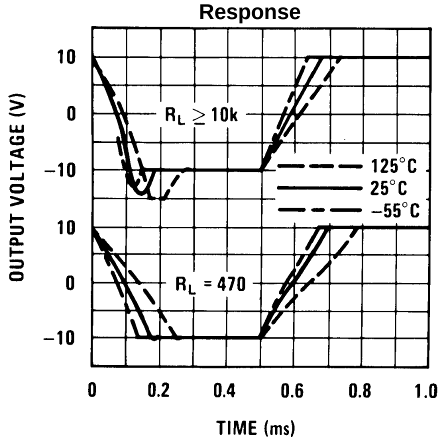


Figure 22.

Noise Rejection

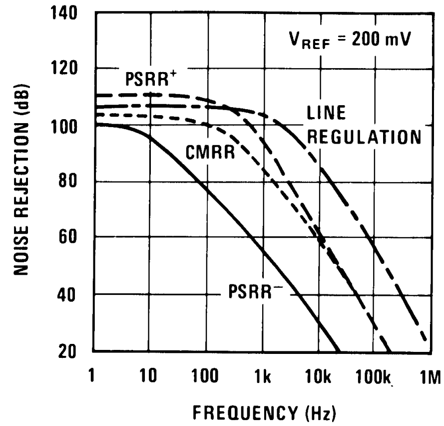


Figure 23.

Rejection Slew Limiting

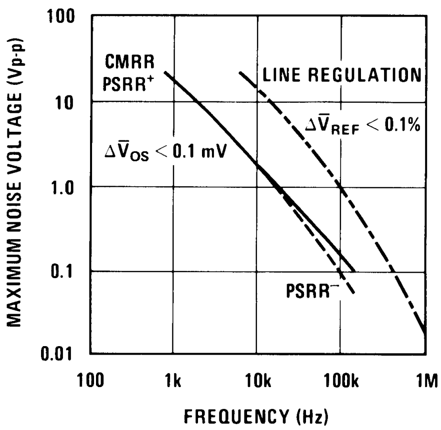


Figure 24.

Supply Current

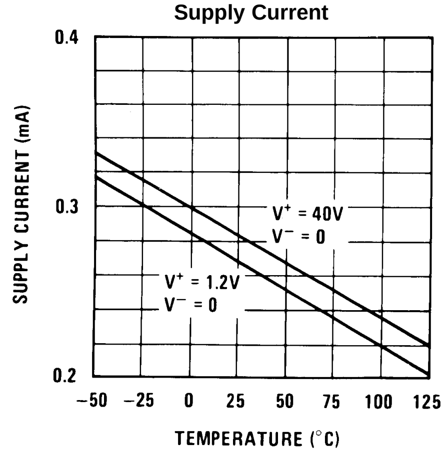


Figure 25.

Thermal Gradient Feedback

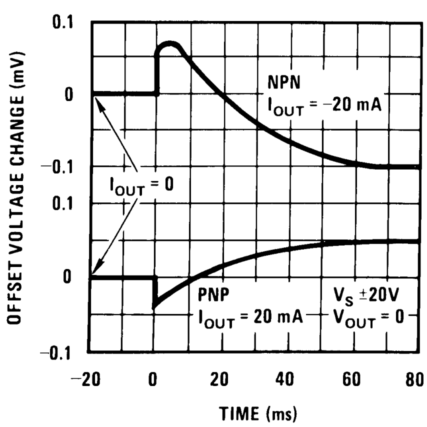


Figure 26.

Thermal Gradient Cross-coupling

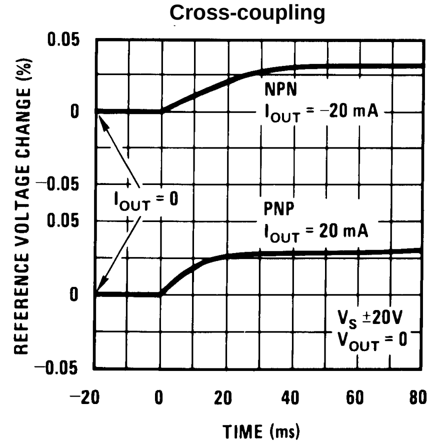


Figure 27.

Typical Performance Characteristics (Op Amp) (continued)

Shunt Gain

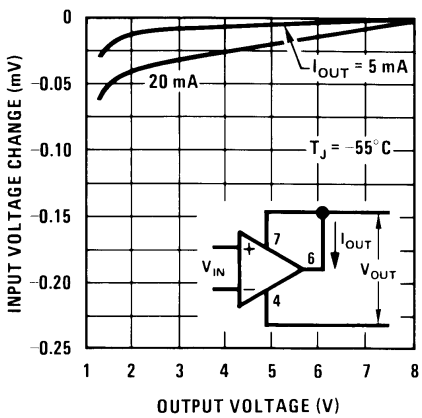


Figure 28.

Shunt Gain

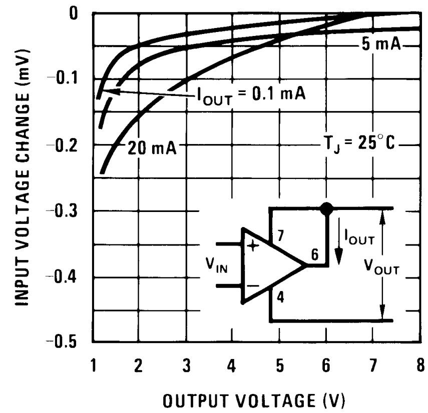


Figure 29.

Shunt Gain

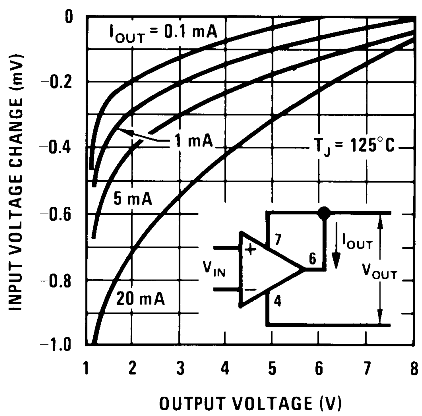


Figure 30.

Shunt Gain

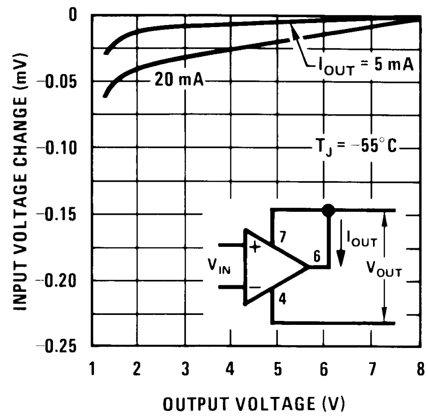


Figure 31.

Shunt Gain

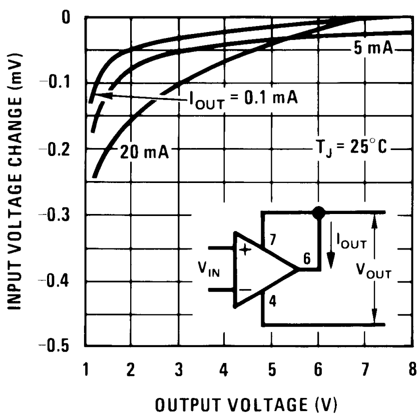


Figure 32.

Shunt Gain

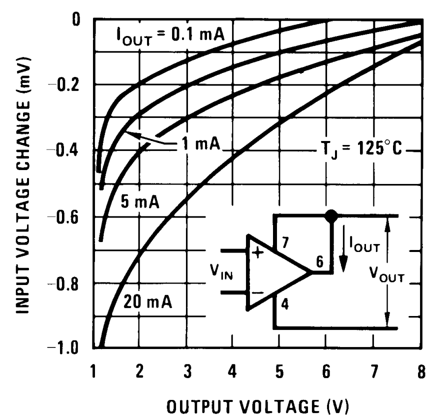


Figure 33.

Typical Performance Characteristics (Reference)

Line Regulation

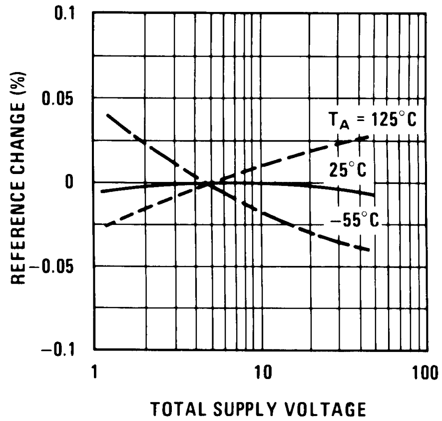


Figure 34.

Load Regulation

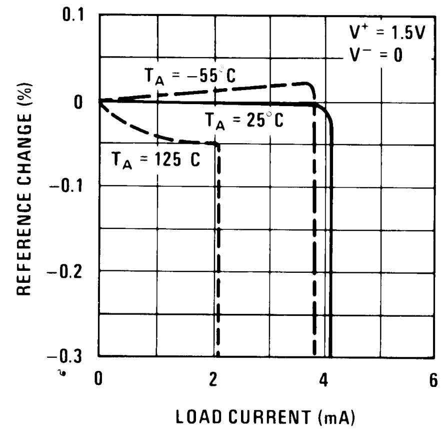


Figure 35.

Reference Noise Voltage

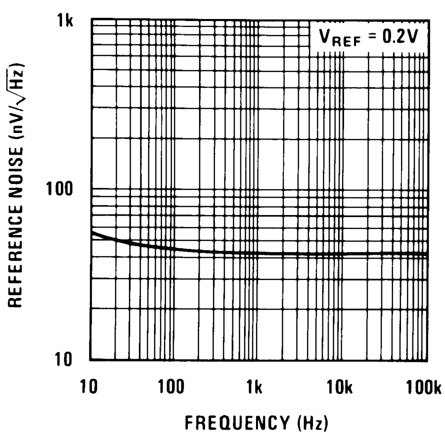


Figure 36.

Minimum Supply Voltage

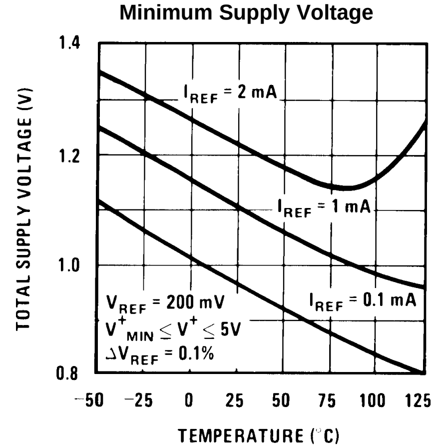


Figure 37.

Output Saturation

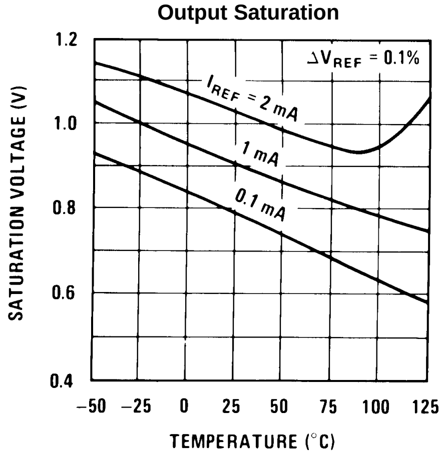


Figure 38.

Typical Stability Range

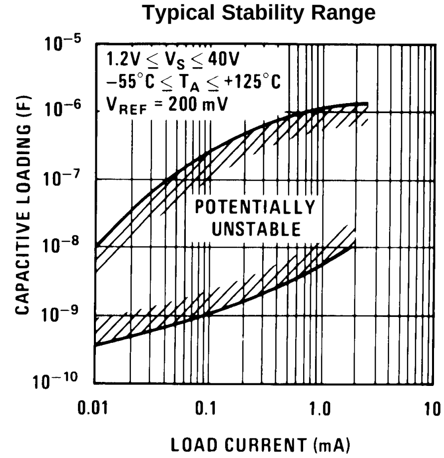


Figure 39.

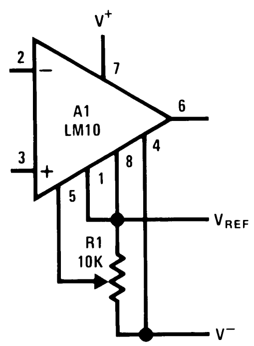
Typical Applications

Circuit descriptions available in application note AN-211 (SNOA638).

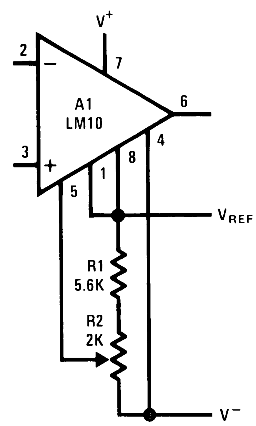
(Pin numbers are for devices in 8-pin packages)

Op Amp Offset Adjustment

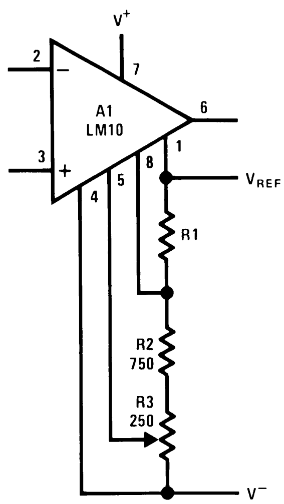
Standard



Limited Range



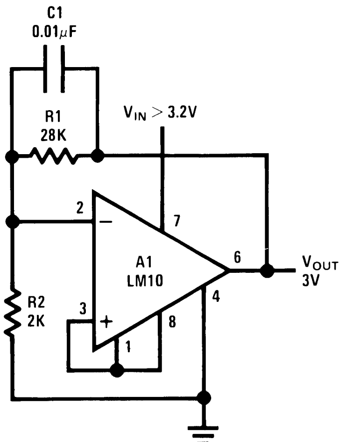
Limited Range With Boosted Reference



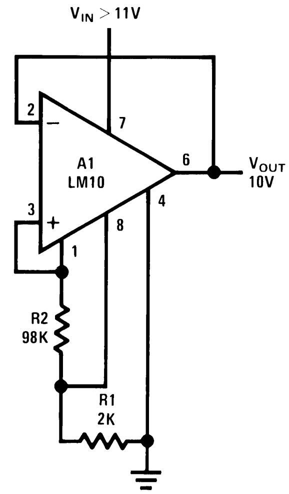
Positive Regulators

Use only electrolytic output capacitors.

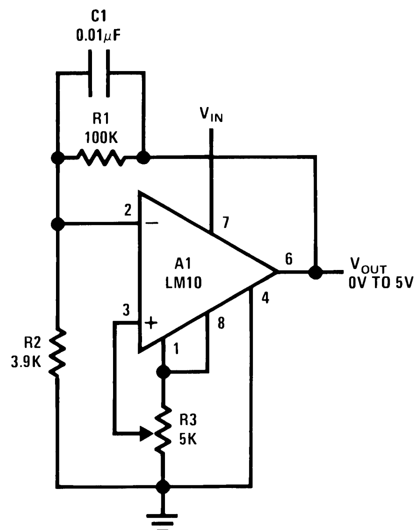
Low Voltage



Best Regulation

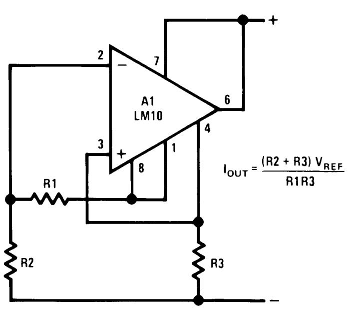


Zero Output

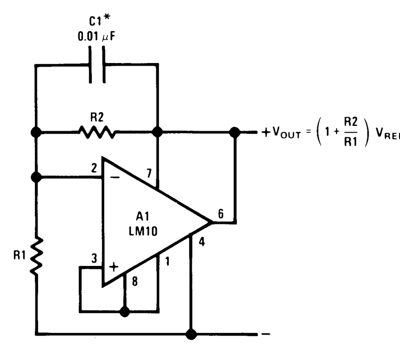


Use only electrolytic output capacitors.

Current Regulator

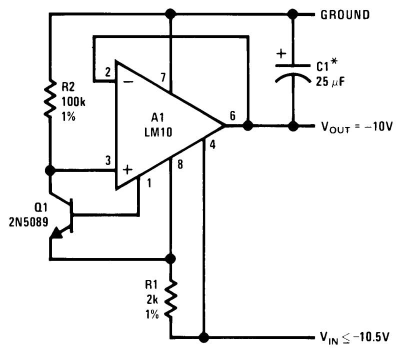


Shunt Regulator



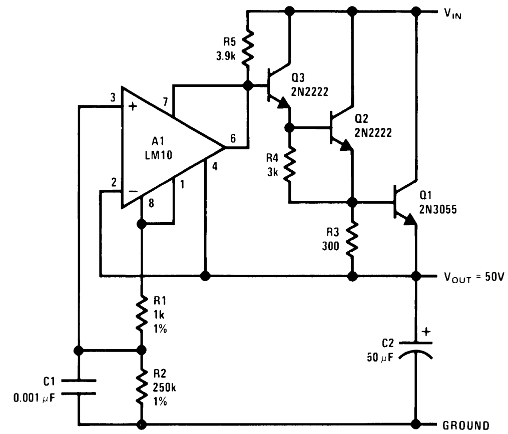
Required For Capacitive Loading

Negative Regulator

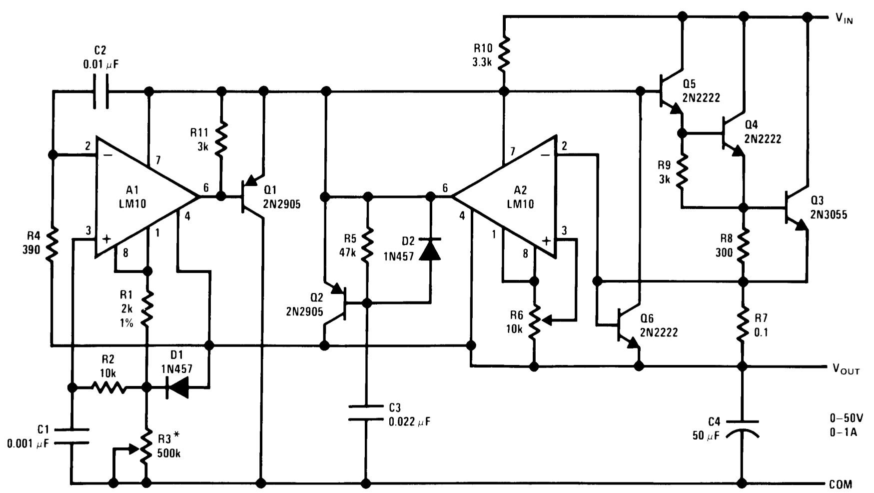


*Electrolytic

Precision Regulator

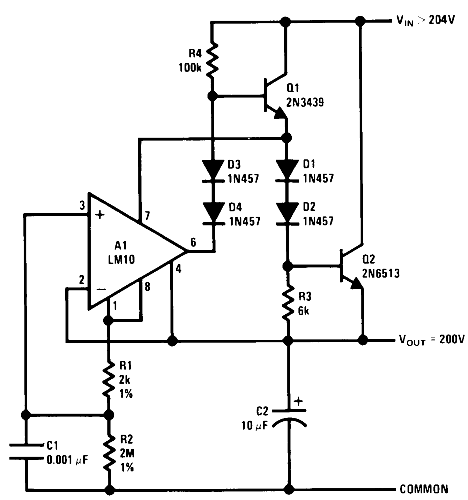


Laboratory Power Supply



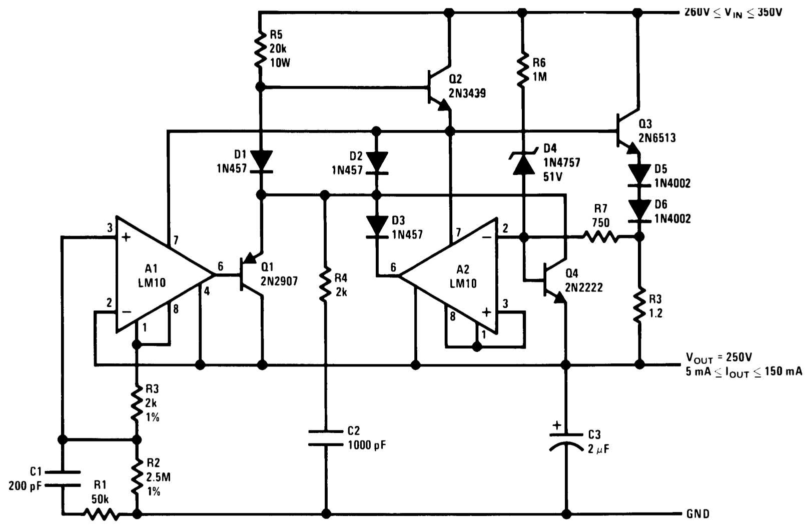
$*V_O = 10^{-4}$ R3

HV Regulator

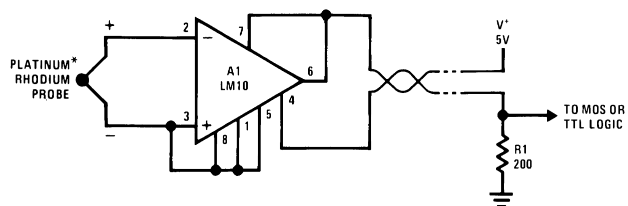


$$V_{OUT} = \frac{R2}{R1} V_{REF}$$

Protected HV Regulator

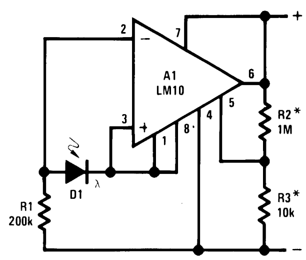


Flame Detector



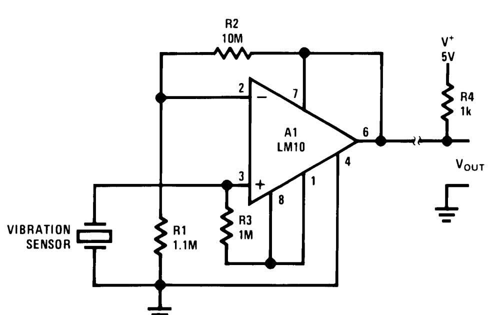
*800°C Threshold Is Established By Connecting Balance To V_{Ref}.

Light Level Sensor

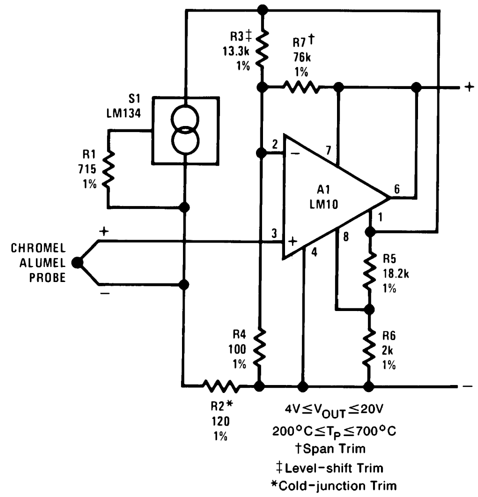


*Provides Hysteresis

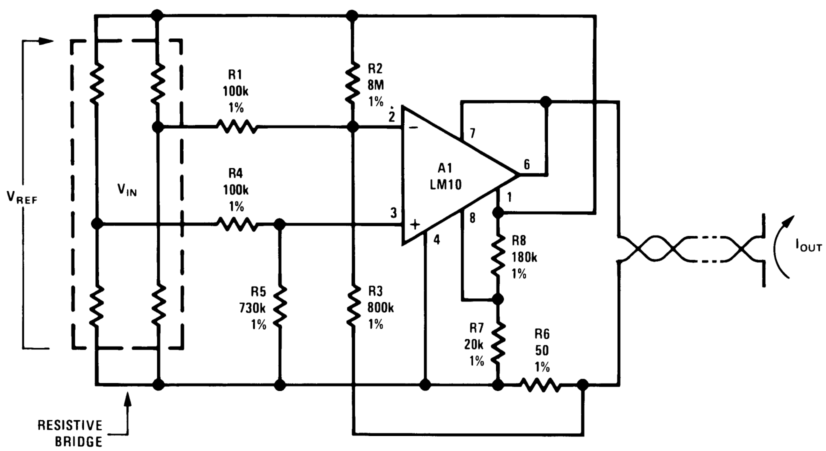
Remote Amplifier



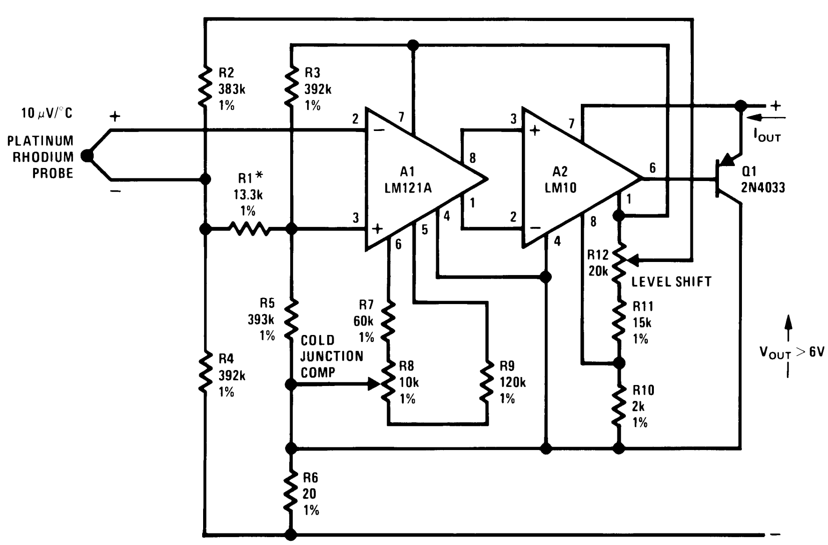
Remote Thermocouple Amplifier



Transmitter for Bridge Sensor

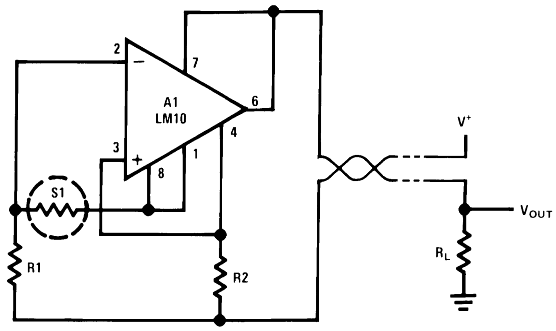


Precision Thermocouple Transmitter

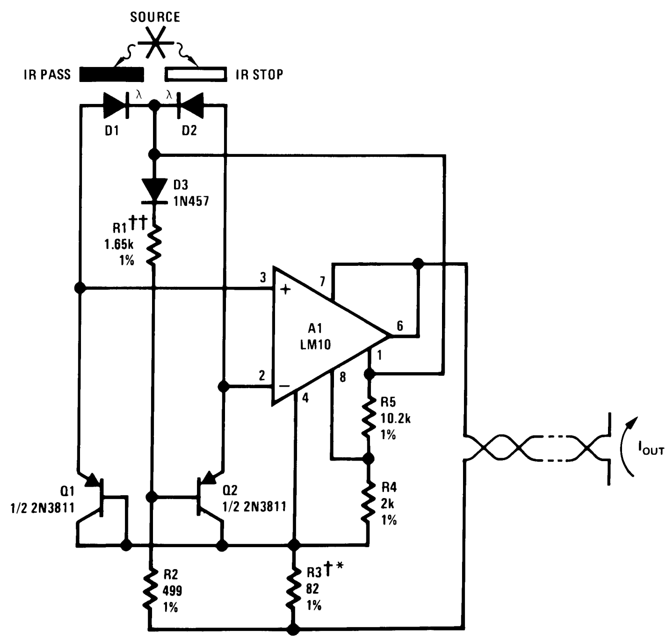


10 mA ≤ I_{OUT}≤50 mA 500°C ≤ T_P ≤ 1500°C *Gain Trim

Resistance Thermometer Transmitter



Optical Pyrometer

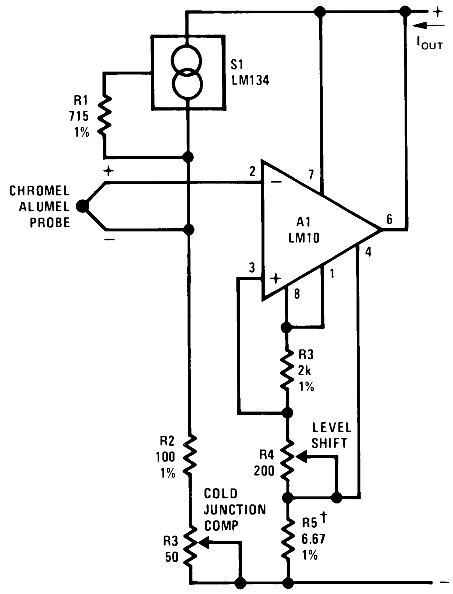


††Level-shift Trim
*Scale Factor Trim
†Copper Wire Wound

$$1\ \text{mA} \le I_{OUT} \le 5\ \text{mA}$$

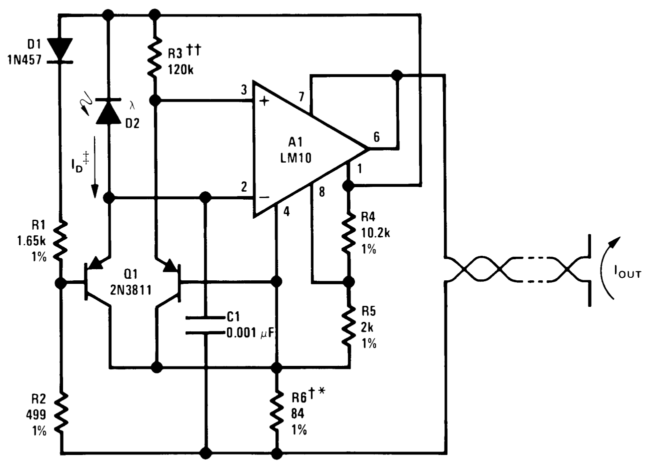
$$0.01 \le \frac{I_{D2}}{I_{D1}} \le 100$$

Thermocouple Transmitter



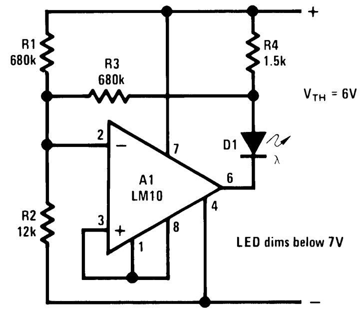
200°C≤T_p≤700°C
1 mA≤I_{OUT}≤5 mA
†Gain Trim

Logarithmic Light Sensor

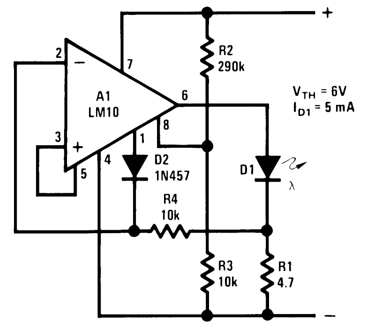


1 mA ≤ I_{OUT}≤5 mA
‡50 µA ≤ I_D ≤ 500 µA
††Center Scale Trim
†Scale Factor Trim
*Copper Wire Wound

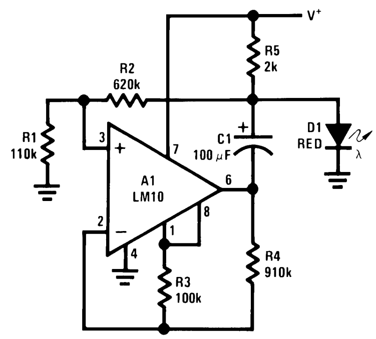
Battery-level Indicator



Battery-threshold Indicator

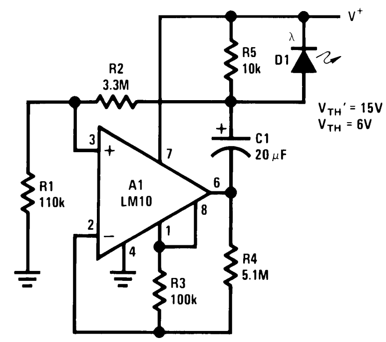


Single-cell Voltage Monitor



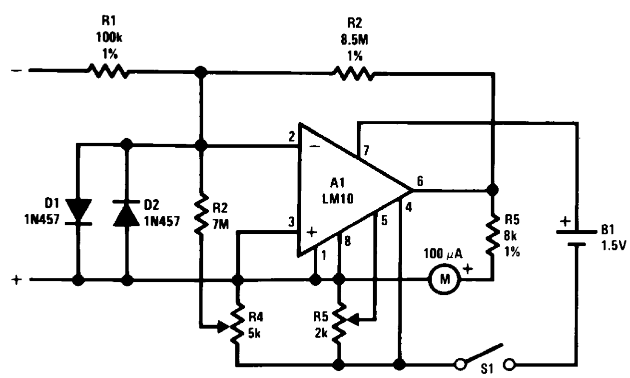
Flashes Above 1.2V
Rate Increases With
Voltage

Double-ended Voltage Monitor



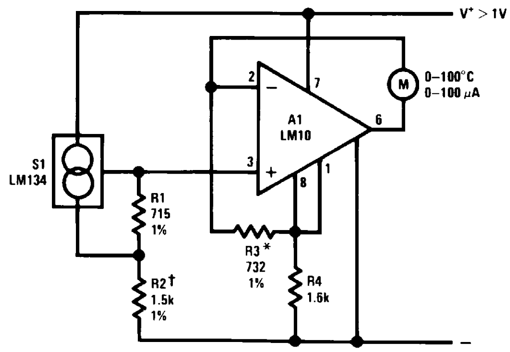
Flash Rate Increases
Above 6V and Below 15V

Meter Amplifier



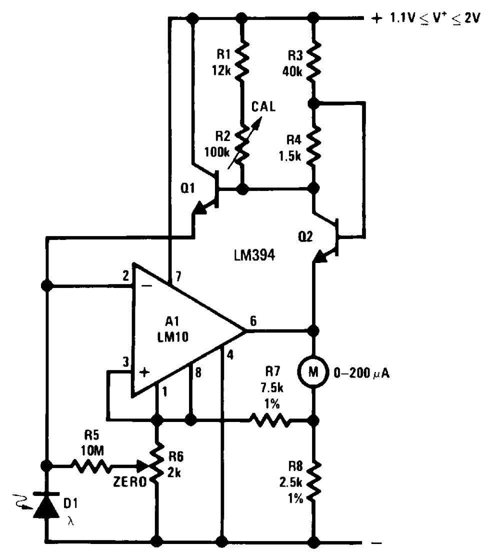
Input
10 mV, 100nA
Full-Scale

Thermometer



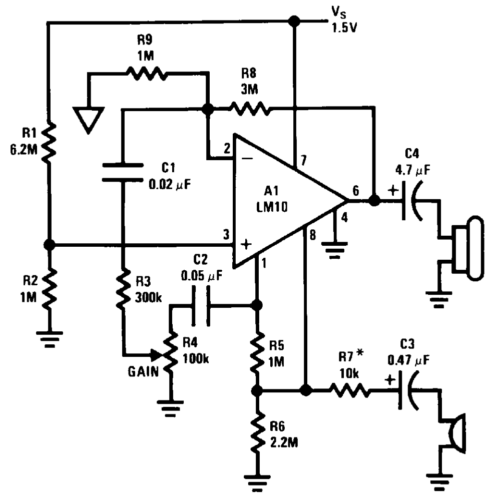
*Trim For Span
†Trim For Zero

Light Meter



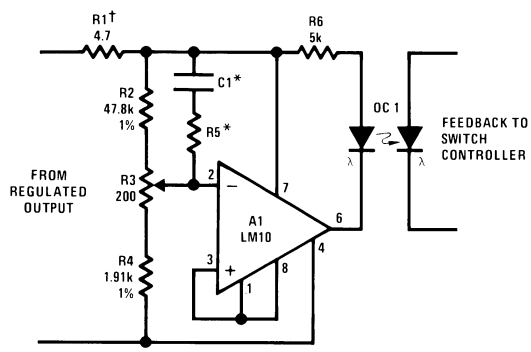
$1 \leq \lambda/\lambda_0 \leq 10^5$

Microphone Amplifier



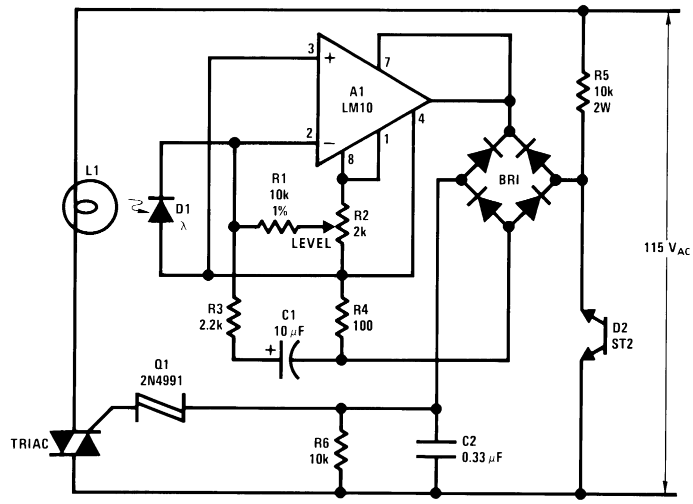
Z_{OUT}~680Ω @ 5 kHz
A_V ≤ 1k
f_1~100 Hz
f_2~5 kHz
R_L~500
*Max Gain Trim

Isolated Voltage Sensor



†Controls "Loop Gain"
*Optional Frequency Shaping

Light-level Controller



Circuit descriptions available in application note AN-211 (SNOA638).

APPLICATION HINTS

With heavy amplifier loading to V_S^-, resistance drops in the V_S^- lead can adversely affect reference regulation. Lead resistance can approach 1Ω. Therefore, the common to the reference circuitry should be connected as close as possible to the package.

Table 1. Revision History

Date Released	Revision	Section	Changes
10/26/2010	A	New release to corporate format	1 MDS converted to standard corporate format. MNLM10-X Rev 0AL will be archived
03/26/2013	A	All sections	Changed layout of National Data Sheet to TI format

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
5962-8760401GA	ACTIVE	TO	NEV	8	20	TBD	Call TI	Call TI	-55 to 125	LM10H/883 5962-8760401GA Q A CO 5962-8760401GA Q > T	Samples
LM10H/883	ACTIVE	TO	NEV	8	20	TBD	Call TI	Call TI	-55 to 125	LM10H/883 5962-8760401GA Q A CO 5962-8760401GA Q > T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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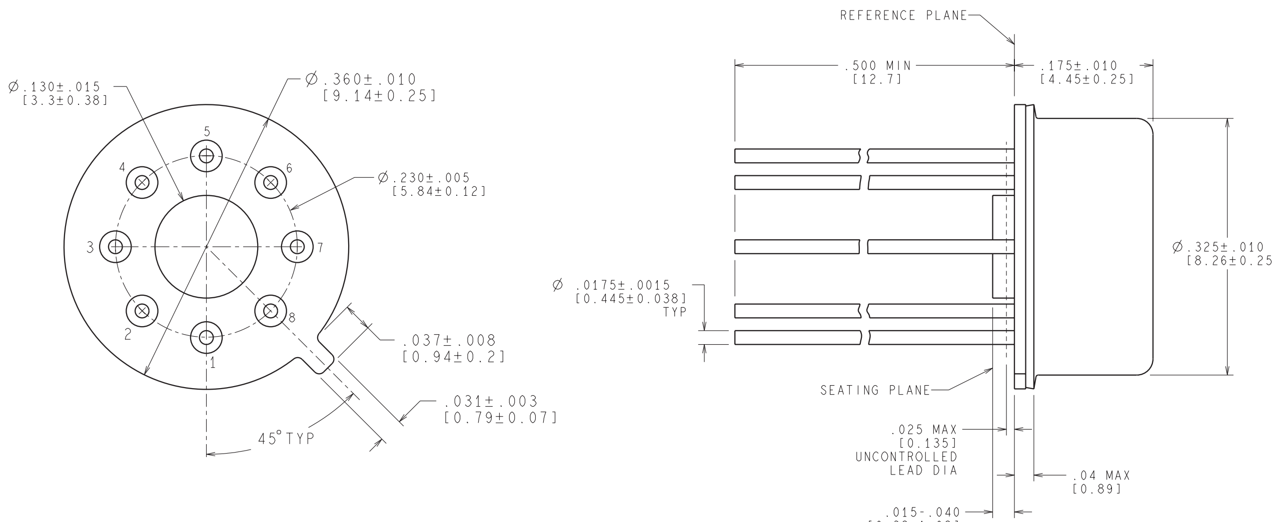

MIL-PRF-38535
CONFIGURATION CONTROL

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE IN MILLIMETERS

H08A (REV C)

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