LF156JAN JFET Input Operational Amplifiers

Check for Samples: LF156JAN

FEATURES

- **Advantages**
  - **Replace Expensive Hybrid and Module FET Op Amps**
  - **Rugged JFETs Allow Blow-Out Free Handling Compared with MOSFET Input Devices**
  - **Excellent for Low Noise Applications using either High or Low Source Impedance—Very Low 1/f Corner**
  - **Offset Adjust does not Degrade Drift or Common-Mode Rejection as in Most Monolithic Amplifiers**
  - **New Output Stage Allows use of Large Capacitive Loads (5,000 pF) without Stability Problems**
  - **Internal Compensation and Large Differential Input Voltage Capability**

APPLICATIONS

- **Precision High Speed Integrators**
- **Fast D/A and A/D Converters**
- **High Impedance Buffers**
- **Wideband, Low Noise, Low Drift Amplifiers**
- **Logarithmic Amplifiers**
- **Photocell Amplifiers**
- **Sample and Hold Circuits**

COMMON FEATURES

- **Low Input Bias Current: 30pA**
- **Low Input Offset Current: 3pA**
- **High Input Impedance: $10^{12}\Omega$**
- **Low Input Noise Current: 0.01 pA / $\sqrt{Hz}$**
- **High Common-Mode Rejection Ratio: 100 dB**
- **Large DC Voltage Gain: 106 dB**

UNCOMMON FEATURES

- **Extremely Fast Settling Time to 0.01% 1.5μs**
- **Fast Slew Rate 12V/μs**
- **Wide Gain Bandwidth 5MHz**
- **Low Input Noise Voltage 12 nV / $\sqrt{Hz}$**

DESCRIPTION

This is the first monolithic JFET input operational amplifier to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (BI-FET™ Technology). This amplifier features low input bias and offset currents/low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The device is also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/*f* noise corner.

Connection Diagrams

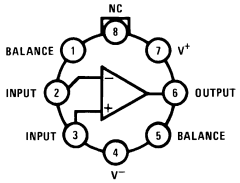
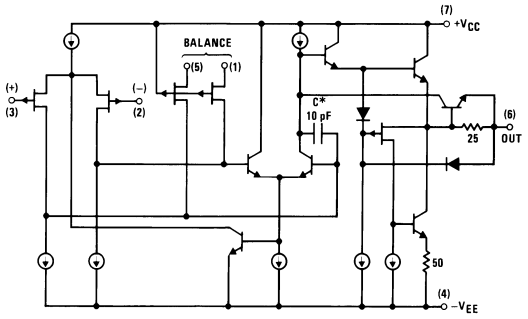


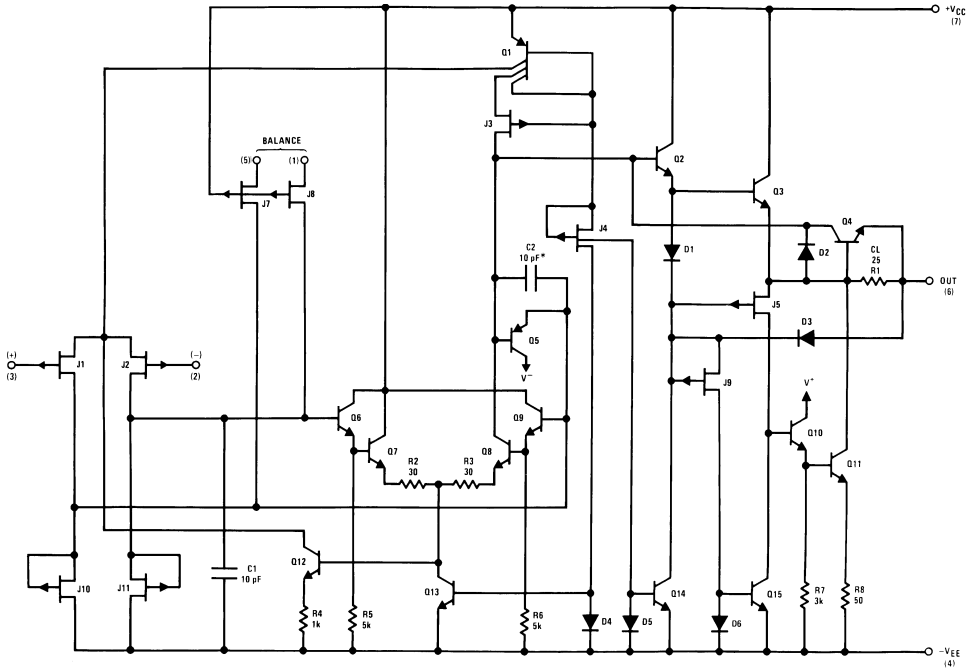
Figure 1. Top View
Metal Can Package (LMC)
See Package LMC0008C

Simplified Schematic



*3pF in LF357 series.

Detailed Schematic



*C = 3pF in LF357 series.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

Supply Voltage			±22V
Differential Input Voltage			±40V
Input Voltage Range(2)			±20V
Output Short Circuit Duration(3)			Continuous
T_{JMAX}			175°C
Power Dissipation at T_A = 25°C(4)	Still Air		560 mW
	500 LF/Min Air Flow		1200 mW
Thermal Resistance	θ_{JA}	Still Air	160°C/W
		400 LF/Min Air Flow	65°C/W
	θ_{JC}		23°C/W
Storage Temperature Range			−65°C ≤ T_A ≤ +150°C
Lead Temperature (Soldering 10 sec.)			300°C
ESD tolerance (5)			1200V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate condition for which the device is functional, but do not ensure specific performance limits . For specified specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) The absolute maximum negative input voltage is equal to the negative power supply voltage.
(3) Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax}(maximum junction temperature), θ_{JA}(package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_D=(T_{Jmax}-T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.
(5) Human body model, 100pF discharged through 1.5KΩ.

Recommended Operating Conditions

Supply voltage range	±5 to ±20 V_{DC}
Ambient temperature range	−55°C ≤ T_A ≤ +125°C

Quality Conformance Inspection

MIL-STD-883, Method 5005 - Group A

Subgroup	Description	Temp (C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25

LF156 Electrical Characteristics DC Parameters

The following conditions apply, unless otherwise specified.
DC: V_{CC} = ±20V, V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{CC}	Supply Current	+V_{CC} = 15V, -V_{CC} = -15V			7.0	mA	1
					6.0	mA	2
					11	mA	3
V_{IO}	Input Offset Voltage	+V_{CC} = 5V, -V_{CC} = -35V, V_{CM} = 15V		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
		+V_{CC} = 35V, -V_{CC} = -5V, V_{CM} = -15V		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
				-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
		+V_{CC} = 5V, -V_{CC} = -5V		-5.0	5.0	mV	1
				-7.0	7.0	mV	2, 3
±I_{IB}	Input Bias Current	+V_{CC} = 5V, -V_{CC} = -35V, V_{CM} = 15V		-0.1	3.5	nA	1
				-10	60	nA	2
		+V_{CC} = 35V, -V_{CC} = -5V, V_{CM} = -15V		-0.1	0.1	nA	1
				-10	50	nA	2
				-0.1	0.1	nA	1
				-10	50	nA	2
		+V_{CC} = 5V, -V_{CC} = -25V, V_{CM} = 10V		-0.1	0.3	nA	1
				-10	50	nA	2
I_{IO}	Input Offset Current			-0.02	0.02	nA	1
				-20	+20	nA	2
+PSRR	Power Supply Rejection Ratio	+V_{CC} = 10V, -V_{CC} = -20V		85		dB	1, 2, 3
-PSRR	Power Supply Rejection Ratio	+V_{CC} = 20V, -V_{CC} = -10V		85		dB	1, 2, 3
CMR	Input Voltage Common Mode Rejection	V_{CM} = -15V to 15V		85		dB	1, 2, 3
V_{IOAdj}(+)	Adjustment for Input Offset Voltage			8.0		mV	1, 2, 3
V_{IOAdj}(-)	Adjustment for Input Offset Voltage				-8.0	mV	1, 2, 3
+I_{OS}	Output Short Circuit Current (For Positive Output)	+V_{CC} = 15V, -V_{CC} = -15V, t ≤ 25mS		-50		mA	1, 2, 3
-I_{OS}	Output Short Circuit Current (For Negative Output)	+V_{CC} = 15V, -V_{CC} = -15V, t ≤ 25mS			50	mA	1, 2, 3
Δ V_{IO}/ΔT	Temperature Coefficient of Input Offset Voltage	25°C ≤ T_A ≤ +125°C	See (1)	-30	30	µV/°C	2
		-55°C ≤ T_A ≤ 25°C	See (1)	-30	30	µV/°C	3
-A_{VS}	Open Loop Voltage Gain (Single Ended)	V_O = -15V, R_L = 2KΩ	See (2)	50		V/mV	4
			See (2)	25		V/mV	5, 6
+A_{VS}	Open Loop Voltage Gain (Single Ended)	V_O = +15V, R_L = 2KΩ	See (2)	50		V/mV	4
			See (2)	25		V/mV	5, 6
A_{VS}	Open Loop Voltage Gain (Single Ended)	V_{CC} = ±5V, V_O = ±2V, R_L = 2KΩ	See (2)	10		V/mV	4, 5, 6
-V_{OP}	Output Voltage Swing	V_{CM} = 20V, R_L = 10KΩ			-16	V	4, 5, 6
		V_{CM} = 20V, R_L = 2KΩ			-15	V	4, 5, 6
+V_{OP}	Output Voltage Swing	V_{CM} = -20V, R_L = 10KΩ		16		V	4, 5, 6
		V_{CM} = -20V, R_L = 2KΩ		15		V	4, 5, 6

(1) Calculated parameter.
(2) Datalog Reading in K = V/mV.

LF156 Electrical Characteristics AC Parameters

The following conditions apply, unless otherwise specified.
AC: V_{CC} = ±15V, V_{CM} = 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
-SR	Slew Rate Fall	V_I = 5V to -5V, A_V = 1		7.5		V/µS	7
				5		V/µS	8A, 8B
+SR	Slew Rate Rise	V_I = -5V to 5V, A_V = 1		7.5		V/µS	7
				5		V/µS	8A, 8B
TR_{TR}	Transient Response Rise Time	R_L = 2KΩ, C_L= 100pF, V_I = 50mV, A_V = 1			100	nS	7, 8A, 8B
TR_{OS}	Transient Response Overshoot	R_L = 2KΩ, C_L = 100pF, V_I = 50mV, A_V = 1			40	%	7, 8A, 8B
NI_{BB}	Noise Broad Band	BW = 5KHz, V_{CC} = ±20V			10	$µV_{RMS}$	7
NI_{PC}	Noise Popcorn	BW = 5KHz, V_{CC} = ±20V			40	$µV_{PK}$	7
tS (+)	Settling Time	A_V = -1			1500	nS	12
tS (-)	Settling Time	A_V = -1			1500	nS	12

LF156 Electrical Characteristics Drift Values

The following conditions apply, unless otherwise specified.
AC: V_{CC} = ±20V, V_{CM} = 0V
Delta calculations performed on JAN S devices at group B, subgroup 5 only

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage			-1.0	1.0	mV	1
$±I_{IB}$	Input Bias Current			-0.05	0.05	nA	1

Typical DC Performance Characteristics

Input Bias Current

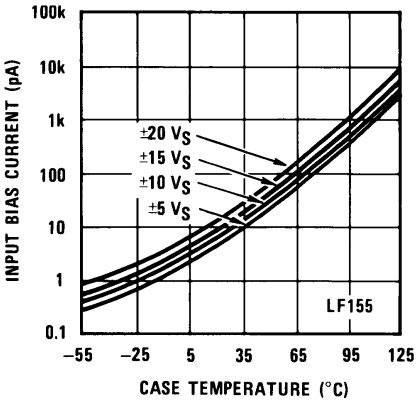


Figure 2.

Input Bias Current

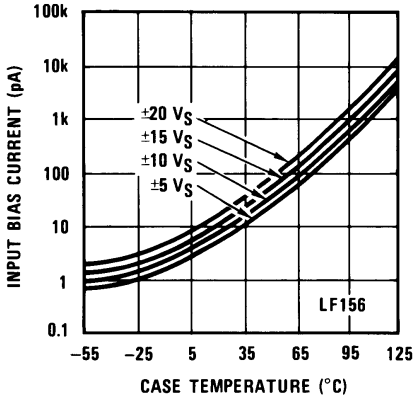


Figure 3.

Input Bias Current

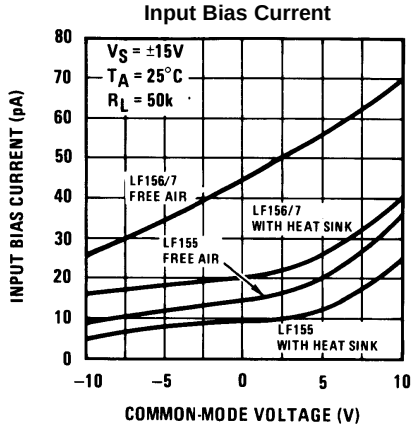


Figure 4.

Voltage Swing

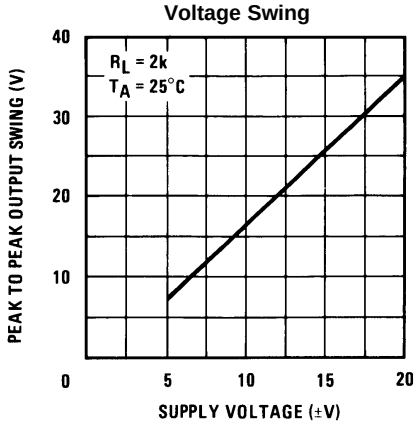


Figure 5.

Supply Current

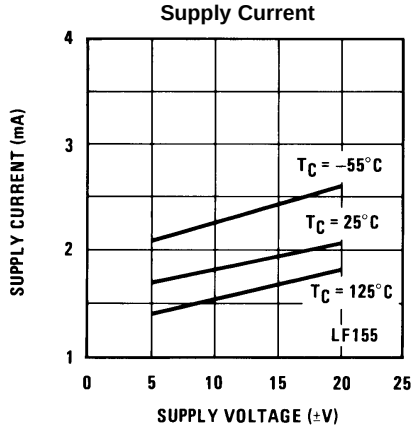


Figure 6.

Supply Current

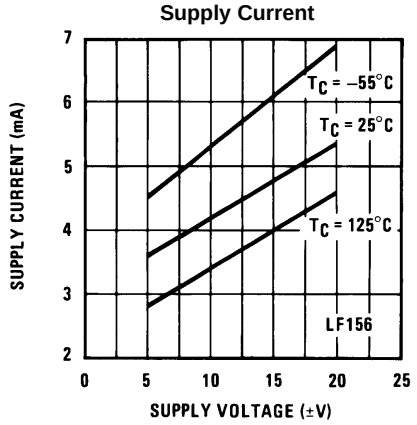


Figure 7.

Typical DC Performance Characteristics (continued)

Negative Current Limit

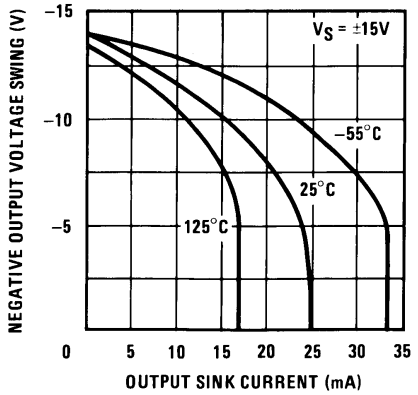


Figure 8.

Positive Current Limit

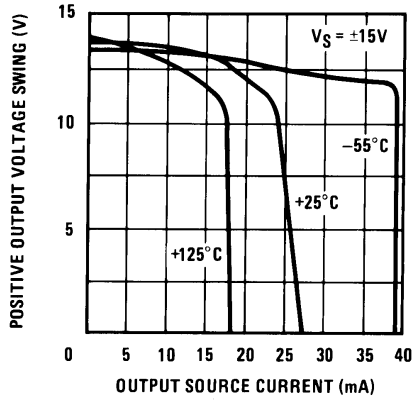


Figure 9.

Positive Common-Mode Input Voltage Limit

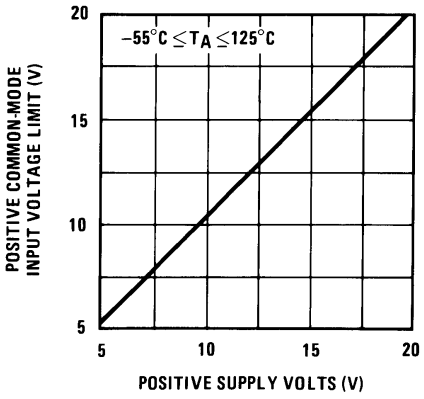


Figure 10.

Negative Common-Mode Input Voltage Limit

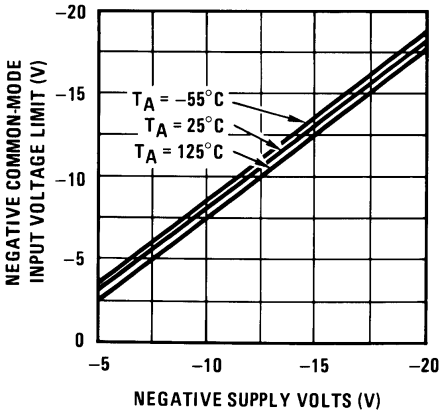


Figure 11.

Open Loop Voltage Gain

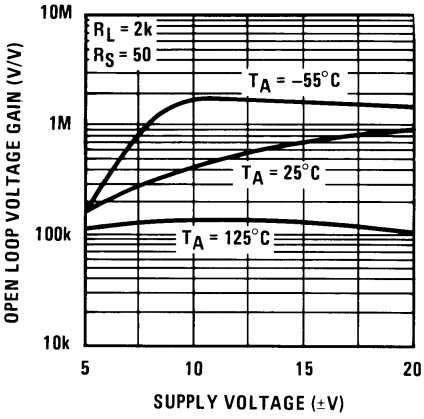


Figure 12.

Output Voltage Swing

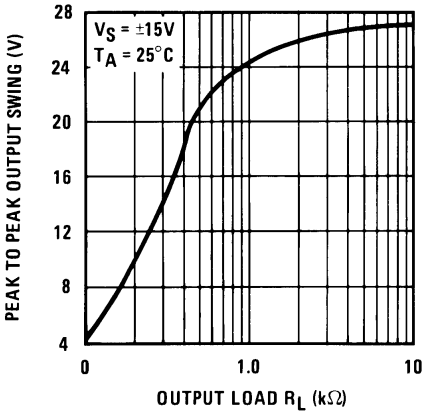


Figure 13.

Typical AC Performance Characteristics

Gain Bandwidth

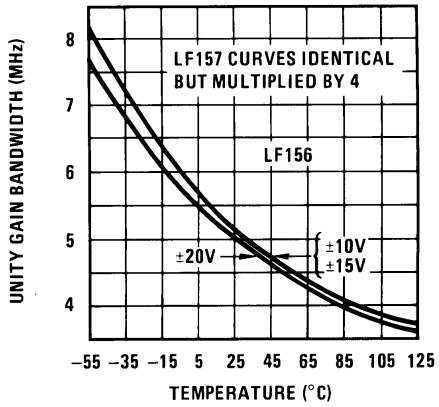


Figure 14.

Normalized Slew Rate

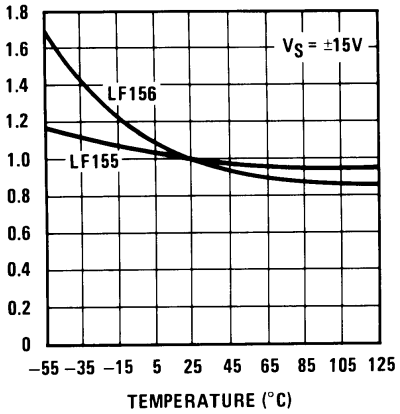


Figure 15.

Output Impedance

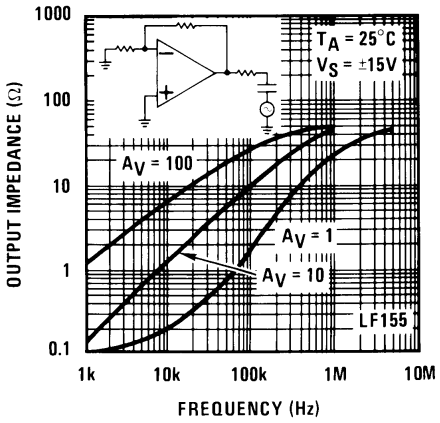


Figure 16.

Output Impedance

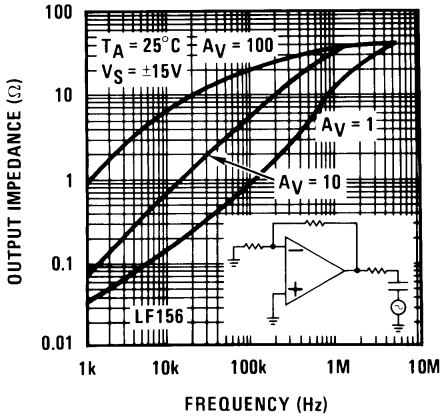


Figure 17.

LF156 Small Signal Pulse Response, A_V = +1

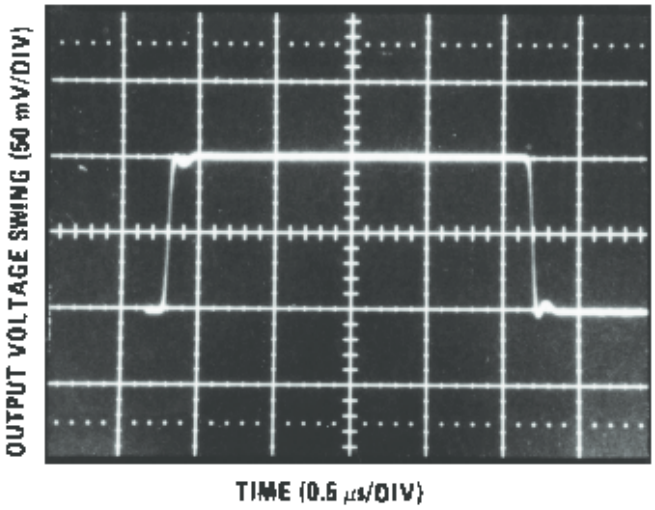


Figure 18.

LF156 Large Signal Puls Response, A_V = +1

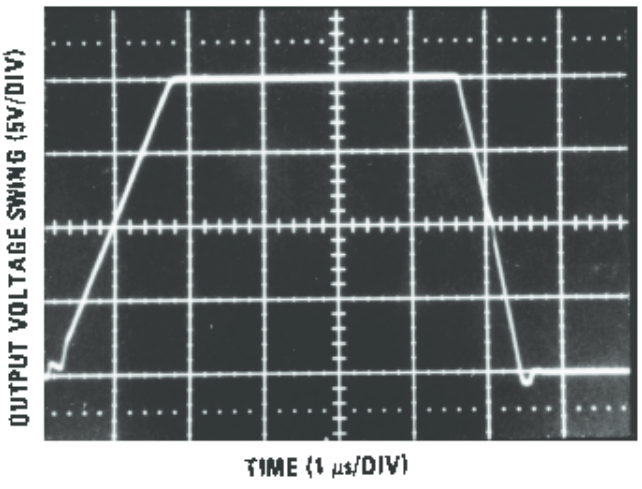


Figure 19.

Typical AC Performance Characteristics (continued)

Inverter Settling Time

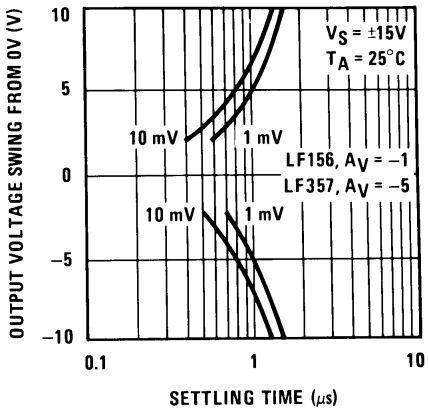


Figure 20.

Open Loop Frequency Response

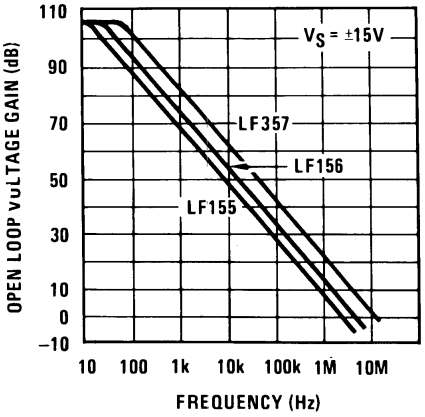


Figure 21.

Bode Plot

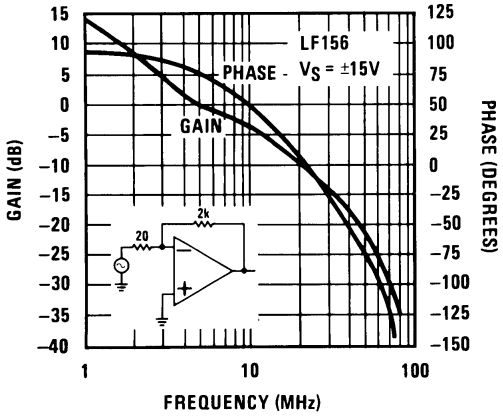


Figure 22.

Common-Mode Rejection Ratio

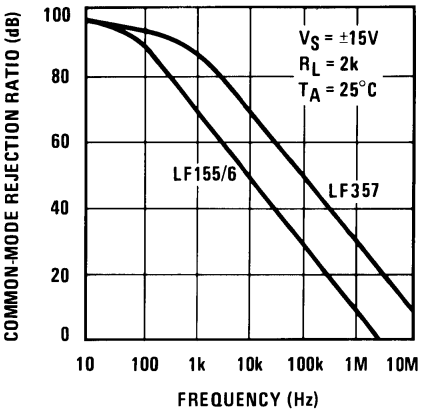


Figure 23.

Power Supply Rejection Ratio

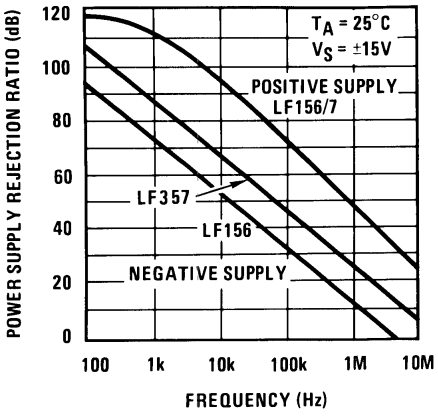


Figure 24.

Undistorted Output Voltage Swing

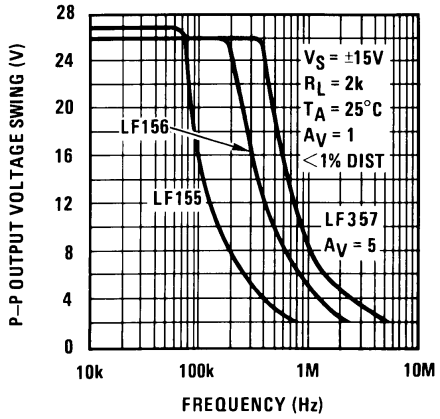


Figure 25.

Typical AC Performance Characteristics (continued)

Equivalent Input Noise Voltage

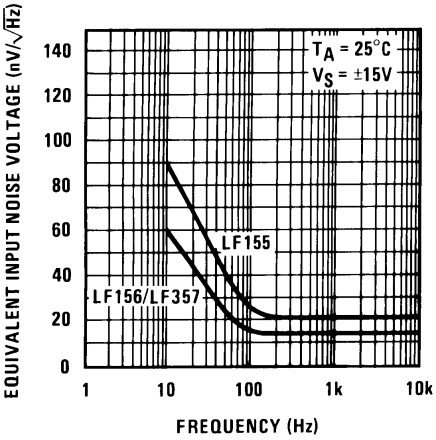


Figure 26.

Equivalent Input Noise Voltage (Expanded Scale)

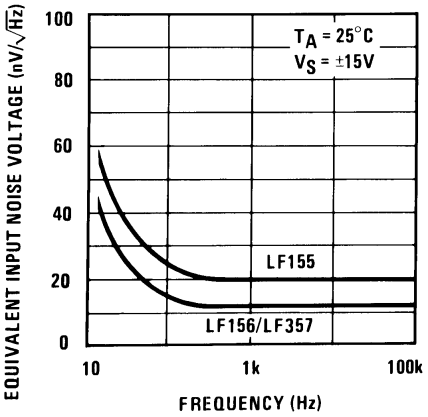


Figure 27.

APPLICATION HINTS

These are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pickup” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Circuit Connections

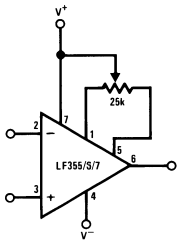


Figure 28. V_{OS} Adjustment

- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V^+
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is ≈ 0.5µV/°C/mV of adjustment
- Typical overall drift: 5µV/°C ±(0.5µV/°C/mV of adj.)

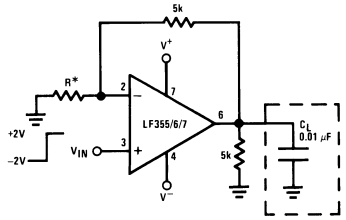


Figure 29. Driving Capacitive Loads

***** LF156 R = 5k
Due to a unique output stage design, these amplifiers have the ability to drive large capacitive loads and still maintain stability. $C_{L(MAX)} \approx 0.01\mu F$.
Overshoot ≤ 20%
Settling time (t_S) ≈ 5µs

Typical Applications

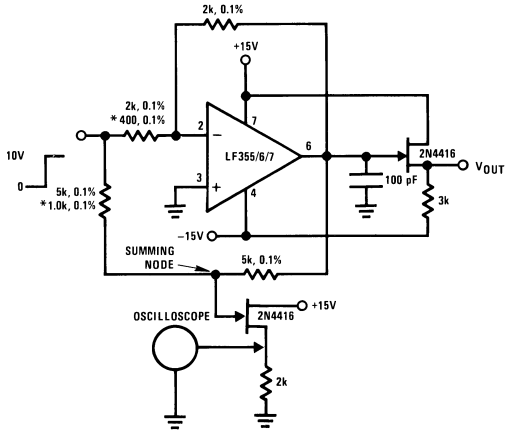


Figure 30. Settling Time Test Circuit

- Settling time is tested with the LF156 connected as unity gain inverter.
- FET used to isolate the probe capacitance
- Output = 10V step

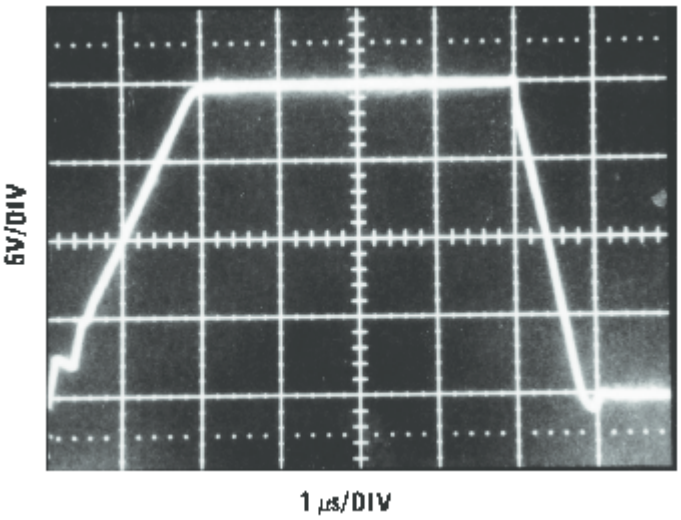


Figure 31. Large Signal Inverter Output, V_{OUT} (from Settling Time Circuit) LF356

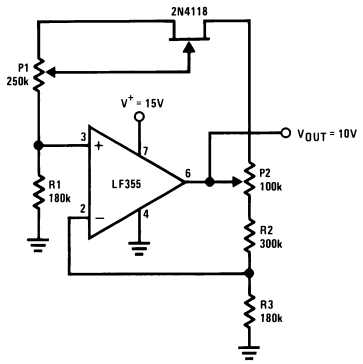


Figure 32. Low Drift Adjustable Voltage Reference

- $\Delta V_{OUT}/\Delta T = \pm 0.002\%/°C$
- All resistors and potentiometers should be wire-wound
- P1: drift adjust
- P2: V_{OUT} adjust

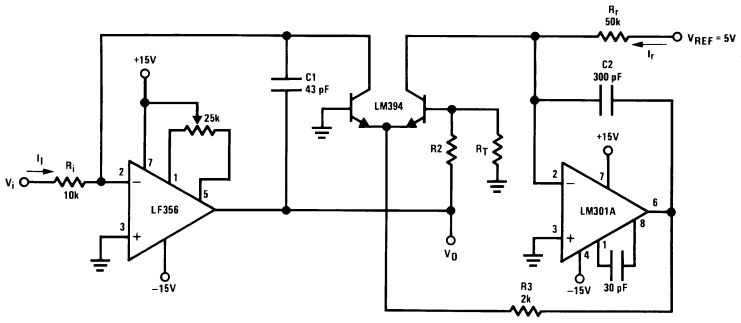


Figure 33. Fast Logarithmic Converter

- Dynamic range: $100\mu A \le I_i \le 1mA$ (5 decades), $|V_O| = 1V$/decade
- Transient response: 3µs for ΔI_i = 1 decade

- C1, C2, R2, R3: added dynamic compensation
- V_{OS} adjust the LF156 to minimize quiescent error
- R_T: Tel Labs type Q81 + 0.3%/°C

$$|V_{OUT}| = \left[1 + \frac{R2}{R_T}\right] \frac{kT}{q} \text{ in } V_i \left[\frac{R_r}{V_{REF}\, Ri}\right] = \log V_i \frac{1}{R_i I_r} \quad R2 = 15.7k,\ R_T = 1k,\ 0.3\%/°C \text{ (for temperature compensation)} \tag{1}$$

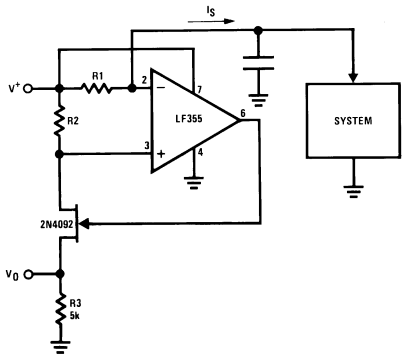


Figure 34. Precision Current Monitor

- V_O = 5 R1/R2 (V/mA of I_S)
- R1, R2, R3: 0.1% resistors

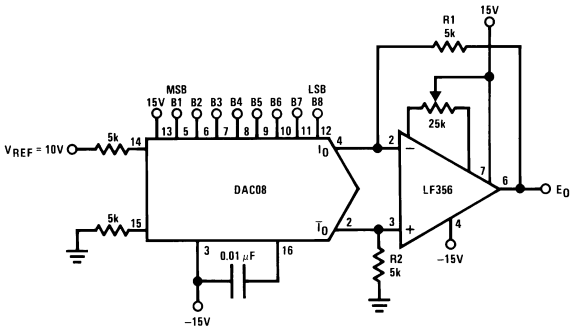
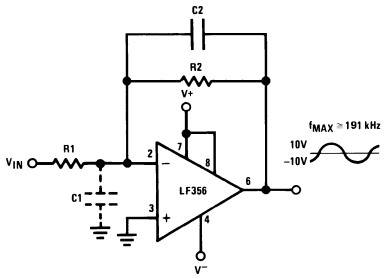


Figure 35. 8-Bit D/A Converter with Symmetrical Offset Binary Operation

- R1, R2 should be matched within ±0.05%
- Full-scale response time: 3µs

E_O	B1	B2	B3	B4	B5	B6	B7	B8	Comments
+9.920	1	1	1	1	1	1	1	1	Positive Full-Scale
+0.040	1	0	0	0	0	0	0	0	(+) Zero-Scale
−0.040	0	1	1	1	1	1	1	1	(−) Zero-Scale
−9.920	0	0	0	0	0	0	0	0	Negative Full-Scale



- Power BW: $f_{MAX} = \frac{S_r}{2\pi V_P} \cong 191\,kHz$

Figure 36. Wide BW Low Noise, Low Drift Amplifier

- Parasitic input capacitance C1 ≃ 3pF interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: R2 C2 ≃ R1 C1.

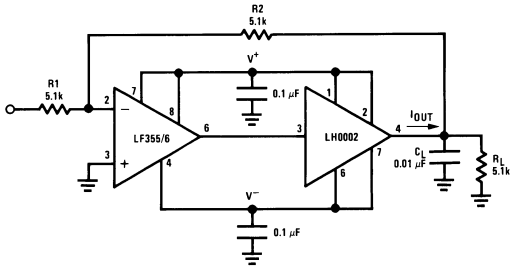
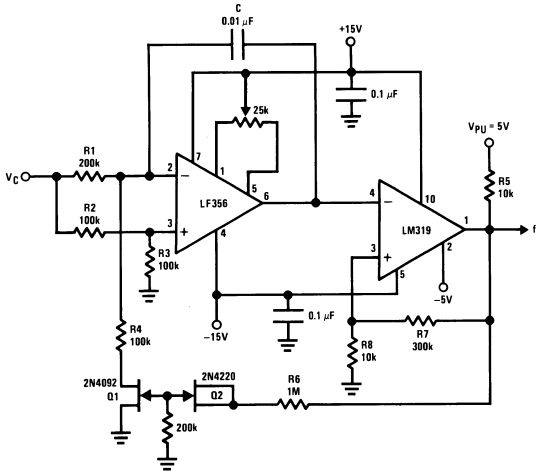


Figure 37. Boosting the LF156 with a Current Amplifier

- $I_{OUT(MAX)} \simeq 150mA$ (will drive $R_L \geq 100\Omega$)
- $\frac{\Delta V_{OUT}}{\Delta T} = \frac{0.15}{10^{-2}}\ V/\mu s$ (with C_L shown)
- No additional phase shift added by the current amplifier



$$f = \frac{V_C\,(R8 + R7)}{(8\ V_{PU}\ R8\ R1)\ C'} \quad 0 \leq V_C \leq 30V,\ 10\,Hz \leq f \leq 10\,kHz$$

R1, R4 matched. Linearity 0.1% over 2 decades.

Figure 38. 3 Decades VCO

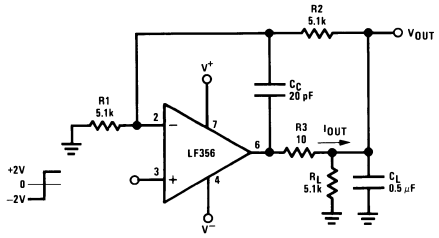


Figure 39. Isolating Large Capacitive Loads

- Overshoot 6%
- t_s 10μs
- When driving large C_L, the V_{OUT} slew rate determined by C_L and $I_{OUT(MAX)}$:

$$\frac{\Delta V_{OUT}}{\Delta T} = \frac{I_{OUT}}{C_L} \cong \frac{0.02}{0.5}\ V/\mu s = 0.04\ V/\mu s \text{ (with } C_L \text{ shown)} \quad (2)$$

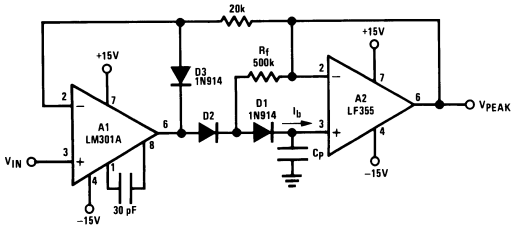
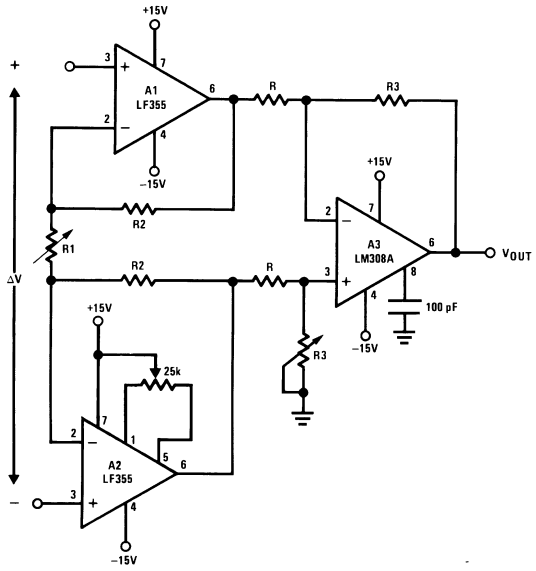


Figure 40. Low Drift Peak Detector

- By adding D1 and R_f, V_{D1}=0 during hold mode. Leakage of D2 provided by feedback path through R_f.
- Leakage of circuit is essentially I_b plus capacitor leakage of Cp.
- Diode D3 clamps V_{OUT} (A1) to $V_{IN}-V_{D3}$ to improve speed and to limit reverse bias of D2.
- Maximum input frequency should be << $\frac{1}{2}\pi R_f C_{D2}$ where C_{D2} is the shunt capacitance of D2.



- $V_{OUT} = \frac{R3}{R}\left[\frac{2R2}{R1} + 1\right]\Delta V$, $V^- + 2V \leq V_{IN}$ common-mode $\leq V^+$

Figure 41. High Impedance, Low Drift Instrumentation Amplifier

- System V_{OS} adjusted via A2 V_{OS} adjust

- Trim R3 to boost up CMRR to 120 dB. Instrumentation amplifier resistor array recommended for best accuracy and lowest drift

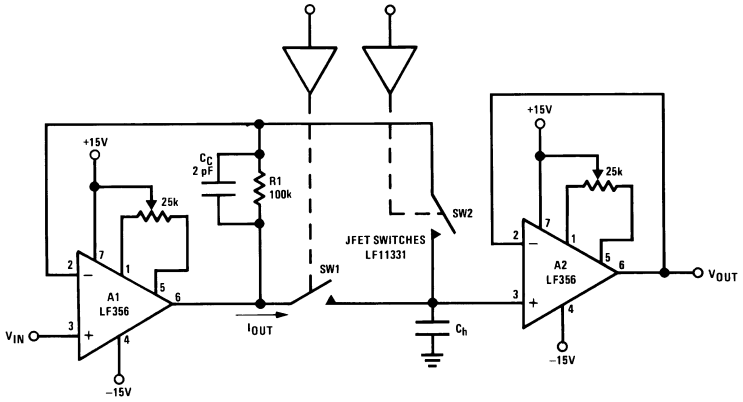


Figure 42. Fast Sample and Hold

- Both amplifiers (A1, A2) have feedback loops individually closed with stable responses (overshoot negligible)
- Acquisition time T_A, estimated by:

$$T_A \cong \left[\frac{2R_{ON},\ V_{IN},\ C_h}{S_r}\right] \text{ 1/2 provided that:}$$

$$V_{IN} < 2\pi S_r\, R_{ON} C_h \text{ and } T_A > \frac{V_{IN} C_h}{I_{OUT(MAX)}},\ R_{ON} \text{ is of SW1}$$

$$\text{If inequality not satisfied: } T_A \cong \frac{V_{IN} C_h}{20\ mA} \tag{3}$$

- LF156 develops full S_r output capability for $V_{IN} \geq 1V$
- Addition of SW2 improves accuracy by putting the voltage drop across SW1 inside the feedback loop
- Overall accuracy of system determined by the accuracy of both amplifiers, A1 and A2

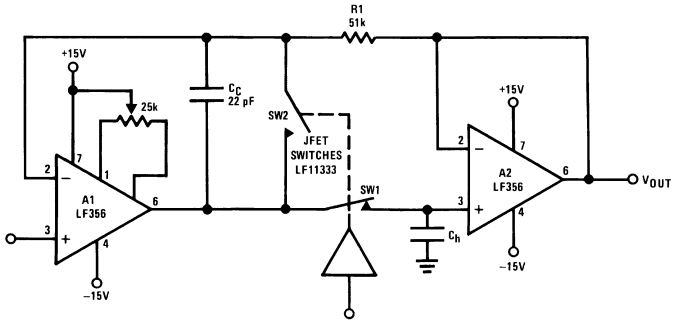


Figure 43. High Accuracy Sample and Hold

- By closing the loop through A2, the V_{OUT} accuracy will be determined uniquely by A1.
  - No V_{OS} adjust required for A2.
- T_A can be estimated by same considerations as previously but, because of the added
  - propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold
- R1, C_C: additional compensation
- Use LF156 for
  - Fast settling time
  - Low V_{OS}

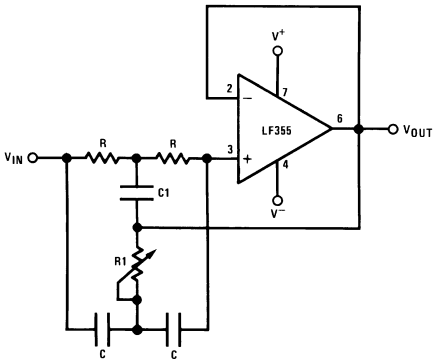


Figure 44. High Q Notch Filter

- 2R1 = R = 10MΩ
  - 2C = C1 = 300pF
- Capacitors should be matched to obtain high Q
- f_{NOTCH} = 120 Hz, notch = −55 dB, Q > 100
- Use LF155 for
  - Low I_B
  - Low supply current

REVISION HISTORY

Date Released	Revision	Section	Originator	Changes
03/10/06	A	New Released, Corporate format.	R. Malone	New Release, Corporate format 1 MDS data sheet converted into a Corp. data sheet format. Following MDS data sheet will be Archived MJLF156-X, Rev. 0A0.
03/25/13	A	All	-	Changed layout of National Data Sheet to TI format.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
JL156BGA	ACTIVE	TO-99	LMC	8	20	TBD	Call TI	Call TI	-55 to 125	JL156BGA JM38510/11402BGA Q ACO JM38510/11402BGA Q >T	Samples
JM38510/11402BGA	ACTIVE	TO-99	LMC	8	20	TBD	Call TI	Call TI	-55 to 125	JL156BGA JM38510/11402BGA Q ACO JM38510/11402BGA Q >T	Samples
M38510/11402BGA	ACTIVE	TO-99	LMC	8	20	TBD	Call TI	Call TI	-55 to 125	JL156BGA JM38510/11402BGA Q ACO JM38510/11402BGA Q >T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

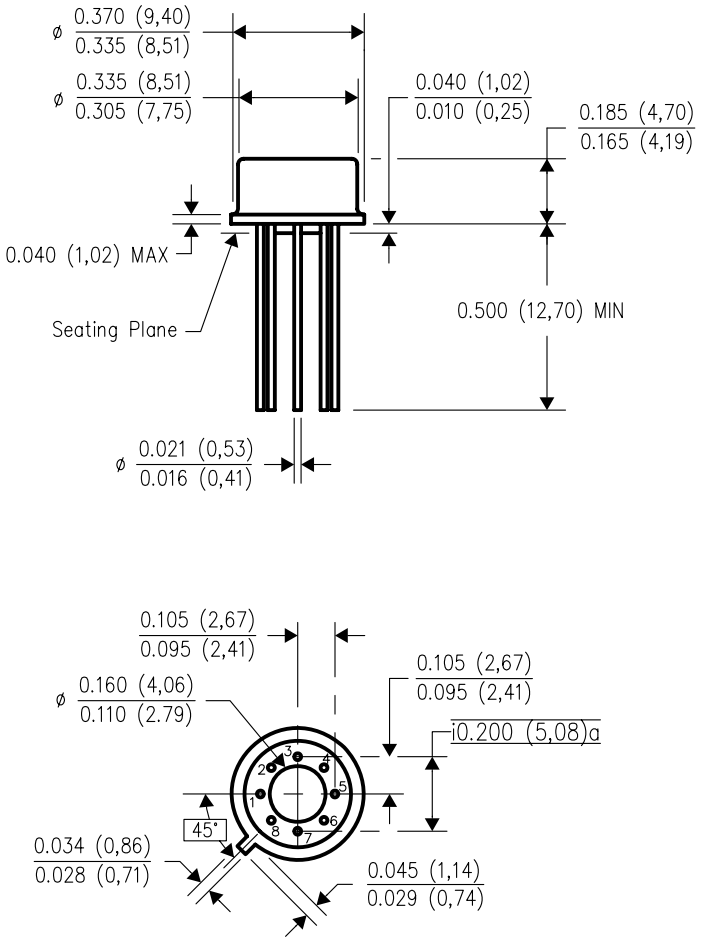
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

LMC (O–MBCY–W8) METAL CYLINDRICAL PACKAGE



4202483/B 09/07

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
D. Pin numbers shown for reference only. Numbers may not be marked on package.
E. Falls within JEDEC MO–002/TO–99.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265