

LM555JAN Timer

Check for Samples: [LM555JAN](#)

FEATURES

- Direct Replacement for SE555/NE555
- Timing from Microseconds Through Hours
- Operates in both Astable and Monostable Modes
- Adjustable Duty Cycle
- Output can Source or Sink 200 mA
- Output and Supply TTL Compatible
- Temperature Stability Better than 0.005% per °C
- Normally On and Normally Off Output

APPLICATIONS

- Precision Timing
- Pulse Generation
- Sequential Timing
- Time Delay Generation
- Pulse Width Modulation
- Pulse Position Modulation
- Linear Ramp Generator

DESCRIPTION

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200mA or drive TTL circuits.

Connection Diagram

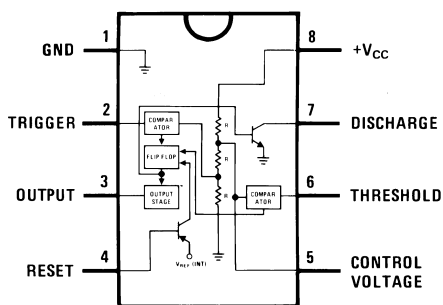


Figure 1. 8-Pin CDIP - Top View
See NAB0008A Package

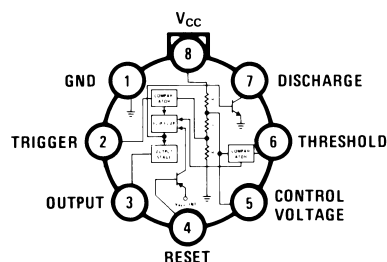


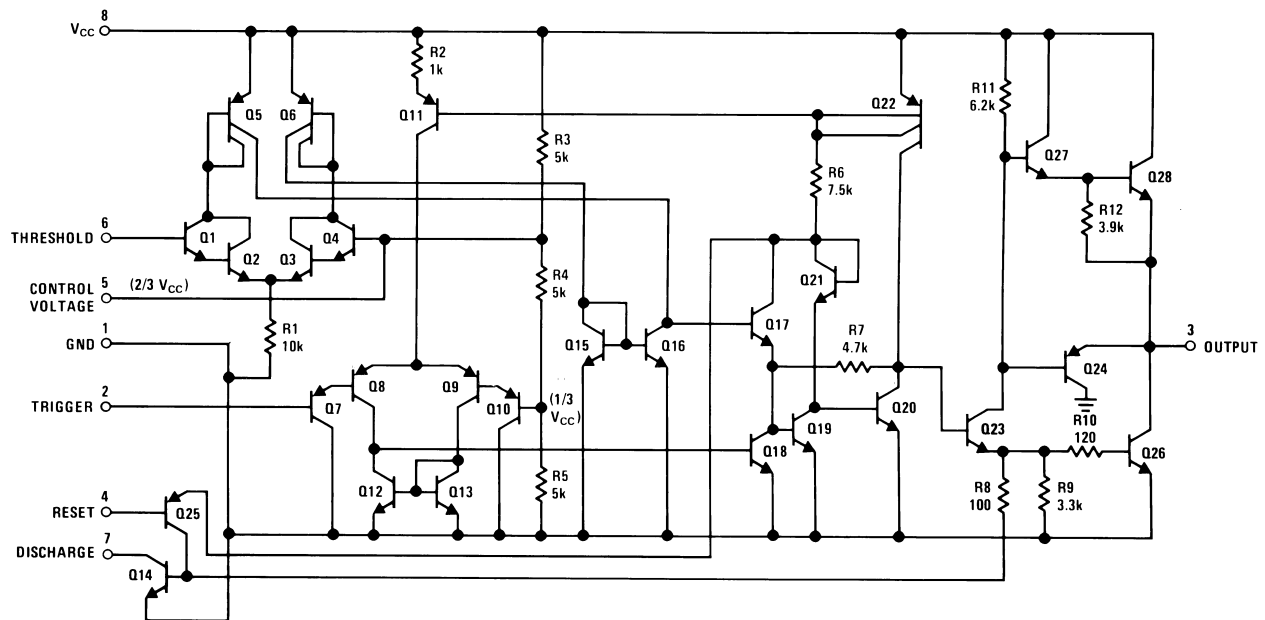
Figure 2. 8-Pin SDIP - Top View
See NEV0008A Package



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Schematic Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾

Supply Voltage		+18V	
Discharge Current		+200mA	
Output Sink Current		+200mA	
Output Source Current		-200mA	
Power Dissipation ⁽²⁾	SDIP	300mW @ +125°C	
	CDIP	370mW @ +125°C	
Operating Temperature Range		-55°C ≤ T _A ≤ +125°C	
Maximum Junction Temperature (T _{Jmax})		+175°C	
Storage Temperature Range		-65°C ≤ T _A ≤ +150°C	
Soldering Information (Soldering 10 Seconds)		300°C	
Thermal Resistance	θ _{JA}	CDIP Still Air	123°C/W
		CDIP 500LF / Min Air Flow	69°C/W
		SDIP Still Air	171°C/W
		SDIP 500LF / Min Air Flow	92°C/W
	θ _{JC}	CDIP	18°C/W
		SDIP	41°C/W
ESD Tolerance ⁽³⁾		1KV	

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- (2) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is P_{Dmax} = (T_{Jmax} - T_A)/θ_{JA} or the number given in the Absolute Maximum Ratings, whichever is lower.
- (3) Human body model, 1.5KΩ in series with 100pF.

Recommended Operating Conditions

Supply Voltage Range	+4.5V to +16V _{DC}
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Table 1. Quality Conformance Inspection Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp °C
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55
12	Settling time at	25
13	Settling time at	125
14	Settling time at	-55

Electrical Characteristics DC Parameters

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
I _{CC}	Power Supply Current	V _{CC} = 4.5V			5.0	mA	1, 2, 3
		V _{CC} = 16.5V			20	mA	1, 2, 3
V _{Trig}	Trigger Voltage	V _{CC} = 4.5V		1.3	1.8	V	1
				1.3	2.1	V	2
				1.15	1.8	V	3
		V _{CC} = 16.5V		5.2	5.8	V	1
				5.2	6.1	V	2
				5.0	5.8	V	3
I _{Trig}	Trigger Current	V _{CC} = 16.5V		-5.0		μA	1, 2, 3
V _{Th}	Threshold Voltage	V _{CC} = 4.5V		2.7	3.3	V	1
				2.6	3.4	V	2, 3
		V _{CC} = 16.5V		10.7	11.3	V	1
				10.6	11.4	V	2, 3
I _{Th}	Threshold Current	V _{CC} = 16.5V			250	nA	1, 2
					2,500	nA	3
					0	nA	
V _{OL}	Logical "0" Output Voltage	V _{CC} = 4.5V, I _{Sink} = 5mA			0.25	V	1
					0.35	V	2, 3
		V _{CC} = 4.5V, I _{Sink} = 50mA			2.2	V	1, 2
					2.6	V	3
		V _{CC} = 16.5V, I _{Sink} = 10mA			0.15	V	1, 3
					0.25	V	2
		V _{CC} = 16.5V, I _{Sink} = 50mA			0.5	V	1, 3
					0.7	V	2
		V _{CC} = 16.5V, I _{Sink} = 100mA			2.2	V	1
					2.8	V	2, 3
V _{OH}	Logical "1" Output Voltage	V _{CC} = 4.5V, I _{Source} = -100mA		2.6		V	1, 2
				2.2		V	3
		V _{CC} = 16.5V, I _{Source} = -100mA		14.6		V	1, 2
				14		V	3
I _{CEX}	Discharge Transistor Leakage Current	V _{CC} = 16.5V			100	nA	1, 3
					3,000	nA	2
V _{Sat}	Discharge Transistor Saturation Voltage	V _{CC} = 16.5V			0.8	V	1, 3
					1.0	V	2
V _R	Reset Voltage	V _{CC} = 16.5V	See ⁽¹⁾⁽²⁾	0.1	1.3	V	1, 2, 3
I _R	Reset Current	V _{CC} = 16.5V		-1.6		mA	1, 2, 3

(1) Parameter tested go-no-go, only.

(2) Datalog reading of 0.7V will reflect the Reset Voltage levels passing and a reading of 0.5V or 1.5V reflects the Reset voltage levels failing the low level or high level respectfully.

Electrical Characteristics AC Parameters

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
t_{PLH}	Propagation Delay Time	$V_{CC} = 4.5V$			800	nS	9, 11
					900	nS	10
		$V_{CC} = 16.5V$			800	nS	9, 11
					900	nS	10
t_{PHL}	Propagation Delay Time	$V_{CC} = 4.5V$			12	μS	9, 10, 11
		$V_{CC} = 16.5V$			12	μS	9, 10, 11
t_{TLH}	Transition Time	$V_{CC} = 4.5V$			300	nS	9, 10, 11
		$V_{CC} = 16.5V$			300	nS	9, 10, 11
t_{THL}	Transition Time	$V_{CC} = 4.5V$			300	nS	9, 10, 11
		$V_{CC} = 16.5V$			300	nS	9, 10, 11
t_{DOH}	Time Delay Output High $R_T = 1K\Omega$	$V_{CC} = 4.5V$		106.7	113.3	μS	9, 10, 11
		$V_{CC} = 16.5V$		106.7	113.3	μS	9, 10, 11
	Time Delay Output High $R_T = 100K\Omega$	$V_{CC} = 4.5V$		10.67	11.33	mS	9, 10, 11
		$V_{CC} = 16.5V$		10.67	11.33	mS	9, 10, 11
$\Delta t_D / \Delta V_{CC}$	Drift In Time Delay	$\Delta V_{CC} = 12,$ $V_{CC} = 4.5V$ to $16.5V$	See ⁽¹⁾	-220	220	nS/V	9
$\Delta t_D / \Delta T$	Temperature Coefficient of Time Delay	$V_{CC} = 16.5V$		-11	11	nS/ $^{\circ}C$	10, 11
t_{Ch}	Capacitor Charge Time $R_T = 1K\Omega$	$V_{CC} = 4.5V$		120	156	μS	9, 10, 11
		$V_{CC} = 16.5V$		120	156	μS	9, 10, 11
	Capacitor Charge Time $R_T = 100K\Omega$	$V_{CC} = 4.5V$		11.3	15	mS	9, 10, 11
		$V_{CC} = 16.5V$		11.3	15	mS	9, 10, 11
t_{Dis}	Capacitor Discharge Time $R_T = 1K\Omega$	$V_{CC} = 4.5V$		57.5	80	μS	9, 10, 11
		$V_{CC} = 16.5V$		57.5	80	μS	9, 10, 11
	Capacitor Discharge Time $R_T = 100K\Omega$	$V_{CC} = 4.5V$		5.4	7.7	mS	9, 10, 11
		$V_{CC} = 16.5V$		5.4	7.7	mS	9, 10, 11
$\Delta t_{Ch} / \Delta V_{CC}$	Drift In Capacitor Charge Time	$\Delta V_{CC} = 12,$ $V_{CC} = 4.5V$ to $16.5V$		-820	820	nS/V	9
$\Delta t_{Ch} / \Delta T$	Temperature Coefficient Capacitor Charge Time	$V_{CC} = 16.5V$	See ⁽¹⁾	-68	68	nS/ $^{\circ}C$	10, 11
t_{Res}	Reset Time	$V_{CC} = 16.5V$			1.5	μS	9, 11
					2.0	μS	10

(1) Calculated parameter.

Electrical Characteristics DC Drift Parameters

Delta calculations performed on JAN S devices at Group B, Subgroup 5, only.

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{Trig}	Trigger Voltage	$V_{CC} = 16.5V$		-0.05	0.05	V	1
V_{Th}	Threshold Voltage	$V_{CC} = 16.5V$		-0.05	0.05	V	1
V_{OL}	Logical "0" Output Voltage	$V_{CC} = 16.5V, I_{Sink} = 10mA$		-0.05	0.05	V	1
I_{CEX}	Discharge Transistor Leakage Current	$V_{CC} = 16.5V$		-50	50	nA	1

Typical Performance Characteristics

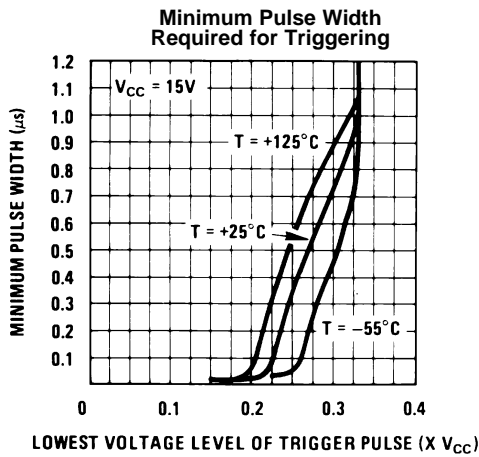


Figure 3.

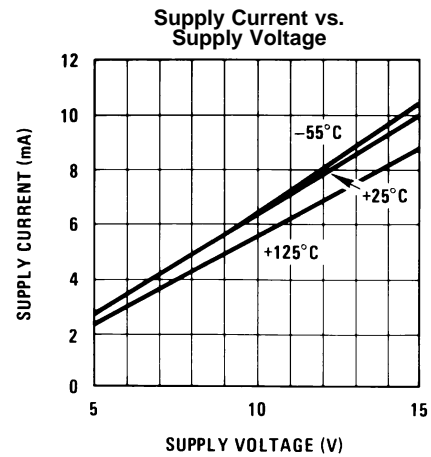


Figure 4.

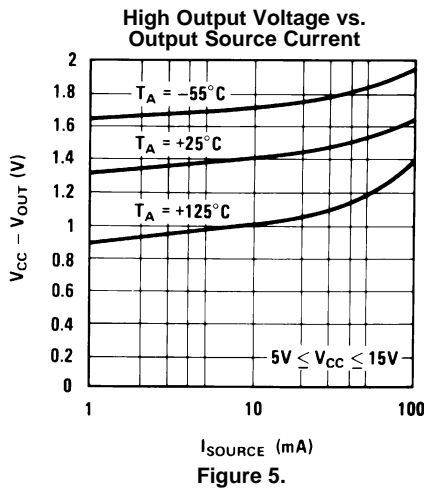


Figure 5.

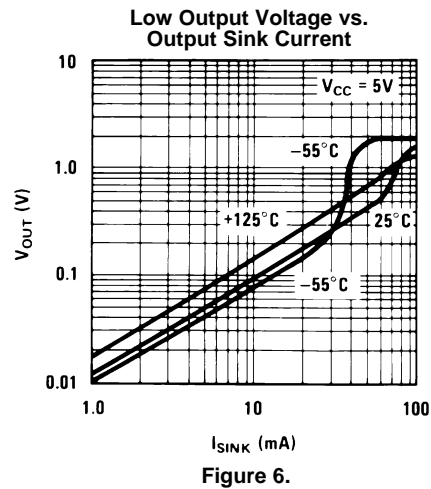


Figure 6.

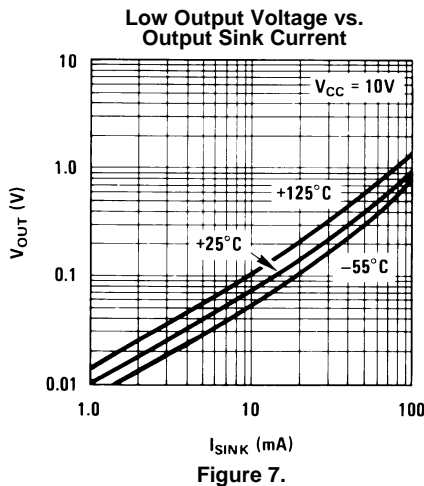


Figure 7.

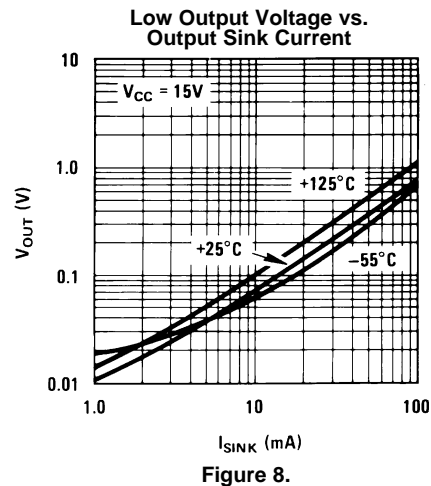


Figure 8.

Typical Performance Characteristics (continued)

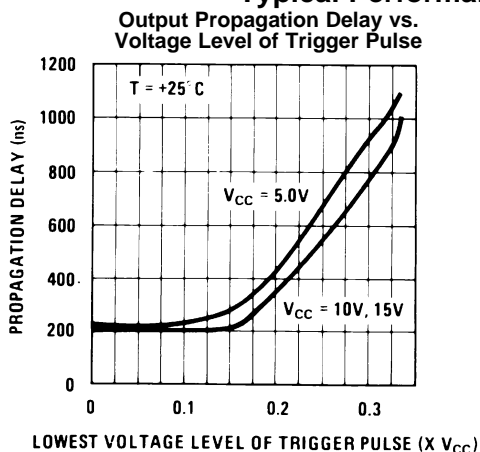


Figure 9.

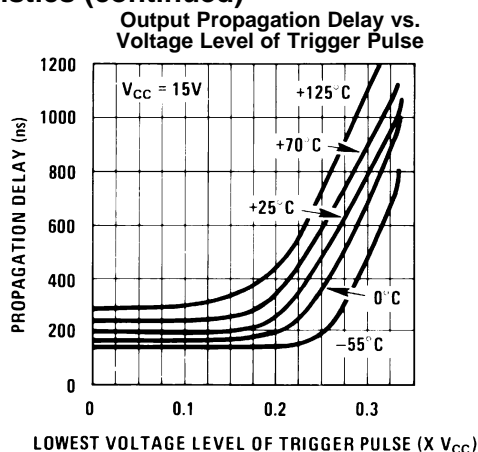


Figure 10.

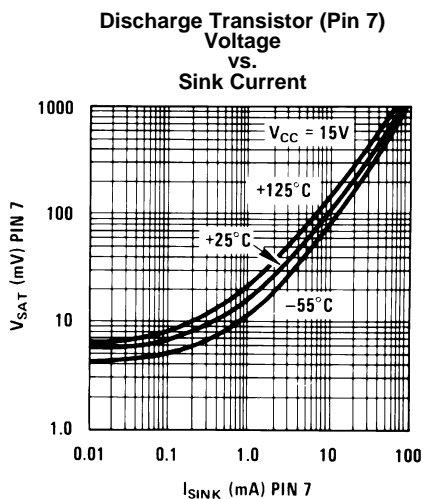


Figure 11.

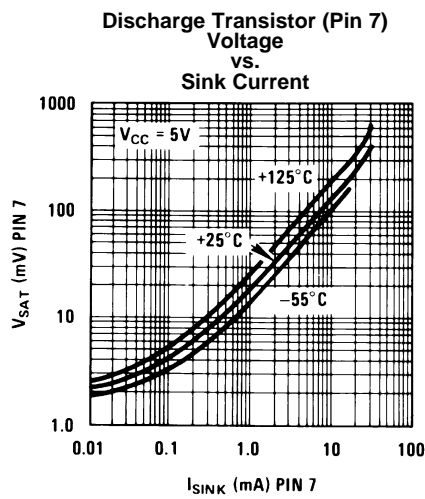


Figure 12.

APPLICATIONS INFORMATION

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot (Figure 13). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than $1/3 V_{CC}$ to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

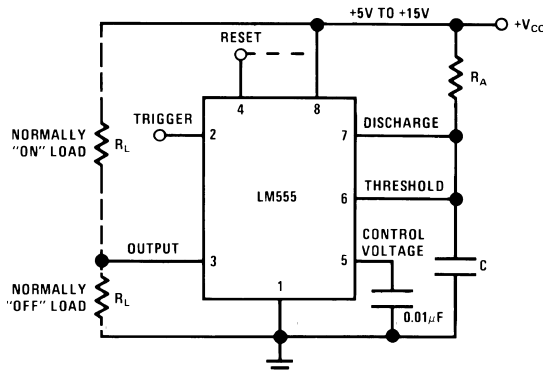
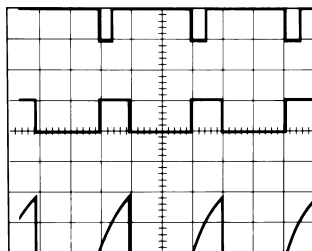


Figure 13. Monostable

The voltage across the capacitor then increases exponentially for a period of $t = 1.1 R_A C$, at the end of which time the voltage equals $2/3 V_{CC}$. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. Figure 14 shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply.



$V_{CC} = 5V$
 TIME = 0.1 ms/DIV.
 $R_A = 9.1k\Omega$
 $C = 0.01\mu F$

Top Trace: Input 5V/Div.
 Middle Trace: Output 5V/Div.
 Bottom Trace: Capacitor Voltage 2V/Div.

Figure 14. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least $10\mu s$ before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 15 is a nomogram for easy determination of R, C values for various time delays.

NOTE: In monostable operation, the trigger should be driven high before the end of timing cycle.

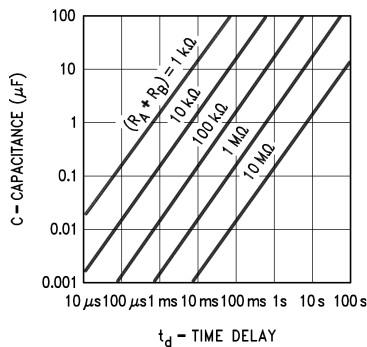


Figure 15. Time Delay

ASTABLE OPERATION

If the circuit is connected as shown in [Figure 16](#) (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through $R_A + R_B$ and discharges through R_B . Thus the duty cycle may be precisely set by the ratio of these two resistors.

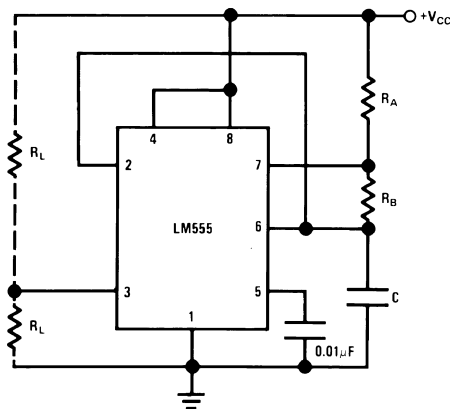
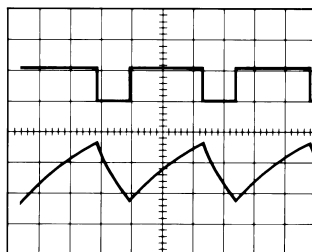


Figure 16. Astable

In this mode of operation, the capacitor charges and discharges between $1/3 V_{CC}$ and $2/3 V_{CC}$. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

[Figure 17](#) shows the waveforms generated in this mode of operation.



$V_{CC} = 5V$
 TIME = 20μs/DIV.
 $R_A = 3.9k\Omega$
 $R_B = 3k\Omega$
 $C = 0.01\mu F$

Top Trace: Output 5V/Div.
 Bottom Trace: Capacitor Voltage 1V/Div.

Figure 17. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693 (R_A + R_B) C \tag{1}$$

And the discharge time (output low) by:

$$t_2 = 0.693 (R_B) C \tag{2}$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693 (R_A + 2R_B) C \tag{3}$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B) C} \tag{4}$$

Figure 18 may be used for quick determination of these RC values.

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B} \tag{5}$$

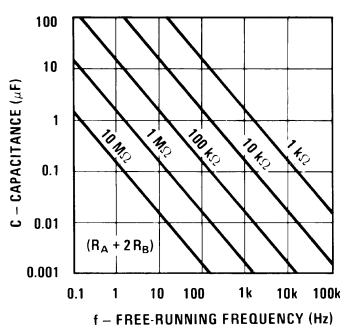
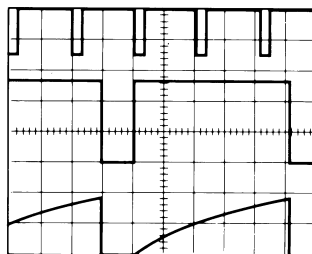


Figure 18. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of Figure 13 can be used as a frequency divider by adjusting the length of the timing cycle. Figure 19 shows the waveforms generated in a divide by three circuit.



$V_{CC} = 5V$
 $TIME = 20\mu s/DIV.$
 $R_A = 9.1k\Omega$
 $C = 0.01\mu F$

Top Trace: Input 4V/Div.
 Middle Trace: Output 2V/Div.
 Bottom Trace: Capacitor 2V/Div.

Figure 19. Frequency Divider

PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. Figure 20 shows the circuit, and in Figure 21 are some waveform examples.

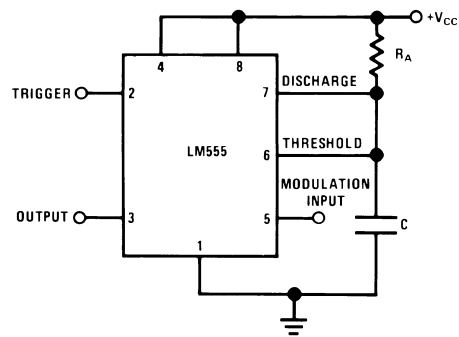
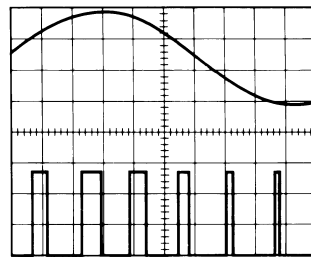


Figure 20. Pulse Width Modulator



$V_{CC} = 5V$ Top Trace: Modulation 1V/Div.
 TIME = 0.2 ms/DIV. Bottom Trace: Output Voltage 2V/Div.
 $R_A = 9.1k\Omega$
 $C = 0.01\mu F$

Figure 21. Pulse Width Modulator

PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in [Figure 22](#), with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. [Figure 23](#) shows the waveforms generated for a triangle wave modulation signal.

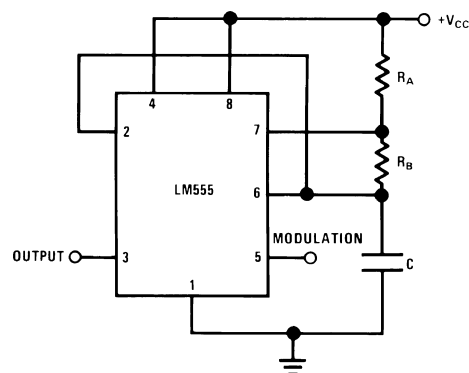
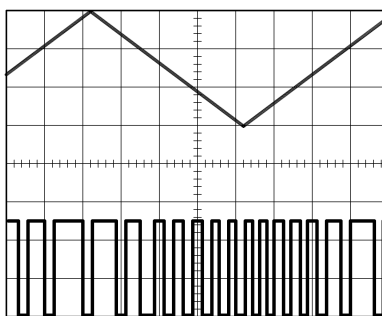


Figure 22. Pulse Position Modulator



$V_{CC} = 5V$
 TIME = 0.1 ms/DIV. Top Trace: Modulation Input 1V/Div.
 Bottom Trace: Output 2V/Div.
 $R_A = 3.9k\Omega$
 $R_B = 3k\Omega$
 $C = 0.01\mu F$

Figure 23. Pulse Position Modulator

LINEAR RAMP

When the pull-up resistor, R_A , in the monostable circuit is replaced by a constant current source, a linear ramp is generated. Figure 24 shows a circuit configuration that will perform this function.

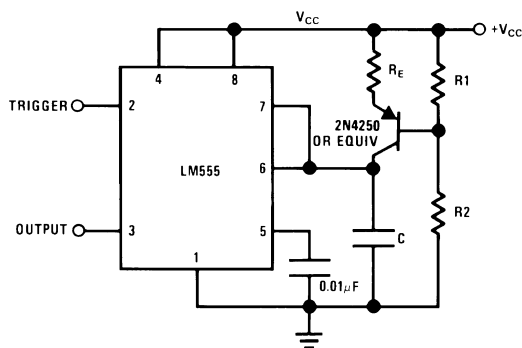


Figure 24.

Figure 25 shows waveforms generated by the linear ramp.

The time interval is given by:

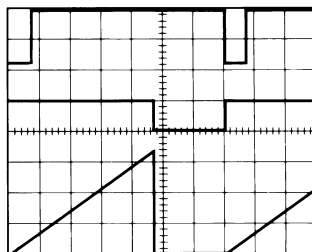
$$T = \frac{2/3 V_{CC} R_E (R_1 + R_2) C}{R_1 V_{CC} - V_{BE} (R_1 + R_2)}$$

$$V_{BE} \approx 0.6V$$

(6)

$$V_{BE} \approx 0.6V$$

(7)



$V_{CC} = 5V$
 TIME = 20μs/DIV.
 $R_1 = 47k\Omega$
 $R_2 = 100k\Omega$
 $R_E = 2.7 k\Omega$
 $C = 0.01 \mu F$

Top Trace: Input 3V/Div.
 Middle Trace: Output 5V/Div.
 Bottom Trace: Capacitor Voltage 1V/Div.

Figure 25. Linear Ramp

50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle, the resistors R_A and R_B may be connected as in Figure 26. The time period for the output high is the same as previous, $t_1 = 0.693 R_A C$. For the output low it is $t_2 =$

$$\left[(R_A R_B) / (R_A + R_B) \right] C \ln \left[\frac{R_B - 2R_A}{2R_B - R_A} \right] \quad (8)$$

Thus the frequency of oscillation is

$$f = \frac{1}{t_1 + t_2} \quad (9)$$

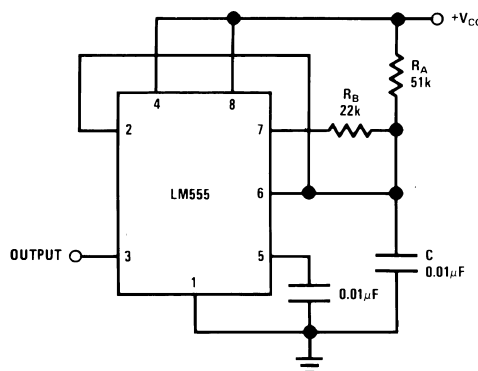


Figure 26. 50% Duty Cycle Oscillator

Note that this circuit will not oscillate if R_B is greater than $1/2 R_A$ because the junction of R_A and R_B cannot bring pin 2 down to $1/3 V_{CC}$ and trigger the lower comparator.

ADDITIONAL INFORMATION

Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is $0.1\mu F$ in parallel with $1\mu F$ electrolytic.

Lower comparator storage time can be as long as $10\mu s$ when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to $10\mu s$ minimum.

Delay time reset to output is $0.47\mu s$ typical. Minimum reset pulse width must be $0.3\mu s$, typical.

Pin 7 current switches within 30ns of the output (pin 3) voltage.

Table 2. Revision History

Date Released	Revision	Section	Changes
08/04/05	A	New Release to corporate format	1 MDS datasheet converted into corporate format. MJLM555-X Rev 1A0 to be archived
07/25/06	B	Applications Information, page 8	Correct a typo in the paragraph after figure 1 (change the word internal to interval) to reflect same change made to Commercial data sheet. Revision A will be Archived.
09/27/2010	C	Obsolete Data Sheet	End Of Life on Product/NSID Sept. 1998
04/11/2013	C		Changed layout of National Data Sheet to TI format.

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