

60-V Common-Mode Bidirectional Precision Current Sensing Amplifier

 Check for Samples: [LMP8601](#), [LMP8601-Q1](#)

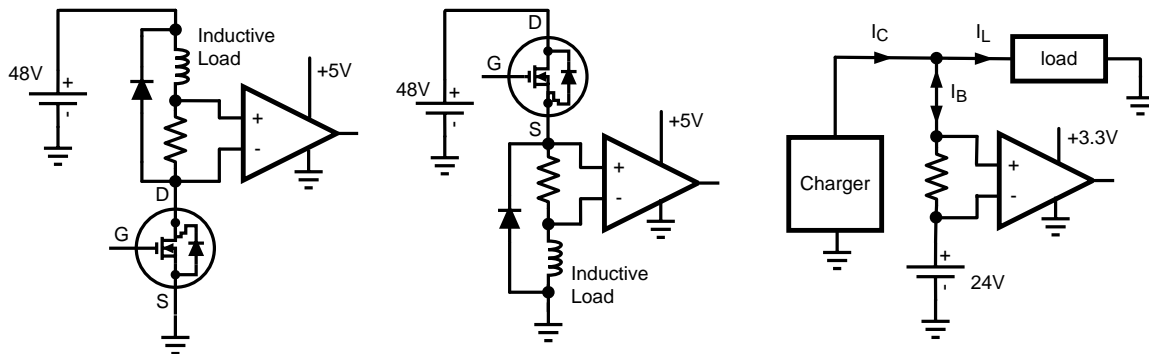
FEATURES

- Unless Otherwise Noted, Typical Values at $T_A = 25^\circ\text{C}$, $V_S = 5.0\text{V}$, Gain = 20x
 - $\text{TCV}_{\text{OS}} 10\mu\text{V}/^\circ\text{C}$ Max
 - **CMRR 90 dB** Min
 - **Input offset voltage 1 mV** Max
 - **CMVR at $V_S = 3.3\text{V}$ -4V to 27V**
 - **CMVR at $V_S = 5.0\text{V}$ -22V to 60V**
 - **Operating Ambient Temperature Range -40°C to 125°C**
 - **LMP8601Q Available in Automotive AEC-Q100 Grade 1 Qualified Version**
 - **Single-Supply Bidirectional Operation**
 - **All Min / Max Limits 100% Tested**

APPLICATIONS

- High-Side and Low-Side Driver Configuration Current Sensing
- Bidirectional Current Measurement
- Current Loop to Voltage Conversion
- Automotive Fuel Injection Control
- Transmission Control
- Power Steering
- Battery Management Systems

Typical Applications



DESCRIPTION

The LMP8601 and LMP8601Q are fixed 20x gain precision amplifiers. The part will amplify and filter small differential signals in the presence of high common mode voltages. The input common mode voltage range is -22V to $+60\text{V}$ when operating from a single 5V supply. With 3.3V supply, the input common mode voltage range is from -4V to $+27\text{V}$. The LMP8601 and LMP8601Q are members of the Linear Monolithic Precision (LMP®) family and are ideal parts for unidirectional and bidirectional current sensing applications. All parameter values of the part that are shown in the tables are 100% tested and all bold values are also 100% tested over temperature.

The part has a precise gain of 20x which is adequate in most targeted applications to drive an ADC to its full scale value. The fixed gain is achieved in two separate stages, a preamplifier with a gain of 10x and an output stage buffer amplifier with a gain of 2x. The connection between the two stages of the signal path is brought out on two pins to enable the possibility to create an additional filter network around the output buffer amplifier. These pins can also be used for alternative configurations with different gain as described in [Application Information](#).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

DESCRIPTION (CONTINUED)

The mid-rail offset adjustment pin enables the user to use these devices for bidirectional single supply voltage current sensing. The output signal is bidirectional and mid-rail referenced when this pin is connected to the positive supply rail. With the offset pin connected to ground, the output signal is unidirectional and ground-referenced.

The LMP8601Q incorporates enhanced manufacturing and support processes for the automotive market, including defect detection methodologies. Reliability qualification is compliant with the requirements and temperature grades defined in the AEC Q100 standard.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾

ESD Tolerance ⁽²⁾ , Human Body	For input pins only	±4000V
	For all other pins	±2000V
Machine Model		200V
Charge Device Model		1000V
Supply Voltage (V_S - GND)		6.0V
Continuous Input Voltage (-IN and +IN)		-22V to 60V
Transient (400 ms)		-25V to 65V
Maximum Voltage at A1, A2, OFFSET and OUT Pins		$V_S + 0.3V$ and GND -0.3V
Storage Temperature Range		-65°C to 150°C
Junction Temperature ⁽³⁾		150°C
Mounting Temperature	Infrared or Convection (20 sec)	235°C
	Wave Soldering Lead (10 sec)	260°C

- (1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of the device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) Human Body Model per MIL-STD-883, Method 3015.7. Machine Model, per JESD22-A115-A. Field-Induced Charge-Device Model, per JESD22-C101-C.
- (3) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{J(MAX)}$, θ_{JA} , and the ambient temperature, T_A . The maximum allowable power dissipation $P_{DMAX} = (T_{J(MAX)} - T_A) / \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower.

Operating Ratings⁽¹⁾

Supply Voltage (V_S - GND)		3.0V to 5.5V
Offset Voltage (Pin 7)		0 to V_S
Temperature Range ⁽²⁾	Packaged devices	-40°C to +125°C
Package Thermal Resistance ⁽²⁾	8-Pin SOIC (θ_{JA})	190°C/W

- (1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of the device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{J(MAX)}$, θ_{JA} , and the ambient temperature, T_A . The maximum allowable power dissipation $P_{DMAX} = (T_{J(MAX)} - T_A) / \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower.

3.3V Electrical Characteristics ⁽¹⁾

Unless otherwise specified, all limits ensured at $T_A = 25^\circ\text{C}$, $V_S = 3.3\text{V}$, $\text{GND} = 0\text{V}$, $-4\text{V} \leq V_{\text{CM}} \leq 27\text{V}$, and $R_L = \infty$, Offset (Pin 7) is grounded, 10nF between V_S and GND. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Min ⁽²⁾	Typ ⁽³⁾	Max ⁽²⁾	Unit	
Overall Performance (From -IN (pin 1) and +IN (pin 8) to OUT (pin 5) with pins A1 (pin 3) and A2 (pin 4) connected)							
I_S	Supply Current		0.6	1	1.3	mA	
A_V	Total Gain		19.9	20	20.1	V/V	
	Gain Drift ⁽⁴⁾	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		-2.7	± 20	ppm/ $^\circ\text{C}$	
SR	Slew Rate ⁽⁵⁾	$V_{\text{IN}} = \pm 0.165\text{V}$	0.4	0.7		V/ μs	
BW	Bandwidth		50	60		kHz	
V_{OS}	Input Offset Voltage	$V_{\text{CM}} = V_S / 2$		0.15	± 1	mV	
TCV _{OS}	Input Offset Voltage Drift ⁽⁶⁾	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		2	± 10	$\mu\text{V}/^\circ\text{C}$	
e_n	Input Referred Voltage Noise	0.1 Hz - 10 Hz, 6 Sigma		16.4		$\mu\text{V}_{\text{P-P}}$	
		Spectral Density, 1 kHz		830		nV/ $\sqrt{\text{Hz}}$	
PSRR	Power Supply Rejection Ratio	DC, $3.0\text{V} \leq V_S \leq 3.6\text{V}$, $V_{\text{CM}} = V_S/2$	70	86		dB	
	Mid-scale Offset Scaling Accuracy			± 0.15	± 0.5	%	
		Input Referred			± 0.413	mV	
Preamplifier (From input pins -IN (pin 1) and +IN (pin 8) to A1 (pin 3))							
R_{CM}	Input Impedance Common Mode	$-4\text{V} \leq V_{\text{CM}} \leq 27\text{V}$	250	295	350	k Ω	
R_{DM}	Input Impedance Differential Mode	$-4\text{V} \leq V_{\text{CM}} \leq 27\text{V}$	500	590	700	k Ω	
V_{OS}	Input Offset Voltage	$V_{\text{CM}} = V_S / 2$		± 0.15	± 1	mV	
DC CMRR	DC Common Mode Rejection Ratio	$-2\text{V} \leq V_{\text{CM}} \leq 24\text{V}$	86	96		dB	
AC CMRR	AC Common Mode Rejection Ratio ⁽⁷⁾	$f = 1\text{ kHz}$	80	94		dB	
		$f = 10\text{ kHz}$		85			
CMVR	Input Common Mode Voltage Range	for 80 dB CMRR	-4		27	V	
A_{1V}	Gain ⁽⁴⁾		9.95	10.0	10.05	V/V	
$R_{\text{F-INT}}$	Output Impedance Filter Resistor		99	100	101	k Ω	
TCR _{F-INT}	Output Impedance Filter Resistor Drift			± 5	± 50	ppm/ $^\circ\text{C}$	
$A1 V_{\text{OUT}}$	A1 Output Voltage Swing	V_{OL}	$R_L = \infty$		2	10	mV
		V_{OH}		3.2	3.25		V
Output Buffer (From A2 (pin 4) to OUT (pin 5))							
V_{OS}	Input Offset Voltage	$0\text{V} \leq V_{\text{CM}} \leq V_S$	-2 -2.5	± 0.5	2 2.5	mV	
A_{2V}	Gain ⁽⁴⁾		1.99	2	2.01	V/V	
I_B	Input Bias Current of A2 ⁽⁸⁾ ,			-40		fA	
					± 20	nA	
$A2 V_{\text{OUT}}$	A2 Output Voltage Swing ^{(9) (10)}	V_{OL}	$R_L = 100\text{ k}\Omega$		4	20	mV
		V_{OH}		3.28	3.29		V

- (1) The electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (2) Datasheet min/max specification limits are ensured by test.
- (3) Typical values represent the most likely parameter norms at $T_A = +25^\circ\text{C}$, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
- (4) Both the gain of the preamplifier A_{1V} and the gain of the buffer amplifier A_{2V} are measured individually. The over all gain of both amplifiers A_V is also measured to assure the gain of all parts is always within the A_V limits
- (5) Slew rate is the average of the rising and falling slew rates.
- (6) Offset voltage drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
- (7) AC Common Mode Signal is a 5V_{PP} sine-wave (0V to 5V) at the given frequency.
- (8) Positive current corresponds to current flowing into the device
- (9) For this test input is driven from A1 stage.
- (10) For V_{OL} , R_L is connected to V_S and for V_{OH} , R_L is connected to GND.

3.3V Electrical Characteristics ⁽¹⁾ (continued)

Unless otherwise specified, all limits ensured at $T_A = 25^\circ\text{C}$, $V_S = 3.3\text{V}$, $\text{GND} = 0\text{V}$, $-4\text{V} \leq V_{\text{CM}} \leq 27\text{V}$, and $R_L = \infty$, Offset (Pin 7) is grounded, 10nF between V_S and GND. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Min ⁽²⁾	Typ ⁽³⁾	Max ⁽²⁾	Unit
I_{SC}	Output Short-Circuit Current ⁽¹¹⁾	Sourcing, $V_{\text{IN}} = V_S$, $V_{\text{OUT}} = \text{GND}$	-25	-38	-60	mA
		Sinking, $V_{\text{IN}} = \text{GND}$, $V_{\text{OUT}} = V_S$	30	46	65	

(11) Short-Circuit test is a momentary test. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C

5V Electrical Characteristics ⁽¹⁾

Unless otherwise specified, all limits ensured for at $T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $\text{GND} = 0\text{V}$, $-22\text{V} \leq V_{\text{CM}} \leq 60\text{V}$, and $R_L = \infty$, Offset (Pin 7) is grounded, 10nF between V_S and GND. **Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Min ⁽²⁾	Typ ⁽³⁾	Max ⁽²⁾	Unit	
Overall Performance (From -IN (pin 1) and +IN (pin 8) to OUT (pin 5) with pins A1 (pin 3) and A2 (pin 4) connected)							
I_S	Supply Current		0.7	1.1	1.5	mA	
A_V	Total Gain ⁽⁴⁾		19.9	20	20.1	V/V	
	Gain Drift	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		-2.8	± 20	ppm/ $^\circ\text{C}$	
SR	Slew Rate ⁽⁵⁾	$V_{\text{IN}} = \pm 0.25\text{V}$	0.6	0.83		V/ μs	
BW	Bandwidth		50	60		kHz	
V_{OS}	Input Offset Voltage			0.15	± 1	mV	
TCV_{OS}	Input Offset Voltage Drift ⁽⁶⁾	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		2	± 10	$\mu\text{V}/^\circ\text{C}$	
e_N	Input Referred Voltage Noise	0.1 Hz - 10 Hz, 6 Sigma		17.5		$\mu\text{V}_{\text{P-P}}$	
		Spectral Density, 1 kHz		890		nV/ $\sqrt{\text{Hz}}$	
PSRR	Power Supply Rejection Ratio	DC $4.5\text{V} \leq V_S \leq 5.5\text{V}$	70	90		dB	
	Mid-scale Offset Scaling Accuracy			± 0.15	± 0.5	%	
		Input Referred			± 0.625	mV	
Preamplifier (From input pins -IN (pin 1) and +IN (pin 8) to A1 (pin 3))							
R_{CM}	Input Impedance Common Mode	$0\text{V} \leq V_{\text{CM}} \leq 60\text{V}$	250	295	350	k Ω	
		$-20\text{V} \leq V_{\text{CM}} \leq 0\text{V}$	165	193	250	k Ω	
R_{DM}	Input Impedance Differential Mode	$0\text{V} \leq V_{\text{CM}} \leq 60\text{V}$	500	590	700	k Ω	
		$-20\text{V} \leq V_{\text{CM}} \leq 0\text{V}$	300	386	500	k Ω	
V_{OS}	Input Offset Voltage	$V_{\text{CM}} = V_S / 2$		± 0.15	± 1	mV	
DC CMRR	DC Common Mode Rejection Ratio	$-20\text{V} \leq V_{\text{CM}} \leq 60\text{V}$	90	105		dB	
AC CMRR	AC Common Mode Rejection Ratio ⁽⁷⁾	$f = 1\text{ kHz}$	80	96		dB	
		$f = 10\text{ kHz}$		83			
CMVR	Input Common Mode Voltage Range	for 80 dB CMRR	-22		60	V	
A_{1V}	Gain ⁽⁴⁾		9.95	10	10.05	V/V	
$R_{\text{F-INT}}$	Output Impedance Filter Resistor		99	100	101	k Ω	
$\text{TCR}_{\text{F-INT}}$	Output Impedance Filter Resistor Drift			± 5	± 50	ppm/ $^\circ\text{C}$	
$A_1 V_{\text{OUT}}$	A1 Output Voltage Swing	V_{OL}	$R_L = \infty$		2	10	mV
		V_{OH}		4.95	4.985		V

(1) The electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.

(2) Datasheet min/max specification limits are ensured by test.

(3) Typical values represent the most likely parameter norms at $T_A = +25^\circ\text{C}$, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.

(4) Both the gain of the preamplifier A_{1V} and the gain of the buffer amplifier A_{2V} are measured individually. The over all gain of both amplifiers A_V is also measured to assure the gain of all parts is always within the A_V limits

(5) Slew rate is the average of the rising and falling slew rates.

(6) Offset voltage drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

(7) AC Common Mode Signal is a $5V_{\text{PP}}$ sine-wave (0V to 5V) at the given frequency.

5V Electrical Characteristics ⁽¹⁾ (continued)

Unless otherwise specified, all limits ensured for at $T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $\text{GND} = 0\text{V}$, $-22\text{V} \leq V_{\text{CM}} \leq 60\text{V}$, and $R_L = \infty$, Offset (Pin 7) is grounded, 10nF between V_S and GND. **Boldface** limits apply at the temperature extremes.

Parameter	Test Conditions		Min ⁽²⁾	Typ ⁽³⁾	Max ⁽²⁾	Unit	
Output Buffer (From A2 (pin 4) to OUT(pin 5))							
V_{OS}	Input Offset Voltage	$0\text{V} \leq V_{\text{CM}} \leq V_S$	-2 -2.5	± 0.5	2 2.5	mV	
A_{2V}	Gain ⁽⁸⁾		1.99	2	2.01	V/V	
I_B	Input Bias Current of A2 ⁽⁹⁾			-40		fA	
					± 20	nA	
$A_2 V_{\text{OUT}}$	A2 Output Voltage Swing ⁽¹⁰⁾ ⁽¹¹⁾	V_{OL}	$R_L = 100\text{ k}\Omega$		4	20	mV
		V_{OH}		4.98	4.99		V
I_{SC}	Output Short-Circuit Current ⁽¹²⁾	Sourcing, $V_{\text{IN}} = V_S$, $V_{\text{OUT}} = \text{GND}$	-25	-42	-60	mA	
		Sinking, $V_{\text{IN}} = \text{GND}$, $V_{\text{OUT}} = V_S$	30	48	65		

(8) Both the gain of the preamplifier A_{1V} and the gain of the buffer amplifier A_{2V} are measured individually. The over all gain of both amplifiers A_V is also measured to assure the gain of all parts is always within the A_V limits

(9) Positive current corresponds to current flowing into the device

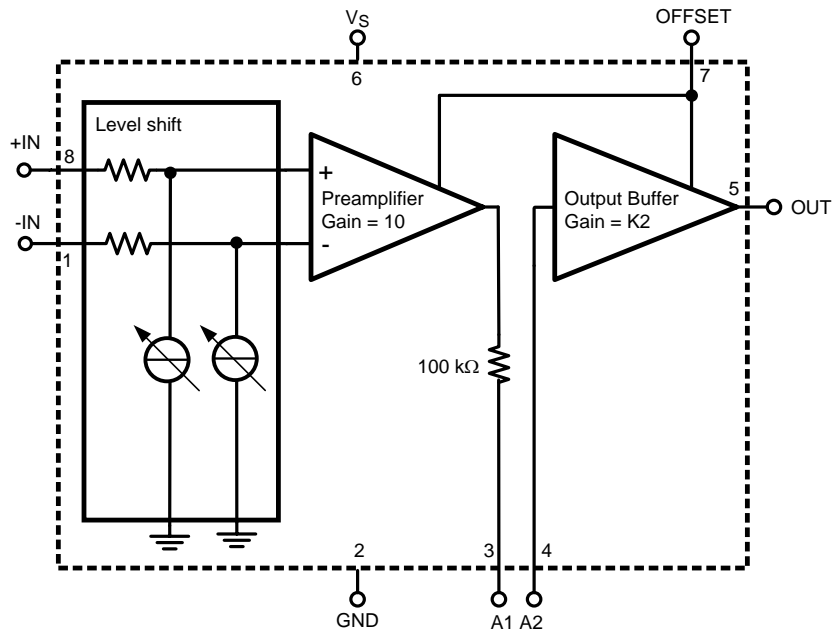
(10) For this test input is driven from A1 stage.

(11) For V_{OL} , R_L is connected to V_S and for V_{OH} , R_L is connected to GND.

(12) Short-Circuit test is a momentary test. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C

DEVICE INFORMATION

Block Diagram



K2 = 2

Figure 1. Block Diagram

Connection Diagram

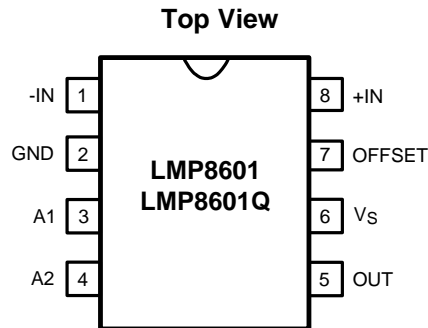


Figure 2. 8-Pin SOIC Package see package number D0008A

Table 1. Pin Descriptions

Name	Pin No.	Description	
GND	2	Power Supply	Power Ground
V _S	6		Positive Supply Voltage
-IN	1	Inputs	Negative Input
+IN	8		Positive Input
A1	3	Filter Network	Pre-amplifier output
A2	4		Input from the external filter network and / or A1
OFFSET	7	Offset	DC Offset for bidirectional signals

Table 1. Pin Descriptions (continued)

Name	Pin No.		Description
OUT	5	Output	Single ended output

Automotive Grade (Q) product incorporates enhanced manufacturing and support processes for the automotive market, including defect detection methodologies. Reliability qualification is compliant with the requirements and temperature grades defined in the AEC Q100 standard. Automotive Grade products are identified with the letter Q. Fully compliant PPAP documentation is available. For more information go to http://www.ti.com/lscs/ti/apps/automotive/end_equipment.page.

Typical Performance Characteristics

Unless otherwise specified, all limits ensured for at $T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $\text{GND} = 0\text{V}$, $-22 \leq V_{\text{CM}} \leq 60\text{V}$, and $R_L = \infty$, Offset (Pin 7) connected to V_S , 10nF between V_S and GND.

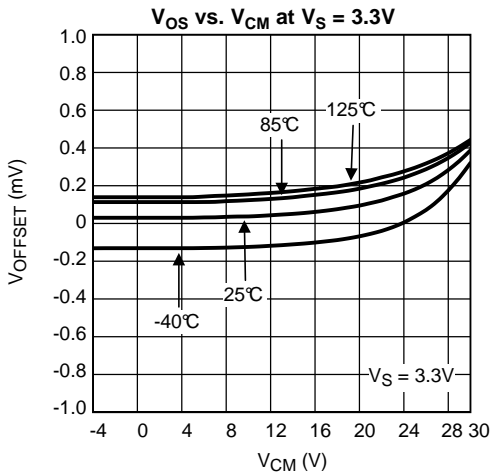


Figure 3.

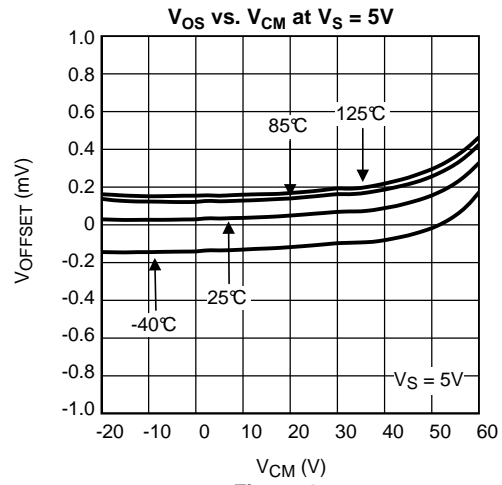


Figure 4.

Input Bias Current Over Temperature (+IN and -IN pins) at $V_S = 3.3\text{V}$

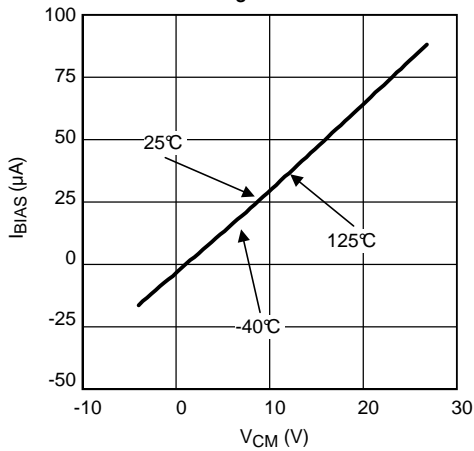


Figure 5.

Input Bias Current Over Temperature (+IN and -IN pins) at $V_S = 5\text{V}$

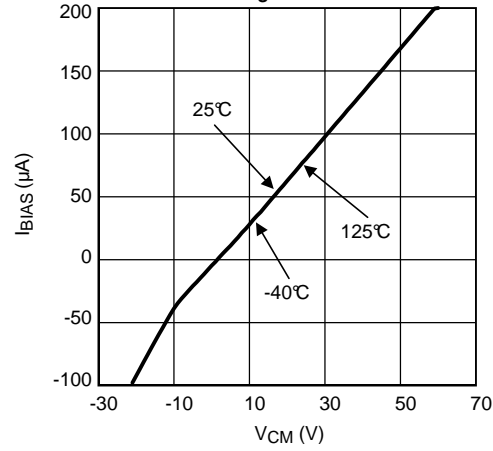


Figure 6.

Input Bias Current Over Temperature (A2 pin) at $V_S = 5\text{V}$

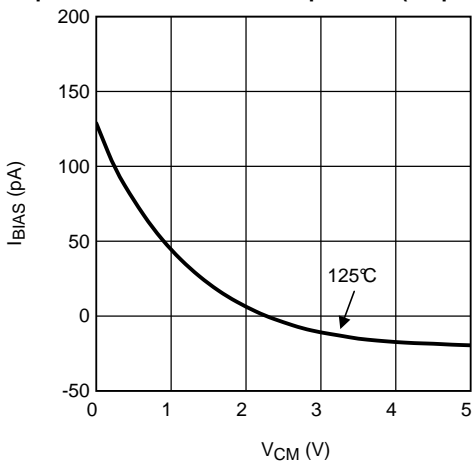


Figure 7.

Input Bias Current Over Temperature (A2 pin) at $V_S = 5\text{V}$

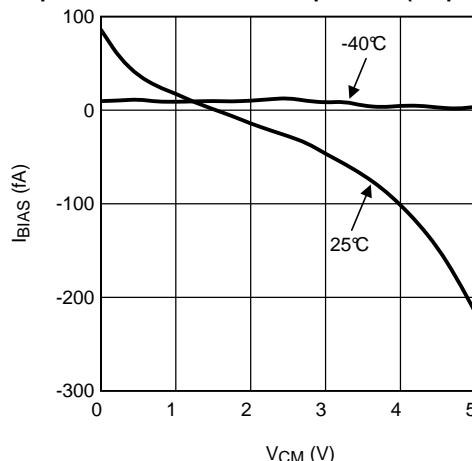


Figure 8.

Typical Performance Characteristics (continued)

Unless otherwise specified, all limits ensured for at $T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $\text{GND} = 0\text{V}$, $-22 \leq V_{\text{CM}} \leq 60\text{V}$, and $R_L = \infty$, Offset (Pin 7) connected to V_S , 10nF between V_S and GND.

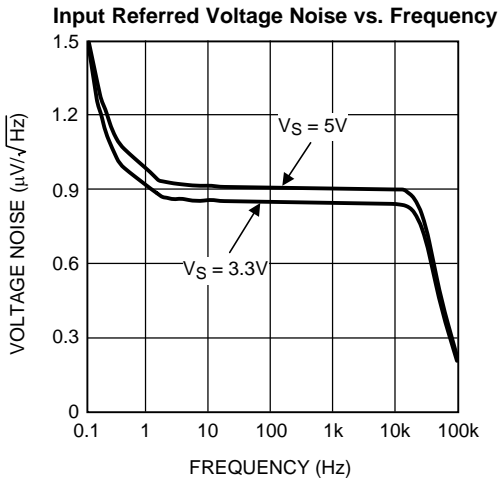


Figure 9.

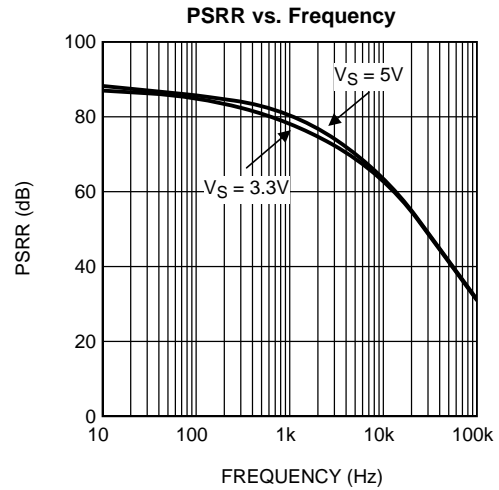


Figure 10.

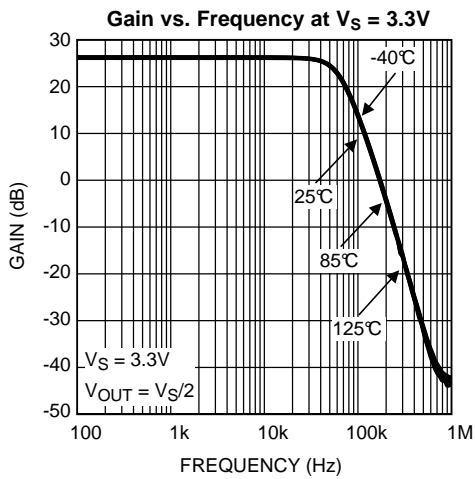


Figure 11.

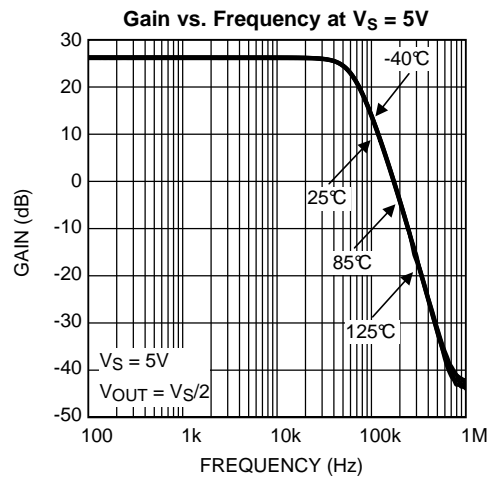


Figure 12.

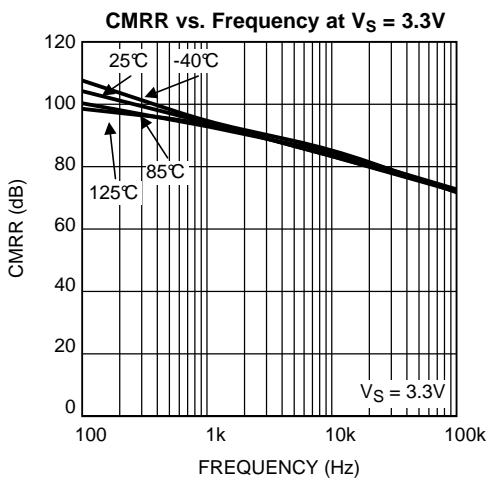


Figure 13.

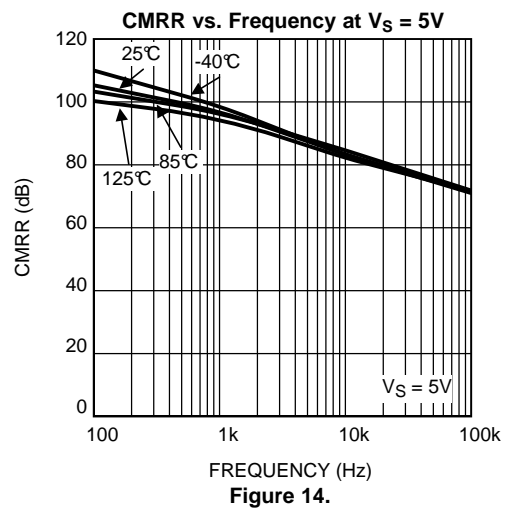


Figure 14.

Typical Performance Characteristics (continued)

Unless otherwise specified, all limits ensured for at $T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $\text{GND} = 0\text{V}$, $-22 \leq V_{\text{CM}} \leq 60\text{V}$, and $R_L = \infty$, Offset (Pin 7) connected to V_S , 10nF between V_S and GND.

Step Response at $V_S = 3.3\text{V}$

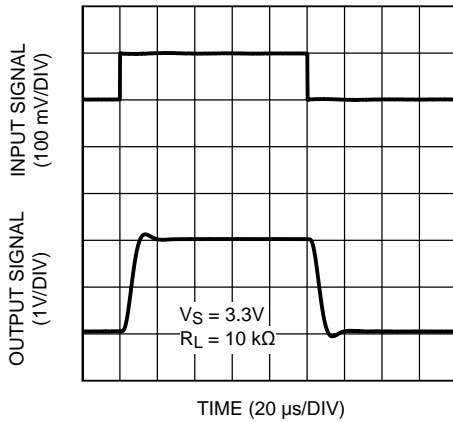


Figure 15.

Step Response at $V_S = 5\text{V}$

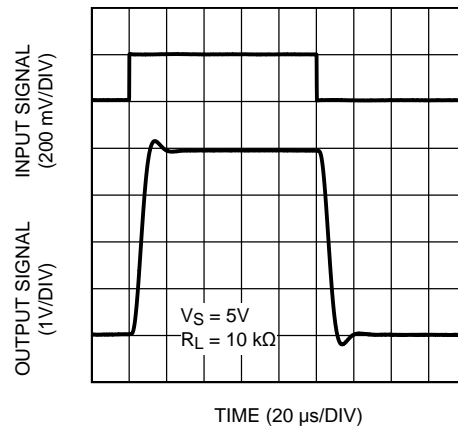


Figure 16.

Settling Time (Falling Edge) at $V_S = 3.3\text{V}$

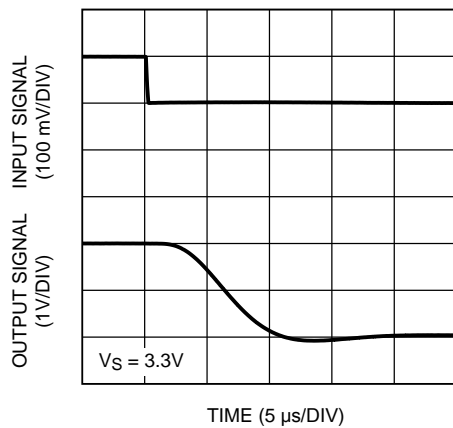


Figure 17.

Settling Time (Falling Edge) at $V_S = 5\text{V}$

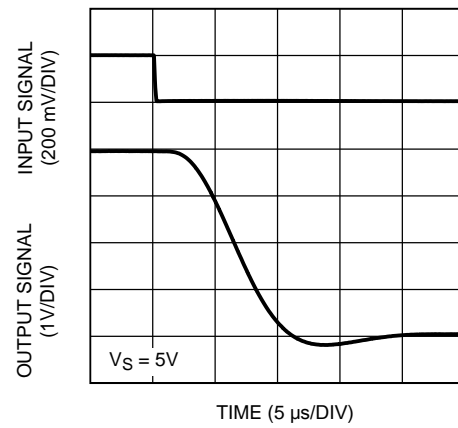


Figure 18.

Settling Time (Rising Edge) at $V_S = 3.3\text{V}$

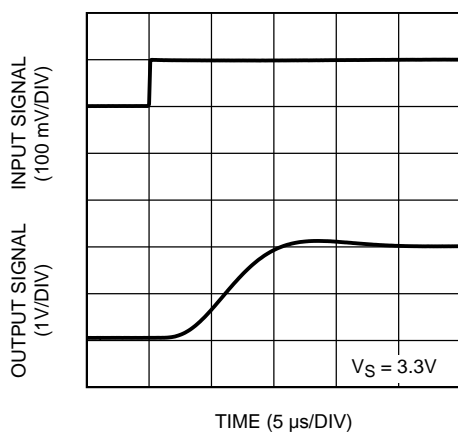


Figure 19.

Settling Time (Rising Edge) at $V_S = 5\text{V}$

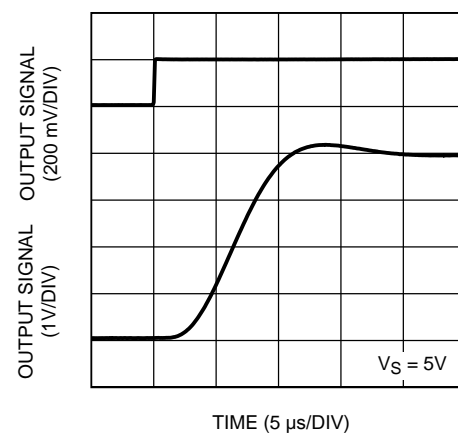


Figure 20.

Typical Performance Characteristics (continued)

Unless otherwise specified, all limits ensured for at $T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $\text{GND} = 0\text{V}$, $-22 \leq V_{\text{CM}} \leq 60\text{V}$, and $R_L = \infty$, Offset (Pin 7) connected to V_S , 10nF between V_S and GND.

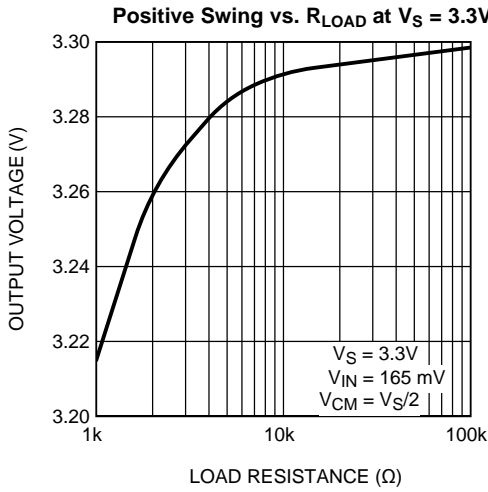


Figure 21.

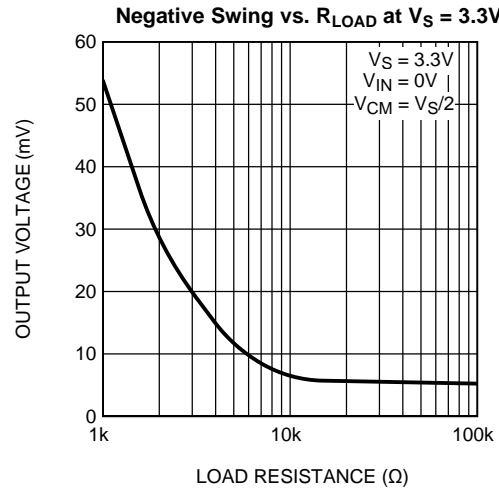


Figure 22.

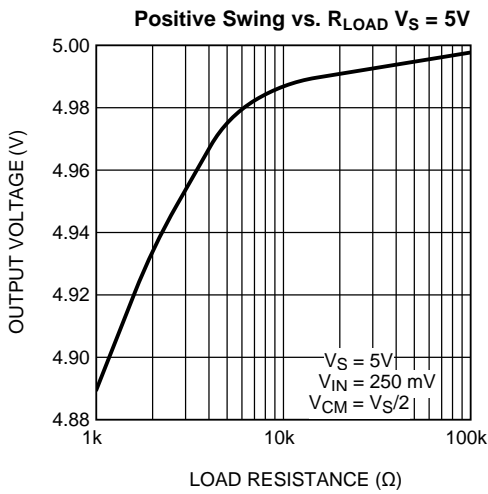


Figure 23.

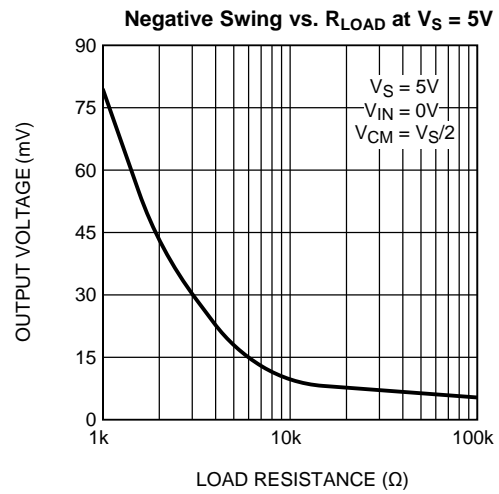


Figure 24.

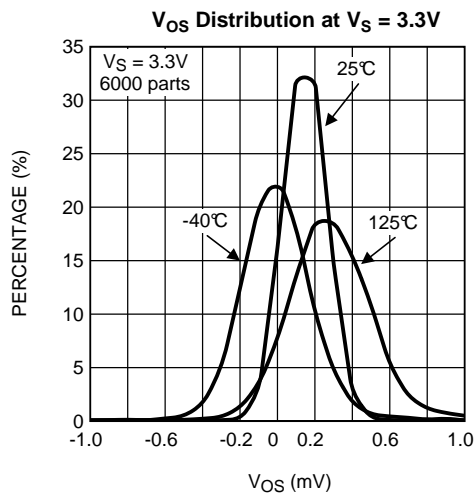


Figure 25.

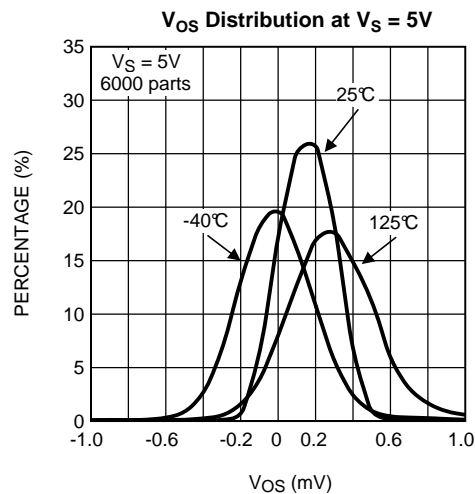


Figure 26.

Typical Performance Characteristics (continued)

Unless otherwise specified, all limits ensured for at $T_A = 25^\circ\text{C}$, $V_S = 5\text{V}$, $\text{GND} = 0\text{V}$, $-22 \leq V_{\text{CM}} \leq 60\text{V}$, and $R_L = \infty$, Offset (Pin 7) connected to V_S , 10nF between V_S and GND.

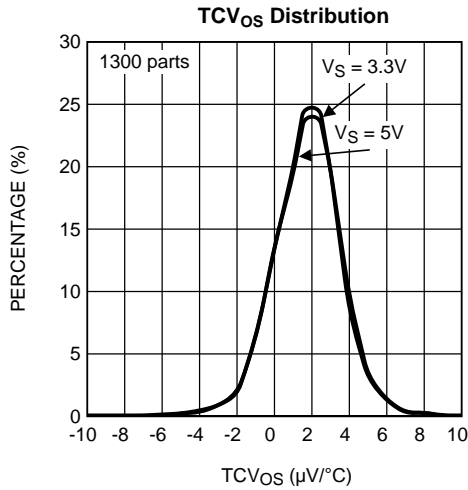


Figure 27.

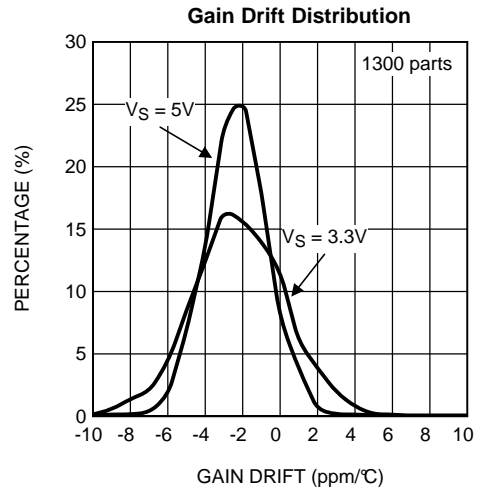


Figure 28.

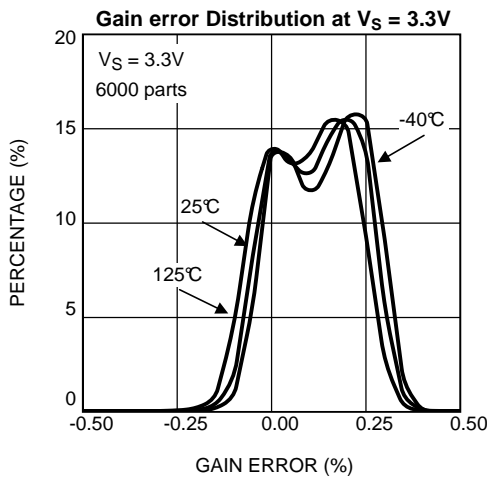


Figure 29.

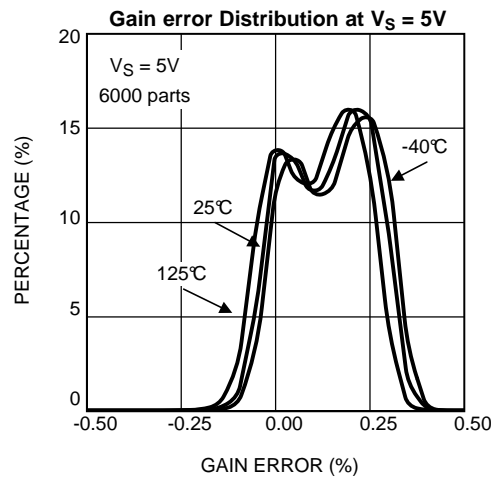


Figure 30.

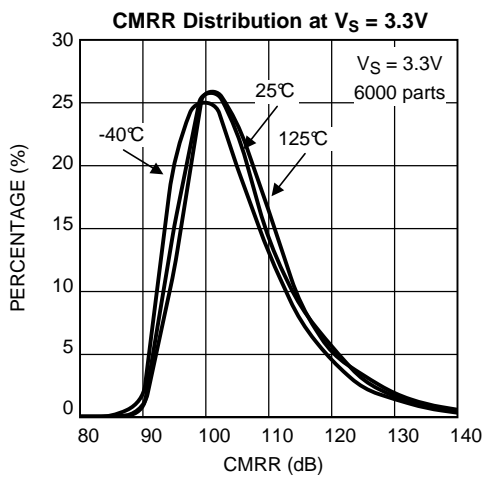


Figure 31.

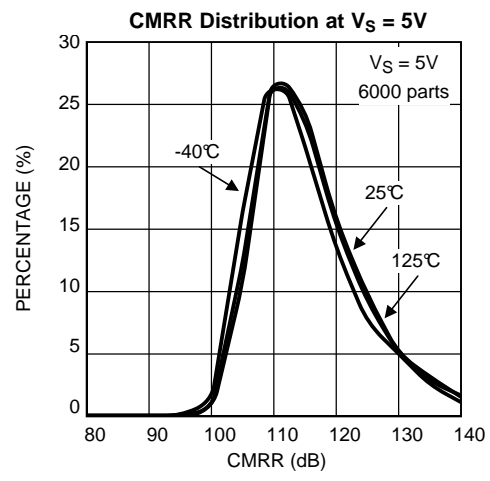


Figure 32.

APPLICATION INFORMATION

GENERAL

The LMP8601 and LMP8601Q are fixed gain differential voltage precision amplifiers with a gain of 20x and a -22V to +60V input common mode voltage range when operating from a single 5V supply or a -4V to +27V input common mode voltage range when operating from a single 3.3V supply. The LMP8601 and LMP8601Q are members of the LMP family and are ideal parts for unidirectional and bidirectional current sensing applications. Because of the proprietary chopping level-shift input stage the LMP8601/LMP8601Q achieve very low offset, very low thermal offset drift, and very high CMRR. The LMP8601 and LMP8601Q will amplify and filter small differential signals in the presence of high common mode voltages.

The LMP8601/LMP8601Q use level shift resistors at the inputs. Because of these resistors, the LMP8601/LMP8601Q can easily withstand very large differential input voltages that may exist in fault conditions where some other less protected high-performance current sense amplifiers might sustain permanent damage.

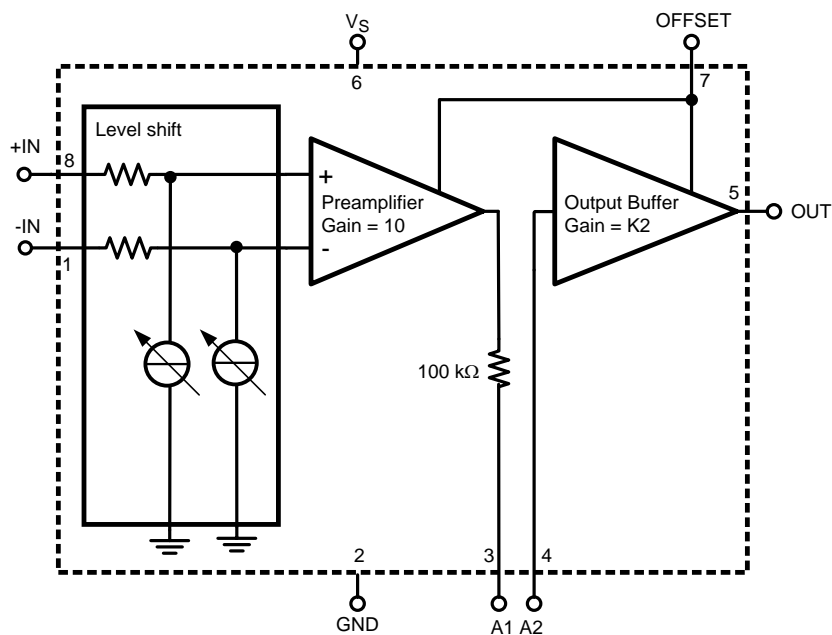
PERFORMANCE GUARANTIES

To guaranty the high performance of the LMP8601/ LMP8601Q, all minimum and maximum values shown in the parameter tables of this data sheet are 100% tested where all bold limits are also 100% tested over temperature.

THEORY OF OPERATION

The schematic shown in [Figure 33](#) gives a schematic representation of the internal operation of the LMP8601/LMP8601Q.

The signal on the input pins is typically a small differential voltage across a current sensing shunt resistor. The input signal may appear at a high common mode voltage. The input signals are accessed through two input resistors. The proprietary chopping level-shift current circuit pulls or pushes current through the input resistors to bring the common mode voltage behind these resistors within the supply rails. Subsequently, the signal is gained up by a factor of 10 and brought out on the A1 pin through a trimmed 100 kΩ resistor. In the application, additional gain adjustment or filtering components can be added between the A1 and A2 pins as will be explained in subsequent sections. The signal on the A2 pin is further amplified by a factor of 2 and brought out on the OUT pin. The OFFSET pin allows the output signal to be level-shifted to enable bidirectional current sensing as will be explained below.



K2 = 2

Figure 33. Theory of Operation

ADDITIONAL SECOND ORDER LOW PASS FILTER

The LMP8601/LMP8601Q has a third order Butterworth low-pass characteristic with a typical bandwidth of 60 kHz integrated in the preamplifier stage of the part. The bandwidth of the output buffer can be reduced by adding a capacitor on the A1 pin to create a first order low pass filter with a time constant determined by the 100 kΩ internal resistor and the external filter capacitor.

It is also possible to create an additional second order Sallen-Key low pass filter by adding external components R_2 , C_1 and C_2 . Together with the internal 100 kΩ resistor R_1 as illustrated in [Figure 34](#), this circuit creates a second order low-pass filter characteristic.

When the corner frequency of the additional filter is much lower than 60 kHz, the transfer function of the described amplifier can be written as:

$$H(s) = \frac{K_1 * K_2 \frac{1}{R_1 R_2 C_1 C_2}}{s^2 + s * \left[\frac{1}{R_1 C_2} + \frac{1}{R_2 C_2} + \frac{(1 - K_2)}{R_2 C_1} \right] + \frac{1}{R_1 R_2 C_1 C_2}} \quad (1)$$

Where K_1 equals the gain of the preamplifier and K_2 that of the buffer amplifier.

[Equation 1](#) can be written in the normalized frequency response for a 2nd order low pass filter:

$$G(j\omega) = K_1 * \frac{K_2}{\frac{(j\omega)^2}{\omega_0^2} + \frac{j\omega}{Q\omega_0} + 1} \quad (2)$$

The cutoff frequency ω_0 in rad/sec (divide by 2π to get the cut-off frequency in Hz) is given by:

$$\omega_0 = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} \quad (3)$$

and the quality factor of the filter is given by:

$$Q = \frac{\sqrt{R_1 R_2 C_1 C_2}}{R_1 C_1 + R_2 C_1 + (1 - K_2) * R_1 C_2} \quad (4)$$

With $K_2 = 2x$, [Equation 4](#) transforms results in:

$$Q = \frac{\sqrt{R_1 R_2 C_1 C_2}}{R_1 C_1 + R_2 C_1 - R_1 C_2} \quad (5)$$

With this filter gain $K_2 = 2x$, the design procedure can be very simple if the two capacitors are chosen to be equal, $C_1 = C_2 = C$. In this case, given the predetermined value of $R_1 = 100\text{k}\Omega$ (the internal resistor), the quality factor is set solely by the value of the resistor R_2 .

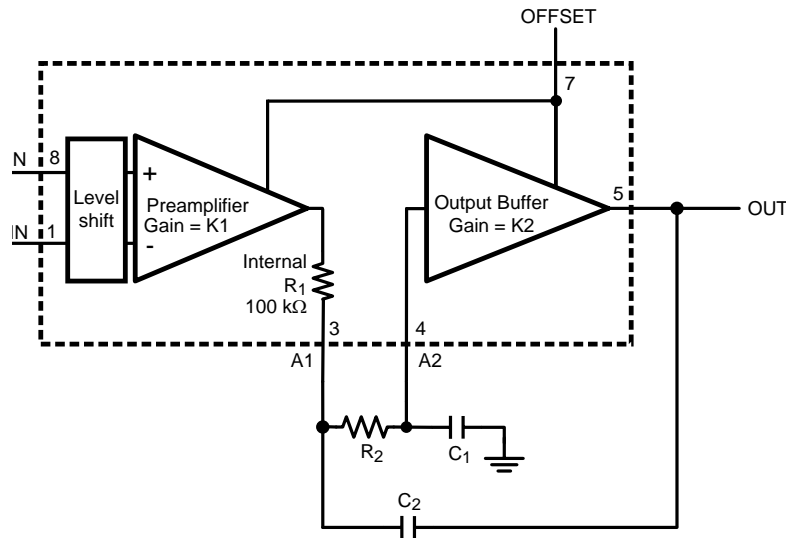
R_2 can be calculated based on the desired value of Q as the first step of the design procedure with [Equation 6](#):

$$R_2 = \frac{R_1}{Q^2} \quad (6)$$

For instance, the value of Q can be set to $0.5\sqrt{2}$ to create a Butterworth response, to $1/\sqrt{3}$ to create a Bessel response, or a 0.5 to create a critically damped response. Once the value of R_2 has been found, the second and last step of the design procedure is to calculate the required value of C to give the desired low-pass cut-off frequency using:

$$C = \frac{Q}{R_1 \omega_0} \quad (7)$$

Note that the frequency response achieved using this procedure will only be accurate if the cut-off frequency of the second order filter is much smaller than the intrinsic 60 kHz low-pass filter. In other words, to have the frequency response of the LMP8601/LMP8601Q circuit chosen such that the internal poles do not affect the external second order filter.



$K1 = 10, K2 = 2$

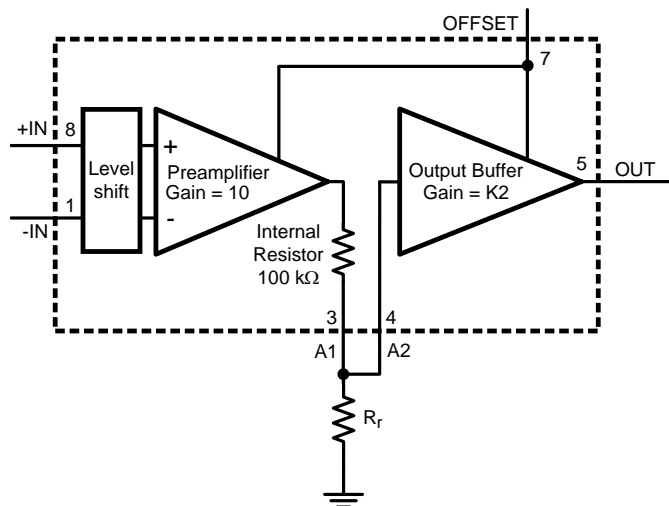
Figure 34. Second Order Low Pass Filter

GAIN ADJUSTMENT

The gain of the LMP8601/LMP8601Q is 20; however, this gain can be adjusted as the signal path in between the two internal amplifiers is available on the external pins.

Reduce Gain

Figure 35 shows the configuration that can be used to reduce the gain of the LMP8601/LMP8601Q.



$K2 = 2$

Figure 35. Reduce Gain

R_r creates a resistive divider together with the internal 100 kΩ resistor such that the reduced gain G_r becomes:

$$G_r = \frac{20 R_r}{R_r + 100 \text{ k}\Omega} \quad (8)$$

Given a desired value of the reduced gain G_r , using this equation the required value for R_r can be calculated with:

$$R_r = 100 \text{ k}\Omega \times \frac{G_r}{20 - G_r} \quad (9)$$

Increase Gain

Figure 36 shows the configuration that can be used to increase the gain of the LMP8601/LMP8601Q.

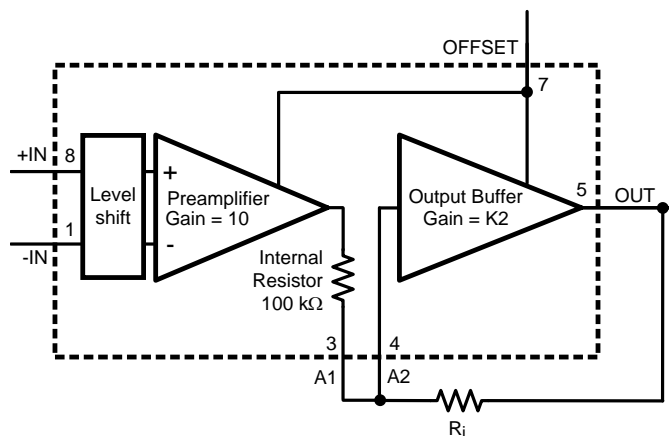
R_i creates positive feedback from the output pin to the input of the buffer amplifier. The positive feedback increases the gain. The increased gain G_i becomes:

$$G_i = \frac{20 R_i}{R_i - 100 \text{ k}\Omega} \quad (10)$$

From this equation, for a desired value of the gain, the required value of R_i can be calculated with:

$$R_i = 100 \text{ k}\Omega \times \frac{G_i}{G_i - 20} \quad (11)$$

It should be noted from the equation for the gain G_i that for large gains R_i approaches 100 k Ω . In this case, the denominator in the equation becomes close to zero. In practice, for large gains the denominator will be determined by tolerances in the value of the external resistor R_i and the internal 100 k Ω resistor. In this case, the gain becomes very inaccurate. If the denominator becomes equal to zero, the system will even become unstable. It is recommended to limit the application of this technique to gain values of 50 or smaller.



$K2 = 2$

Figure 36. Increase Gain

BIDIRECTIONAL CURRENT SENSING

The signal on the A1 and OUT pins is ground-referenced when the OFFSET pin is connected to ground. This means that the output signal can only represent positive values of the current through the shunt resistor, so only currents flowing in one direction can be measured. When the offset pin is tied to the positive supply rail, the signal on the A1 and OUT pins is referenced to a mid-rail voltage which allows bidirectional current sensing. When the offset pin is connected to a voltage source, the output signal will be level shifted to that voltage divided by two. In principle, the output signal can be shifted to any voltage between 0 and $V_S/2$ by applying twice that voltage to the OFFSET pin.

With the offset pin connected to the supply pin (V_S) the operation of the amplifier will be fully bidirectional and symmetrical around 0V differential at the input pins. The signal at the output will follow this voltage difference multiplied by the gain and at an offset voltage at the output of half V_S .

Example:

With 5V supply and a gain of 20x, a differential input signal of +10mV will result in 2.7V at the output pin. similarly -10mV at the input will result in 2.3V at the output pin.

NOTE

The OFFSET pin has to be driven from a very low-impedance source ($<10\Omega$). This is because the OFFSET pin internally connects directly to the resistive feedback networks of the two gain stages. When the OFFSET pin is driven from a relatively large impedance (e.g. a resistive divider between the supply rails) accuracy will decrease.

POWER SUPPLY DECOUPLING

In order to decouple the LMP8601/LMP8601Q from AC noise on the power supply, it is recommended to use a 0.1 μF bypass capacitor between the V_S and GND pins. This capacitor should be placed as close as possible to the supply pins. In some cases an additional 10 μF bypass capacitor may further reduce the supply noise.

DRIVING SWITCHED CAPACITIVE LOADS

Some ADCs load their signal source with a sample and hold capacitor. The capacitor may be discharged prior to being connected to the signal source. If the LMP8601/LMP8601Q is driving such ADCs the sudden current that should be delivered when the sampling occurs may disturb the output signal. This effect was simulated with the circuit shown in Figure 37 where the output is to a capacitor that is driven by a rail to rail square wave.

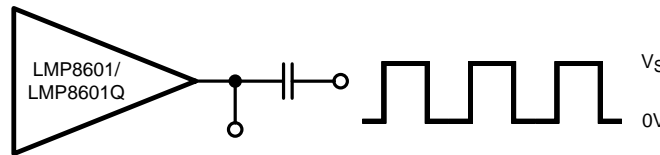


Figure 37. Driving Switched Capacitive Load

This circuit simulates the switched connection of a discharged capacitor to the LMP8601/LMP8601Q output. The resulting V_{OUT} disturbance signals are shown in Figure 38 and Figure 39.

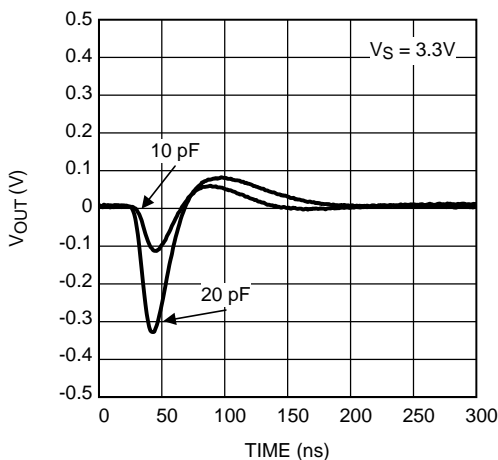


Figure 38. Capacitive Load Response at 3.3V

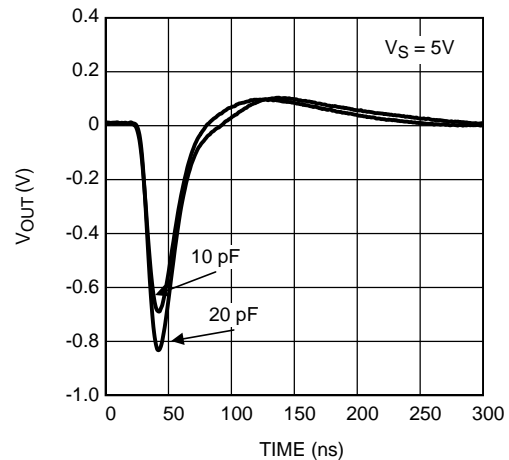


Figure 39. Capacitive Load Response at 5.0V

These figures can be used to estimate the disturbance that will be caused when driving a switched capacitive load. To minimize the error signal introduced by the sampling that occurs on the ADC input, an additional RC filter can be placed in between the LMP8601/LMP8601Q and the ADC as illustrated in Figure 40.

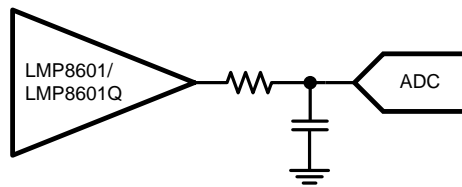


Figure 40. Reduce Error When Driving ADCs

The external capacitor absorbs the charge that flows when the ADC sampling capacitor is connected. The external capacitor should be much larger than the sample and hold capacitor at the input of the ADC and the RC time constant of the external filter should be such that the speed of the system is not affected.

LOW SIDE CURRENT SENSING APPLICATION

Figure 41 illustrates a low side current sensing application with a low side driver. The power transistor is pulse width modulated to control the average current flowing through the inductive load which is connected to a relatively high battery voltage. The current through the load is measured across a shunt resistor R_{SENSE} in series with the load. When the power transistor is on, current flows from the battery through the inductive load, the shunt resistor and the power transistor to ground. In this case, the common mode voltage on the shunt is close to ground. When the power transistor is off, current flows through the inductive load, through the shunt resistor and through the freewheeling diode. In this case the common mode voltage on the shunt is at least one diode voltage drop above the battery voltage. Therefore, in this application the common mode voltage on the shunt is varying between a large positive voltage and a relatively low voltage. Because the large common mode voltage range of the LMP8601/LMP8601Q and because of the high AC common mode rejection ratio, the LMP8601/LMP8601Q is very well suited for this application.

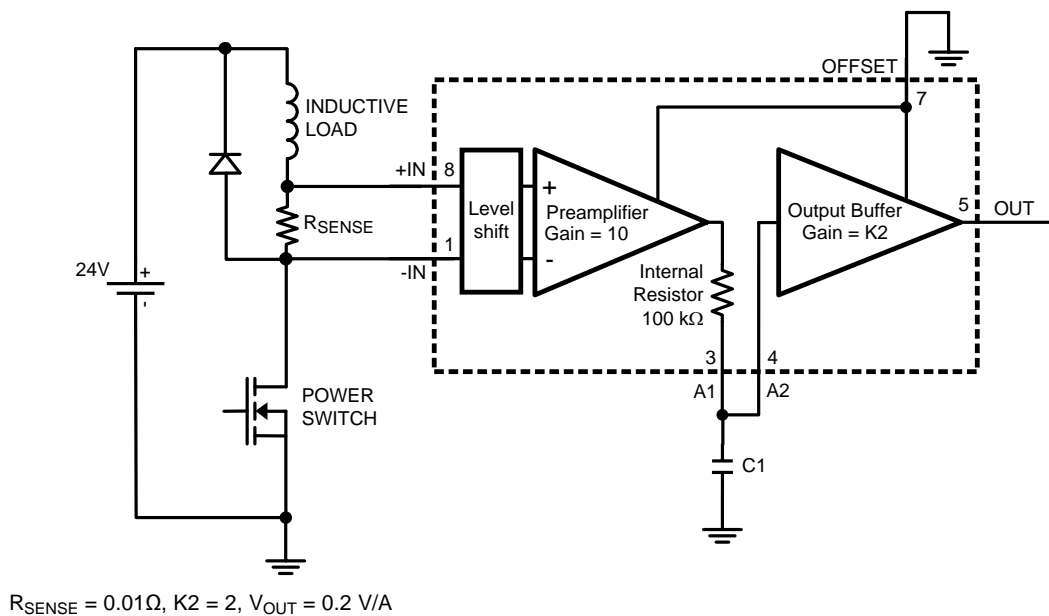


Figure 41. Low Side Current Sensing Application

HIGH SIDE CURRENT SENSING APPLICATION

Figure 42 illustrates the application of the LMP8601/LMP8601Q in a high side sensing application. This application is similar to the low side sensing discussed above, except in this application the common mode voltage on the shunt drops below ground when the driver is switched off. Because the common mode voltage range of the LMP8601/LMP8601Q extends below the negative rail, the LMP8601/LMP8601Q is also very well suited for this application.

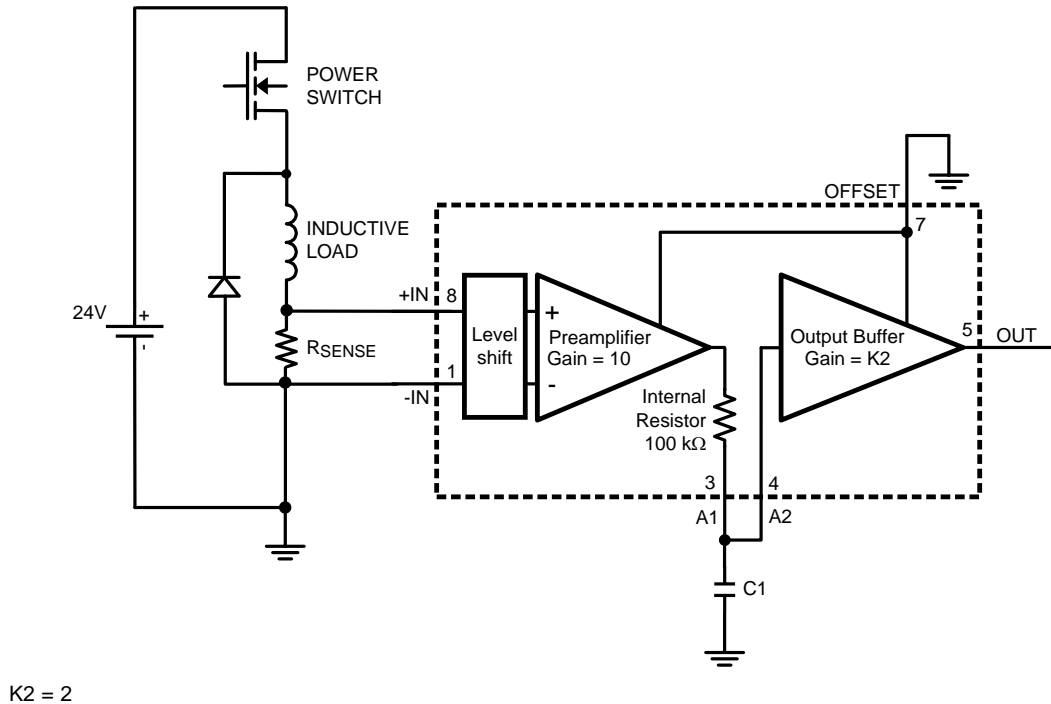


Figure 42. High Side Current Sensing Application

BATTERY CURRENT MONITOR APPLICATION

This application example shows how the LMP8601/LMP8601Q can be used to monitor the current flowing in and out a battery pack. The fact that the LMP8601/LMP8601Q can measure small voltages at a high offset voltage outside the parts own supply range makes this part a very good choice for such applications. If the load current of the battery is higher then the charging current, the output voltage of the LMP8601/LMP8601Q will be above the “half offset voltage” for a net current flowing out of the battery. When the charging current is higher then the load current the output will be below this “half offset voltage”.

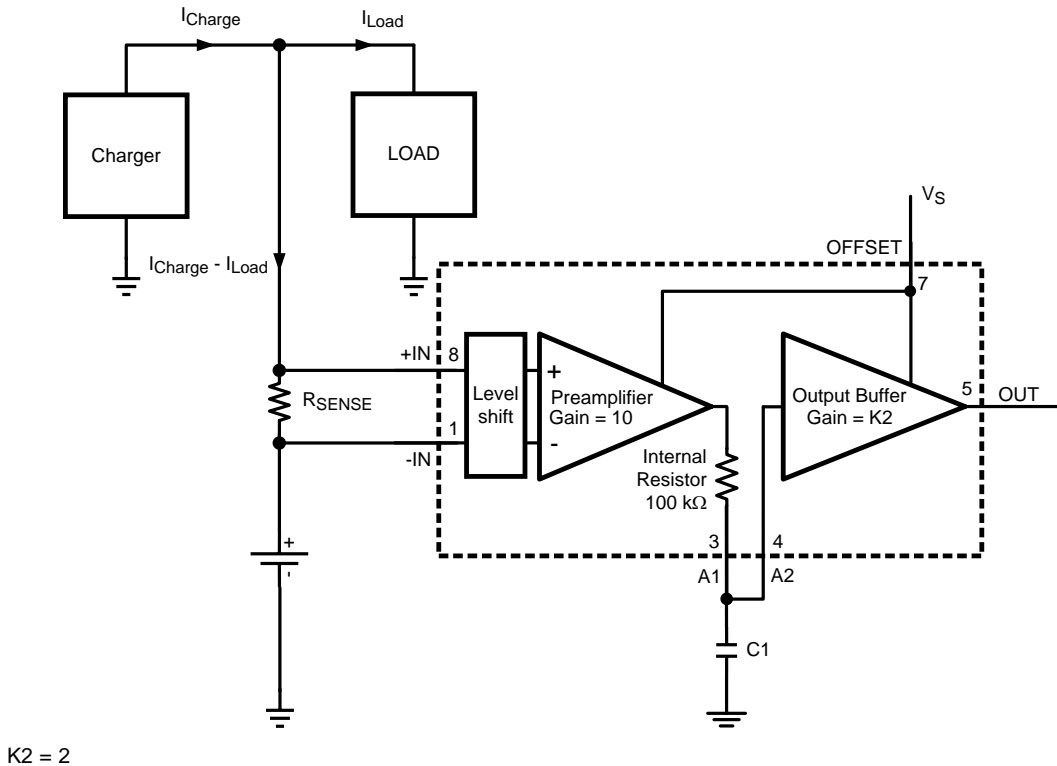


Figure 43. Battery Current Monitor Application

ADVANCED BATTERY CHARGER APPLICATION

The above circuit can be used to realize an advanced battery charger that has the capability to monitor the exact net current that flows in and out the battery as show in Figure 44. The output signal of the LMP8601/LMP8601Q is digitized with the A/D converter and used as an input for the charge controller. The Charge controller can me used to regulate the charger circuit to deliver exactly the current that is required by the load, avoiding overcharging a fully loaded battery

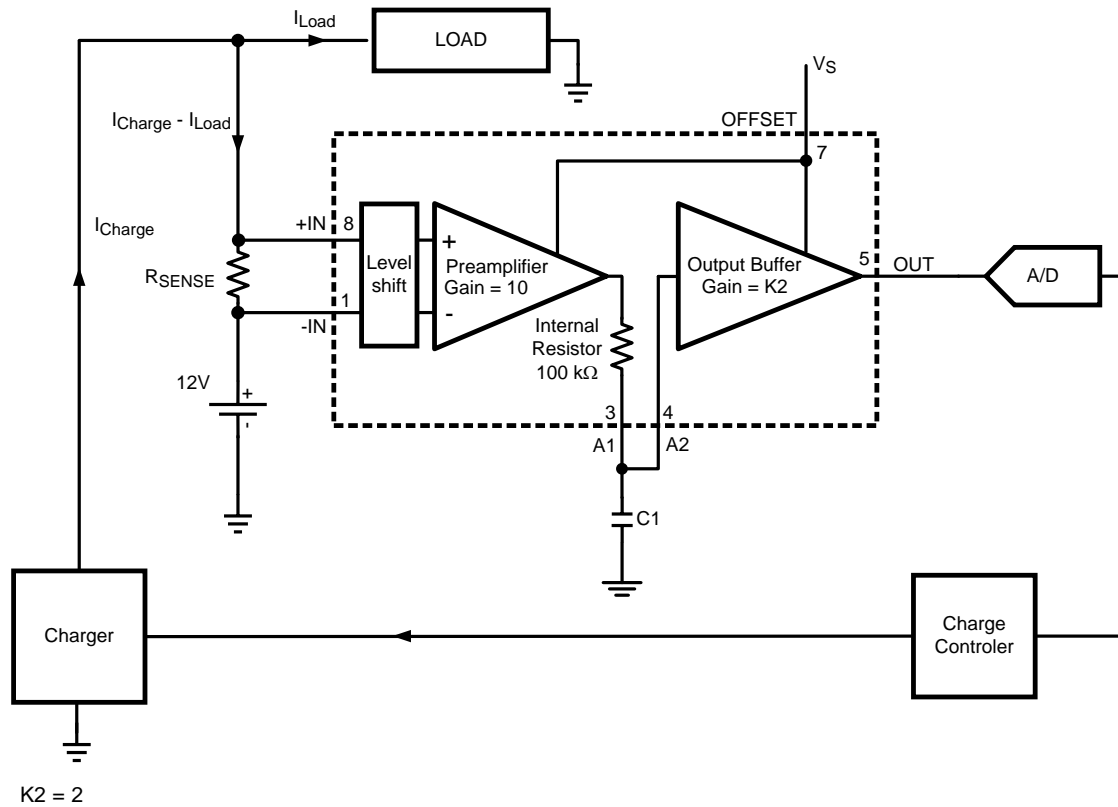
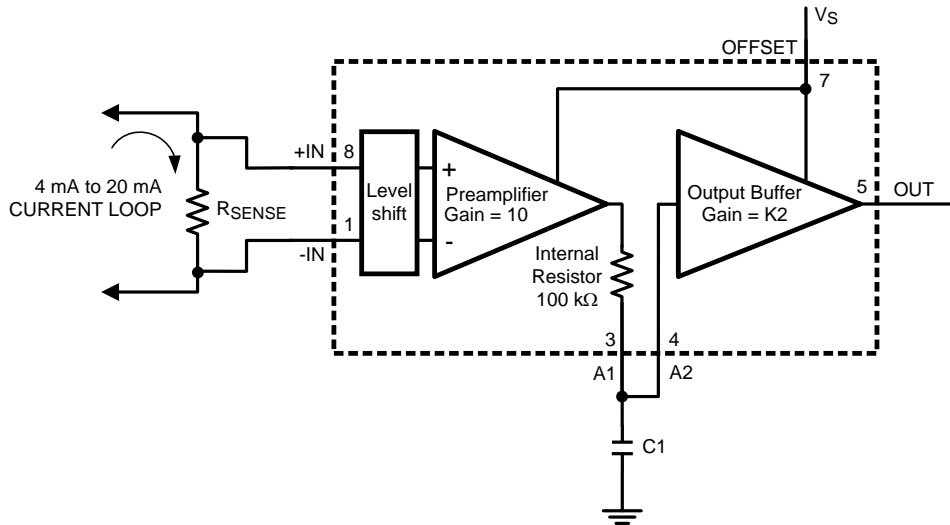


Figure 44. Advanced Battery Charger Application

CURRENT LOOP RECEIVER APPLICATION

Many industrial applications use 4 to 20 mA transmitters to send a sensor’s analog value to a central control room. The LMP8601/LMP8601Q can be used as a current loop receiver as shown in [Figure 45](#).



K2 = 2

Figure 45. Current Loop Receiver Application

REVISION HISTORY

Changes from Revision D (March 2013) to Revision E	Page
<hr/> <ul style="list-style-type: none">• Changed layout of National Data Sheet to TI format	<hr/> 22

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMP8601MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP8601MA	Samples
LMP8601MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP8601MA	Samples
LMP8601QMA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP8601QMA	Samples
LMP8601QMAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP8601QMA	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LMP8601, LMP8601-Q1 :

- Catalog: [LMP8601](#)
- Automotive: [LMP8601-Q1](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP8601MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP8601QMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP8601MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMP8601QMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com