

LM747QML Dual Operational Amplifier

Check for Samples: [LM747QML](#)

FEATURES

- **No Frequency Compensation Required**
- **Short-Circuit Protection**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Low Power Consumption**
- **No Latch-Up**

DESCRIPTION

The LM747 is a general purpose dual operational amplifier. The two amplifiers share a common bias network and power supply leads. Otherwise, their operation is completely independent.

Additional features of the LM747 are: no latch-up when input common mode range is exceeded, freedom from oscillations, and package flexibility.

Connection Diagrams

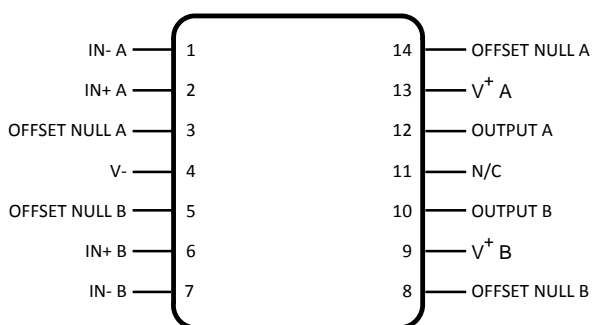


Figure 1. CDIP Top View
See Package Number J (R-GDIP-T14)

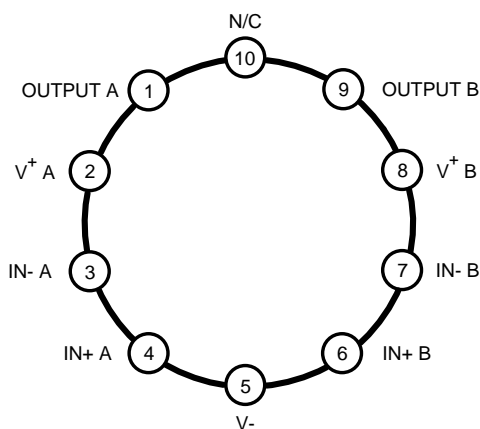


Figure 2. TO-100
See Package Number LME (O-MBCY-W10)



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾

Supply voltage	±22V
Power Dissipation ⁽²⁾	800mW
Differential Input Voltage	±30V
Input Voltage ⁽³⁾	±15V
Output Short-Circuit Duration	Indefinite
Maximum Junction Temperature (T _{Jmax})	150°C
Operating Temperature Range	-55°C ≤ T _A ≤ +125°C
Storage Temperature Range	-65°C ≤ T _A ≤ +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
- (2) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is P_{Dmax} = (T_{Jmax} - T_A)/θ_{JA} or the number given in the Absolute Maximum Ratings, whichever is lower.
- (3) For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

LM747 Electrical Characteristics DC Parameters

 The following conditions apply, unless otherwise specified. $V_{CC} = \pm 15V$, $V_{CM} = 0V$

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups		
V_{IO}	Input Offset Voltage	$R_S = 50\Omega$, $V_{CM} = -12V$		-5.0	5.0	mV	1		
				-6.0	6.0	mV	2, 3		
		$R_S = 50\Omega$, $V_{CM} = 12V$		-5.0	5.0	mV	1		
				-6.0	6.0	mV	2, 3		
		$R_S = 50\Omega$		-5.0	5.0	mV	1		
				-6.0	6.0	mV	2, 3		
		$R_S = 50\Omega$, $V_{CC} = \pm 5V$		-5.0	5.0	mV	1		
				-6.0	6.0	mV	2, 3		
I_{IO}	Input Offset Current	$V_{CM} = -12V$		-200	200	nA	1		
				-500	500	nA	2, 3		
		$V_{CM} = 12V$		-200	200	nA	1		
				-500	500	nA	2, 3		
		$V_{CC} = \pm 5V$		-200	200	nA	1		
				-500	500	nA	2, 3		
		I_{IB}^+	Input Bias Current	$V_{CM} = -12V$		0.0	500	nA	1
						0.0	1500	nA	2, 3
$V_{CM} = 12V$				0.0	500	nA	1		
				0.0	1500	nA	2, 3		
$V_{CC} = \pm 5V$				0.0	500	nA	1		
				0.0	1500	nA	2, 3		
I_{IB}^-	Input Bias Current			$V_{CM} = -12V$		0.0	500	nA	1
						0.0	1500	nA	2, 3
		$V_{CM} = 12V$		0.0	500	nA	1		
				0.0	1500	nA	2, 3		
		$V_{CC} = \pm 5V$		0.0	500	nA	1		
				0.0	1500	nA	2, 3		
		$V_{IO\ Adj}^+$	Input Offset Voltage Adjustment Range		See ⁽¹⁾	6.0		mV	1, 2, 3
		$V_{IO\ Adj}^-$	Input Offset Voltage Adjustment Range				-6.0	mV	1, 2, 3
PSRR ⁺	Power Supply Rejection Ratio	$R_S = 50\Omega$, $V_{CC} = \pm 15V$ to $\pm 5V$		77		dB	1, 2, 3		
PSRR ⁻	Power Supply Rejection Ratio	$R_S = 50\Omega$, $V_{CC} = \pm 15V$ to $\pm 5V$		77		dB	1, 2, 3		
CMRR	Common Mode Rejection Ratio	$R_S = 50\Omega$, $V_{CM} = \pm 12V$		70		dB	1, 2, 3		
I_{OS}^+	Output Short Circuit Current			-45	-9.0	mA	1, 2		
				-50	-9.0	mA	3		
I_{OS}^-	Output Short Circuit Current			9.0	45	mA	1, 2		
				9.0	50	mA	3		
I_{CC}	Supply Current				5.6	mA	1		
					5.0	mA	2		
					6.6	mA	3		

(1) Tested for CDIP only.

LM747 Electrical Characteristics DC Parameters (continued)

The following conditions apply, unless otherwise specified. $V_{CC} = \pm 15V$, $V_{CM} = 0V$

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub- groups
V_{OP}^+	Output Voltage Swing	$R_L = 10K\Omega$		12		V	1, 2, 3
		$R_L = 2K\Omega$		10		V	1, 2, 3
		$V_{CC} = \pm 20V$, $R_L = 10K\Omega$		16		V	1, 2, 3
		$V_{CC} = \pm 20V$, $R_L = 2K\Omega$		15		V	1, 2, 3
V_{OP}^-	Output Voltage Swing	$R_L = 10K\Omega$			-12	V	1, 2, 3
		$R_L = 2K\Omega$			-10	V	1, 2, 3
		$V_{CC} = \pm 20V$, $R_L = 10K\Omega$			-16	V	1, 2, 3
		$V_{CC} = \pm 20V$, $R_L = 2K\Omega$			-15	V	1, 2, 3
A_{VS}^+	Open Loop Voltage Gain	$V_O = 0$ to $+10V$, $R_L = 2K$	See ⁽²⁾	50		V/mV	1
				25		V/mV	2, 3
A_{VS}^-	Open Loop Voltage Gain	$V_O = 0$ to $-10V$, $R_L = 2K$	See ⁽²⁾	50		V/mV	1
				25		V/mV	2, 3
V_I	Input Voltage Range		See ⁽³⁾	12	-12	V	1, 2, 3
V_{OP}	Output Voltage Swing	$V_{CC} = \pm 5V$	See ⁽⁴⁾	2	-2	V	1, 2, 3

(2) Datalog reading in K = V/mV

(3) Parameter tested go-no-go only, specified by CMRR test.

(4) Specified parameter, not tested.

LM747 Electrical Characteristics AC Parameters

The following conditions apply, unless otherwise specified.

AC: $V_{CC} = \pm 15V$, $V_{CM} = 0V$

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub- groups
SR^+	Slew Rate	$A_V = 1$, $V_I = -5V$ to $+5V$		0.2		V/ μ S	9
SR^-	Slew Rate	$A_V = 1$, $V_I = +5V$ to $-5V$		0.2		V/ μ S	9
GBW	Gain Bandwidth	$V_I = 50mV$, $f = 20KHz$, $R_L = 2K\Omega$		0.25		Mhz	9

Table 1. Revision History

Released	Revision	Section	Changes
12/16/2010	A	New Release, Corporate format	1 MDS data sheet converted into one Corp. data sheet format. The drift table was eliminated from the 883 section since it did not apply; MNLM747-X Rev 0BL will be archived.
03/25/2013	A	All Sections	Changed layout of National Data Sheet to TI format

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM747H/883	ACTIVE	TO-100	LME	10	20	TBD	Call TI	Call TI	-55 to 125	LM747H/883 Q ACO LM747H/883 Q >T	Samples
LM747J/883	ACTIVE	CDIP	J	14	25	TBD	Call TI	Call TI	-55 to 125	LM747J/883 Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

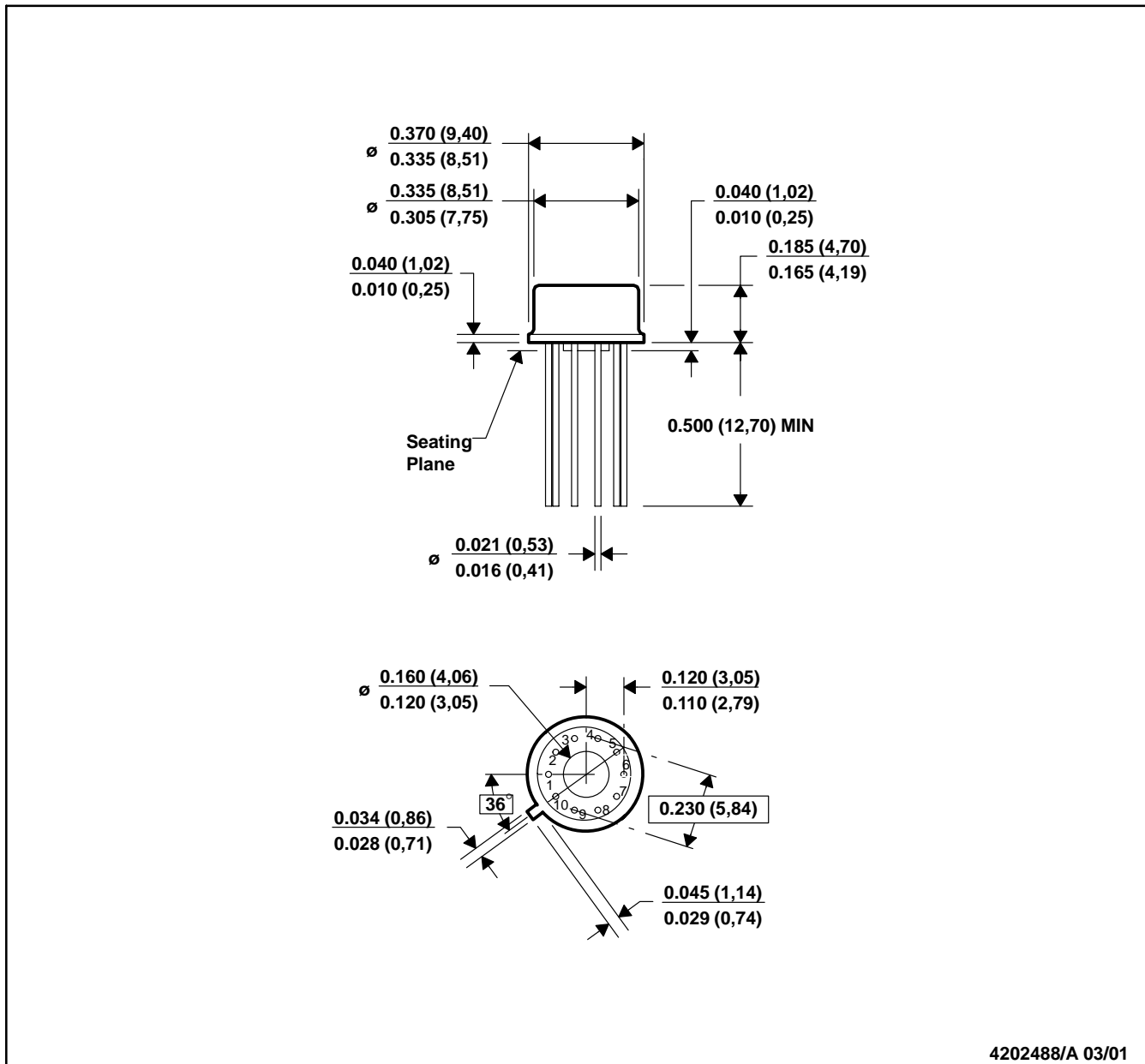


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

LME (O-MBCY-W10)

METAL CYLINDRICAL PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
 D. Pin numbers shown for reference only. Numbers may not be marked on package.
 E. Falls within JEDEC MO-006/TO-100.

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